DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI Design laboratory

EC8661(EVEN Semester) **Regulations:** R17

LIST OF EXPERIMENTS(Recommended as per Anna University)

PART I: DIGITAL SYSTEM DESIGN USING HDL & FPGA (24 Periods)

1.Design an Adder (Min 8 Bit) using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA

2.Design a Multiplier (4 Bit Min) using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA

3.Design an ALU using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA

4.Design a Universal Shift Register using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA

5.Design Finite State Machine (Moore/Mealy) using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA

6.Design Memories using HDL. Simulate it using Xilinx/Altera Software and implement by Xilinx/Altera FPGA

Compare pre synthesis and post synthesis simulation for experiments 1 to 6.
Requirements: Xilinx ISE/Altera Quartus/ equivalent EDA Tools along with Xilinx/Altera/equivalent FPGABoards

PART-II DIGITAL CIRCUIT DESIGN (24 PERIODS)

7.Design and simulate a CMOS inverter using digital flow

8.Design and simulate a CMOS Basic Gates & Flip-Flops

9.Design and simulate a 4-bit synchronous counter using a Flip-Flops

Manual/Automatic Layout Generation and Post Layout Extraction for experiments 7 to 9 Analyze the power, area and timing for experiments 7 to 9 by performing Pre Layout and Post Layout Simulations.

PART-III ANALOG CIRCUIT DESIGN (12 PERIODS)

10.Design and Simulate a CMOS Inverting Amplifier.