UNIT I DISCRETE FOURIER TRANSFORM

PART A

1. State and prove periodicity property of DFT.(Nov 2017)

x(n) ←

DFT

If x(n)=x(n+N), then X(k)=X(k+N)If

then

then х

Proof.

$$x (n + N) = x (n)$$

$$X (k + N) = X (k)$$

$$X (k) = \sum_{n=0}^{N-1} x(n)e^{-j\frac{2\pi k}{N}n}$$

$$X (k + N) = \sum_{n=0}^{N-1} x(n)e^{-j\frac{2\pi (k+N)}{N}n}$$

$$= \sum_{n=0}^{N-1} x(n)e^{-j\frac{2\pi kn}{N}n} \cdot e^{-j2\pi n} = \sum_{n=0}^{N-1} x(n)e^{-j\frac{2\pi kn}{N}n}$$

2. What is the relationship between DTFT and DFT? (April 2017/April 2018)

 $X(k) = X(\omega) / \omega = 2\pi k / N$, k=0,1,2,3....N-1

3. Why the computations in FFT algorithm is said to be in place ? (Nov2014/Nov2018)

The main advantage of in-place computation is reduction in the memory size in-place computation reduces the memory size.



'a' & 'b' are inputs and 'A' and 'B' are outputs of butterfly. For anyone input 'a' and 'b' two memory locations are required for each. One memory location to store real part and other memory location to store imagining part. So for both inputs 'a' & 'b' = 2 + 2 = 4 memory location are required. Thus outputs 'A' & 'B' are calculated by using the values 'a' & 'b' stored in memory. 'A' & 'B' complex numbers, so 2 + 2 = 4 memory location is required. Once the computation of 'A' & 'B' done then values of 'a' & 'b' are not required. Instead of storing 'A' & 'B' at other memory locations, there values are stored at the same place where 'a' & 'b' were stored. This is called as in-place computation.

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4.Indicate the number of stages, the number of complex multiplications at each stage, andthe total number of multiplications required to compute 64-point FFT using radix-algorithm. (Nov 2014)

Number of stages = $\log_2 N = \log_2 64 = 6$

Number of complex multiplication = $N_2 \log_2 N = \frac{64}{2} \times 6 = 192$ Total number of multiplications = $N \log_2 N = 64 \times 6 = 384$.

5 .Compare radix-2 DIT & DIF FFT algorithms (Nov 2016)

Similarities:

- i) Both algorithms require same number of operations to compute the DFT.
- ii) Both algorithms can be done in place and need to perform bit reversal at some place during the computation.

Differences:

DIT- FFT	DIF-FFT
1. input is bit reversed order	1. input is normal order
2. output is normal order	2. output is bit reversed order
3. the time domain sequence is decimated	3. freq. domain sequence is decimated
4. total no. of multipliers required is	4. multipliers required is $N/2(log_2N)$
$N/2(log_2N)$	adders required is N(log ₂ N)
5. In butterfly diagram, each stage of	5. In this case, in each stage of
computation, the phase factor is	computation, the phase factor is multiplied
multiplied before add &subtract operation.	after add & subtract operation.

6.How many multiplications and additions are required to compute N point DFT using radix-2 FFT? (Nov 2018)

No. of Multiplications = N^2 , No. of Additions = N(N-1)

7.Calculate 4 point DFT of the sequence $x(n) = \{1,0,-1,0\}$ (April 2018)

$$\begin{aligned} x(k) &= \sum_{n=0}^{N-1} x(n) \cdot e^{\frac{-j2\pi kn}{N}} \\ &, k = 0, 1, 2, 3 \end{aligned}$$

N=4,
$$X(k) &= x(0) + x(1) e^{-j2\pi k/4} + x(2) e^{-j\pi k} + x(3) e^{-j3\pi k/2} \\ X(k) &= 1 - e^{-j\pi k}, k = 0, 1, 2, 3 \end{aligned}$$

$$X(k) &= \{0, 2, 0, 2\}$$

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Department Of ECE/III YEAR/V SEMESTER 2019-2020 8.What is the smallest number of DFTs and IDFTs needed to compute the linear convolution of a length 50 sequence with a length of 800 sequence is to be computed using 64 point DFT & IDFT. (May 2016)

Number of DFTs and IDFTs for N point sequence = Total length of the sequence / N Total number of DFTs and IDFTs using 64 point DFT is 13. (849/64 = 13.26)

9. Test the causality and stability of $y(n) = \sin x(n)$ (Nov 2016)

LTI system is stable if and only if its impulse response is absolutely summable . ie.,

$$\sum_{k=-\infty}^{\infty} (h(k)) = -\infty + \dots + 0 + \dots + \infty = \infty$$

Therefore above system is Unstable. This system depends on only present input samples. Therefore it is causal system.

10. Write the DFT and inverse DFT for an N-point sequences.(APRIL/MAY 2019)

The sequence of *N* complex numbers $x_0, ..., x_{N-1}$ is transformed into the sequence of *N* complex numbers $X_0, ..., X_{N-1}$ by the DFT according to the formula:

$$X_k = \sum_{n=0}^{N-1} x_n e^{-\frac{2\pi i}{N}kn}$$
 $k = 0, ..., N-1$

where $e^{\frac{2\pi i}{N}}$ is a primitive N'th root of unity.

The transform is sometimes denoted by the symbol \mathcal{F} , as in $\mathbf{X} = \mathcal{F} \{\mathbf{x}\}_{\text{or}} \mathcal{F}(\mathbf{x})_{\text{or}} \mathcal{F}_{\mathbf{X}}$. The inverse discrete Fourier transform (IDFT) is given by

$$x_n = \frac{1}{N} \sum_{k=0}^{N-1} X_k e^{\frac{2\pi i}{N}kn}$$
 $n = 0, \dots, N-1.$

UNIT II IIR FILTER DESIGN PART A

1. What are the methods used for digitizing analog into digital filter? (April 2018)

- (i) Approximation of derivatives
- (ii) Impulse invariant method
- (iii) Bilinear transformation method.

2. What is frequency warping in Bilinear transformation? (May 2016/ April 2018)

The mapping of analog frequency (Ω) into digital frequency (ω) is approximately linear for small value of $\Omega \& \omega$. For the higher frequencies, however the relation between $\Omega \& \omega$ becomes highly non-linear. This introduces the distortion in the frequency scale of digital filter relative to analog filter. This effect is known as warping effect.

3. What is known as prewarping or prescaling.(Nov 2016/April 2017)

For large frequency values the non linear compression that occurs in the mapping of Ω to ω is more apparent .This compression causes the transfer function at high Ω frequency to be highly distorted when it is translate to the w domain. This compression is being compensated by introducing a prescaling or prewarpping to Ω frequency scale. For bilinear transform Ω scale is converted into Ω^* scale (i.e) $\Omega^* = 2/Ts \tan (\Omega Ts/2)$ (prewarped frequency)

4.Why impulse invariant method is not preferred in the design of IIR filter other than LPF?(May 2016)

In this method the mapping from s plane to z plane is many to one. Thus there are infinite number of poles that map to the same location in the z plane producing an aliasing effect. It is inappropriate in designing high pass filters.

5.What are the properties of BLT?(Nov 2017/Nov2018)

i) It is one to one mapping ii) The relation between analog and digital frequency is nonlinear, i.e. $\Omega=2/T \tan(\omega/2)$. Due to nonlinear relation between ω and Ω distortion occurs in frequency domain of digital filter.

ii)Due to the warping effect both amplitude and phase response of analog filter are affected but the magnitude response may be preserved by applying pre- warping procedure.iii) It avoids aliasing in frequency components v)The transformation of stable analog filter results in a stable digital filter.

Butterworth filter	Chebyshev Filter
The Magnitude response of Butterworth	The Magnitude response of Chebyshev filter
filter decreases monotonically as the	exhibits ripples in pass band or stop band.
frequency increases.	Therefore it is known as Equiripple filter.

6.Compare Butterworth filter and Chebyshev filter. (Nov 2014)

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Transition width is more	The Transition width is very small
The order of Butterworth filter is large,	For the same specifications, the order of the
thus it requires more elements to	Chebyshev filter is small and is less complex.
construct.	
The Poles of the Butterworth filter lies	The poles of Chebyshev filter lies along the
along the circle.	ellipse.
Magnitude response is flat at $\omega=0$ thus it	Magnitude response produces ripples in the
is known as Maximally flat filter.	pass band or stop band thus it is known as
	equripple filter.

7. What are the requirements for the digital filter to be stable and causal? (April 2017)

A digital filter is causal if its impulse response h(n) = o, n < 0A digital filter is stable if its impulse response is absolutely summable

$$\sum_{K=-\infty}^{\infty} (h(k)) < \infty$$

8.What are the different structures for realization of IIR systems?(or) State the structure of IIR filter? (Nov 2018)

(i) Direct Form I (ii) Direct Form II (iii) Cascade Form (iv) Transposed structure (v) Parallel Form (vi) Lattice / Ladder Structures

9.List the different types of filters based on frequency response. (Nov 2017)

(i) Low Pass Filter (ii) High Pass Filter (iii) Band Pass Filter (iv) Band Reject Filter (v) Notch Filter.

10.State the use of Z Transforms in IIR filter design.(APRIL/MAY 2019)

i.One of the most important characteristics of the z-plane is that the region of filter stability is mapped to the inside of the unit circle on the z-plane. Given the H(z) transfer function of a digital filter, we can examine that function's pole locations to determine filter stability. If all poles are located inside the unit circle, the filter will be stable. On the other hand, if any pole is located outside the unit circle, the filter will be unstable.

ii.In time delay operation

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<u>UNIT III FIR FILTER DESIGN</u> <u>PART A</u>

1. What are the desirable charcteristics of the window? (Nov 2015 / Nov 2016) Features of a good window for FIR filters:

- 1. The central lobe of the frequency response of window should contain most of the energy and it should be narrow.
- 2. The highest side lobe level of the frequency response should be small.
- 3. The side lobe of the frequency response should decrease in energy rapidly as ω tends to π

2.What is Gibb's Oscillation? (or) State the effect of having abrupt discontinuity in frequency response of FIR filters. (May 2014/April 2017)

The truncation of Fourier series is known to introduce the unwanted ripples in the frequency response characteristics H(w) due to non uniform convergence of Fourier series at a discontinuity These ripples or oscillatory behaviour near the band edge of the filter is known as Gibb's phenomenon.

3.List the disadvantages of FIR filter? (Nov 2015). Disadvantages:

The duration of impulse response should be large to realize sharp cut off filters. The non-integral delay can lead to problems in some signal processing applications.

4.What are the necessary and sufficient conditions for linear phase characteristics of a FIR filter? (Nov2018)

The necessary and sufficient conditions for linear phase characteristics of a FIR filter is that the phase function should be a linear function of ω , which in turn requires constant phase delay or constant phase and group delay.

The conditions for constant phase delay are,

Phase delay, $\alpha = (N-1)/2$ (i.e., phase delay is constant)

Impulse response h(n)=h(N-1-n) (i.e. impulse response is symmetric).

5. How the zeros in FIR filter is located? (April 2018)

FIR filters contain as many poles as they have **zeros**. but all of the poles are located at the origin, . because all of the poles are **located** inside the unit circle, the **FIR filter** is ostensibly stable.

6.List out the advantages of FIR filter.(May 2016) Advantages:

1. They have no feedback. 2. They are inherently stable system .3. The rounding off noise is reduced. 4. They can be realized with linear phase

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7.Write the steps involved in FIR filter design.(Nov2017)

- 1. Choose the desired frequency response $H_d(\omega)$.
- 2. Take the inverse Fourier transform and obtain $H_d(n)$.
- 3.Convert the infinite duration sequence $H_d(n)$ to h(n).
- 4. Take Z transform of h(n) to get H(Z)

8. Draw the direct form realization of FIR system. (April 2018)



9.What do you understand by linear phase response?(Nov 2016)

The linear phase characteristics of a FIR filter is that the phase function should be a linear function of ω , which in turn requires constant phase delay or constant phase and group delay. Phase delay, $\alpha = (N-1)/2$ (i.e., phase delay is constant) Impulse response h(n)=h(N-1-n) (i.e., impulse response is symmetric

10. Realize the following causal linear phase FIR system function.

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UNIT IV FINITE WORD LENGTH EFFECTS PART A

1.Distinguish between fixed point arithmetic and floating point arithmetic?

(Nov 2017/April 2018)

Fixed point arithmetic	Floating point arithmetic
fast operation	slow operation
small dynamic range	increased dynamic range
relatively economical	more expensive due to costlier hardware
round-off errors occur onlyin addition	round-off errors can occur with both multiplication and addition
overflow occurs in addition	overflow does not arise

2. Name the three quantization errors due to finite word length register in digital filters?(Nov 2016)

1. Input quantization error 2. Coefficient quantization error 3. Product quantization error

3.Define 'dead band' of the filter. (May 2016/April 2017)

The limit cycles occur as a result of quantization effect in multiplication. The amplitudes of the output during a limit cycle are confined to a range of values called the dead band of the filter.

4. Why rounding is preferred over truncation in realizing digital filters? (April 2018)

Rounding is preferred over truncation in realizing digital filters due to (i) The quantization error due to rounding is independent of the type of arithmetic. (ii) The mean of rounding error is zero. (iii) The variance of rounding error signal is low.

5. What is product quantization error? (or) What is round-off noise error? (May 2014/Nov2018)

Product quantization error arise at the output of a multiplier. Multiplication of a 'b' bit data with a 'b' bit coefficient results in a product having 2b bits. Since a 'b' bit register is used, the multiplier output must be rounded or truncated to 'b' bits which produces an error. This error is known as product quantization error.

6.State the methods to prevent overflow. (May 2016/April 2017)

Methods to prevent overflow is 1. Saturation Arithmetic 2. Scaling

7.What is scaling (Dec 2014)

With fixed-point arithmetic it is possible for filter calculations to overflow. This happens when two numbers of the same sign add to give a value having magnitude greater than one. *MOHAMED SATHAK A.J COLLEGE OF ENGINEERING* 8

EC 8553 - Discrete Time Signal ProcessingDepartment Of ECE2019-2020Since numbers with magnitude greater than one are not representable, the result overflows. Itis used to eliminate overflow limit cycle in FIR filters.

8.What is meant by finite word length effects in digital system?(Nov 2017)

DSP algorithms are realized with special purpose digital hardware or as programs. In both the cases the numbers and co-efficient are stored in finite length registers. Therefore the co-efficient and number are quantized by truncating or rounding when they are stored. This creates error in the output. These type of effect due to finite precision representation of numbers in digital system are called finite word length effects.

9. Why rounding is preferred over truncation in realizing a digital filter?(APRIL 2019)

Rounding is preferred over truncation in realizing digital filters due to (i) The quantization error due to rounding is independent of the type of arithmetic. (ii) The mean of rounding error is zero. (iii) The variance of rounding error signal is low.

10.What is meant by floating point represention?(Nov 2018)

In floating point representation, a positive number is represented as $N_f = M \times 2^E$ where M is called mantissa and it will be in binary fraction format. The value of M will be in the range of

 $0.5 \le M \le 1$ and E is called exponent and it is either a positive or negative integer. In this form, both mantissa and exponent uses one bit for representing sign.

UNIT –V DIGITAL SIGNAL PROCESSOR PART-A

1. Mention any four applications of DSP? (April 2019)

The applications of PDSP are Digital cell phones, automated inspection, voicemail, motor control, video conferencing, Noise cancellation, Medical imaging, speech synthesis, satellite communication.

2. What are the different stages in pipelining? (April 2018)

i. The Fetch phase ii. The Decode phase iii. Memory read phase iv. The Execute phase

3.What are the different buses of TMS 320C5x and their functions?(May2014)

The TMS 320C5x architecture has four buses

- 1. Program bus (PB) 2. Program address bus (PAB) 3. Data read bus (DB)
- 4. Data read address bus (DAB)
- The program bus carriers the instruction code and immediate operands from program memory to the CPU.
- The program address bus provides address to program memory space for both read and write.
- The data read bus interconnects various elements of the CPU to data memory spaces.
- The data read address bus provides the address to access the data memory spaces.

4. What are the merits and demerits of VLIW architecture? (May 2016)

Advantages: Increased performance, Better compiler targets, potentially easier to program, Disadvantages: Increased memory use, High program memory bandwidth requirements, High power consumption, Misleading MIPS ratings.

5.What are the factors that influence the selection of DSP processor for an application? (May 2016)

The right DSP processor for a job depends heavily on the application. One processor may perform well for some applications, but be a poor choice for others. With this in mind, one can consider a number of features that vary from one DSP to another in selecting a processor. These features are: Ease of Development, Multiprocessor Support, Power Consumption and Management, Cost, Memory Organization.

6.State how spectrum meter application can be designed with DS processor (Dec 2016)

The FFT or Fast Fourier Transform spectrum analyzer uses digital signal processing techniques to analyze a waveform with Fourier transforms to provide in depth analysis of signal waveform spectra. With the FFT analyze, its able to provide facilities that cannot be provided by swept frequency analyzers, enabling fast capture and forms of analysis that are not possible with sweep / superheterodyne techniques alone.

EC 8553 – Discrete Time Signal Processing Department Of ECE 7.What is pipelining and how do define its depth? (May 2017)

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Pipelining a processor means breaking down its instruction into a series of discrete pipeline stages which can be completed in sequence by specialized hardware. The number of pipeline stages is referred to as the pipeline depth.

8.Write some commercial DSP Processors. (May 2017).

TMS320C50, TM 320C54, TM 320C55, ADSP-219x, ADSP-219xx, TMS320C3x TMS320C67x, ADSP-21xxx.

9. Give the special features of DSP processors. (May 2015)(Nov 2017)(Nov 2018)

1. Harmonics can be analyzed using Fourier analysis.

2. Generation of pulses

3. Discretizing the waveform

10.State how a digital signal Processor is different from other processor.(April 2019)

DSP processors are specialized processor for particular application purpose only. Means A specialized DSP for audio which works for audio only, like wise if it is video means that DSP is only work for video processing, like for Speech processing .. etc.

DSP processor are different than General purpose processor in terms of memory. GPP doesn't have memory but DSP has memory on SOC. Memory retirement is different for each application so based on that only DSP processors designed.