UNIT-I

OVERVIEW AND INSTRUCTIONS

PART A

1. Define Computer Architecture

Computer Architecture Is Defined As The Functional Operation Of The Individual H/W Unit In A Computer System And The Flow Of Information Among The Control Of Those Units.

2. Define Computer H/W

Computer H/W Is The Electronic Circuit And Electro Mechanical Equipment that Constitutes the Computer

3. What are the functions of control unit ?

The memory arithmetic and logic ,and input and output units store and process information and perform i/p and o/p operation, the operation of these unit must be coordinate in some way this is the task of control unit the cu is effectively the nerve center that sends the control signal to other units and sense their states.

4. What is an interrupt?

An interrupt is an event that causes the execution of one program to be suspended and

another program to be executed.

5. What are the uses of interrupts?

• Recovery from errors

• Debugging

• Communication between programs

• Use of interrupts in operating system

6. What is the need for reduced instruction chip?

• Relatively few instruction types and addressing modes.

• Fixed and easily decoded instruction formats.

• Fast single-cycle instruction execution.

• Hardwired rather than microprogrammed control.

7. Name any three of the standard I/O interface.

• SCSI (small computer system interface),bus standards

• Backplane bus standards

• IEEE 796 bus (multiuse signals)

• NUBUS

• IEEE 488 bus standard

8. Differentiate between RISC and CISC

RISC	**CISC**
Reduced Instruction Set Computer	1. Complex Instruction set computer
Simple instructions take one cycle per Operation	Complex instruction take multiple Cycles per operation.
*Few instructions and address modes are*Used.	Many instruction and address Modes.
Fixed format instructions are used.	Variable format instructions are used
Instructions are compiled and then executed by hardware.	Instructions are interpreted by the Microprogram and then executed.
RISC machines are multiple registerset.	CISC machines use single registerSet.

Complexity in the compiler	Complexity in the micro program
RISC machines are highly pipelined	CISC machines are not pipelined.

9. Explain the various classifications of parallel structures.

• SISD (single instruction stream single data stream

• SIMD(single instruction stream multiple data stream

• MIMD(multiple instruction stream multiple data stream

• MISD(multiple instruction stream single data stream

10. What is absolute addressing mode?

The address of the location of the operand is given explicitly as a part of the instruction.

Eg. Move a , 2000

11. Specify three types of data transfer techniques.

• Arithmetic data transfer

• Logical data transfer

• Programmed control data transfer

12. What is the role of MAR and MDR?

The MAR (memory address register) is used to hold the address of the location to or from which data are to be transferred and the MDR (memory data register) contains the data to be written into or read out of the addressed location.

13. What are the various types of operations required for instructions?

• Data transfers between the main memory and the CPU registers

• Arithmetic and logic operation on data

• Program sequencing and control

• I/O transfers

14. What is the role of IR and PC?

Instruction Register (IR) contains the instruction being executed. Its output is availableto the control circuits, which generate the timing signals for controlling the processing circuitsneeded to execute the instructions. The Program Counter (PC) register keeps track of the execution of the program. It contains the memory address of the instruction currently being executed . During the execution of the current instruction, the contents of the PC are updated to correspond to the address of the next instructions to be executed.

15. What are the various units in the computer?

• Input unit

• Output unit

• Control unit

• Memory unit

• Arithmetic and logical unit

16. What is an I/O channel?

An I/O channel is actually a special purpose processor, also called peripheral processor. The main processor initiates a transfer by passing the required information in the input output channel. The channel then takes over and controls the actual transfer of data.

17. What is a bus?

A collection of wires that connects several devices is called a bus.

18. Define word length?

Each group of n bits is referred to as a word of information and n is called the word

length.

19. Explain the following the address instruction?

• Three-address instruction-it can be represented as add a,b,c

Operands a,b are called source operand and c is called destination operand.

• Two-address instruction-it can be represented as Add a, b

• One address instruction-it can be represented as add a

20. Zero address instruction.

It is also possible to use instruction where the location s of all operand are defined implicitly. This operand of the use of the method for storing the operand in which called push down stack. Such instructions are sometimes referred to us zero address instruction.

21. What is the straight-line sequencing?

The CPU control circuitry automatically proceeds to fetch and execute instruction, one

ata time in the order of the increasing addresses. This is called straight line sequencing.

22. What is the role of PC?

The CPU contains a register called the program counter, which holds the address of instruction to be executed next to begin the execution of the program the address of its First instruction must be placed into the pc.

23. Define Signal

Signal - The binary information is represented in digital computers by physical quantities

called signals.

24. Define Gates

Gates – The manipulation of binary information is done by logic circuits called gates.

Gates are blocks of hardware that produce signals of binary 1 or 0 where input logic

requirements are satisfied.

25. Flip flop

Flip flop – The storage elements employed in clocked sequential circuits are called flip

flops. A flip flop is a binary cell capable of storing 1 bit of information.

26. State and explain the performance equation?

Suppose that the average number of basic steps needed to execute one machine instruction is S, where each basic step is completed in one clock cycle. If the clock cycle rate is R cycles per second, the program execution time is given by

$T = (N \times S) / R$ This is often referred to as the basic performance equation.

27. Define CPI

The term ClockCyclesPerInstructionWhich is the average number of clock cycles each

Instruction takes to execute, is often abbreviated as CPI.

CPI= CPU clock cycles/Instruction count.

30. Define Throughput and Throughput rate.

Throughput -The total amount of work done in a given time.

Throughput rate-The rate at which the total amount of work done at a given time.

PART B

1. Explain the basic functional units
2. Discuss in detail the basic concepts of instructions and its executions
3. Deduce the concept of performance and factors projecting the performance
4. What are addressing modes and enhance the types of addressing modes
5. Design logical and control unit using its instructions

UNIT-2 ARITHMETIC OPERATIONS

1. State the principle of operation of a carry look-ahead adder.

The input carry needed by a stage is directly computed from carry signals obtained from all the preceding stages i-1,i-2,…..0, rather than waiting for normal carries to supply slowly from stage to stage. An adder that uses this principle is called carry look-ahead adder.

2. What are the main features of Booth's algorithm?

1) It handles both positive and negative multipliers uniformly.

2) It achieves some efficiency in the number of addition required when the multiplier has a few large blocks of 1s.

3. How can we speed up the multiplication process?(CSE Nov/Dec 2003)

There are two techniques to speed up the multiplication process:

1) The first technique guarantees that the maximum number of summands that must be added is n/2 for n-bit operands.

2) The second technique reduces the time needed to add the summands.

4. What is bit pair recoding? Give an example.

Bit pair recoding halves the maximum number of summands. Group the Booth-recoded multiplier bits in pairs and observe the following: The pair (+1 -1) is equivalent to the pair (0 +1). That is instead of adding -1 times the multiplicand m at shift position i to +1 (M at position i+1, the same result is obtained by adding +1 (M at position i.

Eg: 11010 – Bit Pair recoding value is 0 -1 -2

5. What is the advantage of using Booth algorithm?

1) It handles both positive and negative multiplier uniformly.

2) It achieves efficiency in the number of additions required when the multiplier has

a few large blocks of 1's.

3) The speed gained by skipping 1's depends on the data.

6. Write the algorithm for restoring division.

Do the following for n times:

1) Shift A and Q left one binary position.
2) Subtract M and A and place the answer back in A.
3) If the sign of A is 1, set q0 to 0 and add M back to A.
Where A- Accumulator, M- Divisor, Q- Dividend.

7. Write the algorithm for non restoring division.

Do the following for n times:

Step 1: Do the following for n times:

1) If the sign of A is 0 , shift A and Q left one bit position and subtract M from A; otherwise , shift A and Q left and add M to A.

2) Now, if the sign of A is 0,set q0 to 1;otherwise , set q0 to0.

Step 2: if the sign of A is 1, add M to A.

8. When can you say that a number is normalized?

When the decimal point is placed to the right of the first (nonzero) significant digit, the number is said to be normalized.

9. Explain about the special values in floating point numbers.

The end values 0 to 255 of the excess-127 exponent E(are used to represent special values such as:

When E(= 0 and the mantissa fraction M is zero the value exact 0 is represented.

When E(= 255 and M=0, the value (is represented.

When E(= 0 and M (0 , denormal values are represented.

When E(= 2555 and M(0, the value represented is called Not a number.

10. Write the Add/subtract rule for floating point numbers.

1) Choose the number with the smaller exponent and shift its mantissa right a number of steps equal to the difference in exponents.

2) Set the exponent of the result equal to the larger exponent.

3) Perform addition/subtraction on the mantissa and determine the sign of the result

4) Normalize the resulting value, if necessary.

11. Write the multiply rule for floating point numbers.

1) Add the exponent and subtract 127.

2) Multiply the mantissa and determine the sign of the result .

3) Normalize the resulting value , if necessary.

12. What is the purpose of guard bits used in floating point arithmetic

Although the mantissa of initial operands are limited to 24 bits, it is important to retain extra bits, called as guard bits.

13. What are the ways to truncate the guard bits?

There are several ways to truncate the guard bits:1) Chooping 2) Von Neumann rounding 3) Rounding

14. Define carry save addition(CSA) process.

Instead of letting the carries ripple along the rows, they can be saved and introduced into the next roe at the correct weighted position. Delay in CSA is less than delay through the ripple carry adder.

15. What are generate and propagate function?

The generate function is given by

Gi=xiyi and

The propagate function is given as

Pi=xi+yi.

16. What is floating point numbers?

In some cases, the binary point is variable and is automatically adjusted as computation proceeds. In such case, the binary point is said to float and the numbers are called floating point numbers.

17. In floating point numbers when so you say that an underflow or overflow has occurred?

In single precision numbers when an exponent is less than -126 then we say that an underflow has occurred. In single precision numbers when an exponent is less than +127 then we say that an overflow has occurred.

18. What are the difficulties faced when we use floating point arithmetic?

Mantissa overflow: The addition of two mantissas of the same sign may result in a carryout of the most significant bit

Mantissa underflow: In the process of aligning mantissas, digits may flow off the right end of the mantissa.

Exponent overflow: Exponent overflow occurs when a positive exponent exceeds the maximum possible value.

Exponent underflow: It occurs when a negative exponent exceeds the maximum possible exponent value.

19. In conforming to the IEEE standard mention any four situations under which a processor sets exception flag.

Underflow: If the number requires an exponent less than -126 or in a double precision, if the number requires an exponent less than -1022 to represent its normalized form the underflow occurs.

Overflow: In a single precision, if the number requires an exponent greater than -127 or in a double precision, if the number requires an exponent greater than +1023 to represent its normalized form the underflow occurs.

Divide by zero: It occurs when any number is divided by zero.

Invalid: It occurs if operations such as 0/0 are attempted.

20. Why floating point number is more difficult to represent and process than integer?(CSE May/June 2007)

An integer value requires only half the memory space as an equivalent.IEEEdouble-precision floatingpoint value. Applications that use only integer based arithmetic will therefore also have significantly smaller memory requirement

A floating-point operation usually runs hundreds of times slower than an equivalent integer based arithmetic operation.

21. Give the booth's recoding and bit-pair recoding of the computer.

1000111101000101(CSE May/June 2006)

Booth's recoding

1 0 0 0 1 1 1 1 0 1 0 0 0 1 0 1 0

-1 0 0 +1 0 0 0 -1 +1 -1 0 0 +1 -1 +1 -1

Bit-Pair recoding:

1 0 0 0 1 1 1 1 0 1 0 0 0 1 0 1 0

-2 +1 0 -1 +1 0 +1 1

22. Draw the full adder circuit and give the truth table (CSE May/June 2007)

Inputs			Outputs	
A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

UNIT-III
PROCESSOR AND CONTROL UNIT
PART A

1. **Define MIPS .**

MIPS:One alternative to time as the metric is MIPS(Million Instruction Per Second)
MIPS=Instruction count/(Execution time x1000000).
This MIPS measurement is also called Native MIPS to distinguish it from somealternative definitions of MIPS.

2. **Define MIPS Rate:**

The rate at which the instructions are executed at a given time.

3. **Define pipelining.**

Pipelining is a technique of decomposing a sequential process into sub operations with each sub process being executed in a special dedicated segment that operates concurrently with all other segments.

4. **Define parallel processing.**

Parallel processing is a term used to denote a large class of techniques that are used to provide simultaneous data-processing tasks for the purpose of increasing the computational speed of a computer system. Instead of processing each instruction sequentially as in a conventional computer, a parallel processing system is able to perform concurrent data processing to achieve faster execution time.

5. **Define instruction pipeline.**

The transfer of instructions through various stages of the CPU instruction cycle., including fetch opcode, decode opcode, compute operand addresses. Fetch operands, execute Instructions and store results. This amounts to realizing most (or) all of the CPU in the form of multifunction pipeline called an instruction pipelining.

6. What are the steps required for a pipelinened processor to process the instruction?

• F Fetch: read the instruction from the memory

• D Decode: decode the instruction and fetch the source operand(s).

• E Execute: perform the operation specified by the instruction.

• W Write: store the result in the destination location

7. What are Hazards?

A hazard is also called as hurdle .The situation that prevents the next instruction in the instruction stream from executing during its designated Clock cycle. Stall is introduced by hazard. (Ideal stage)

8. State different types of hazards that can occur in pipeline.

The types of hazards that can occur in the pipelining were,

1. Data hazards.
2. Instruction hazards.
3. Structural hazards.

9. Define Data hazards

A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in pipeline. As a result some operation has to be delayed, and the pipeline stalls.

10. Define Instruction hazards

The pipeline may be stalled because of a delay in the availability of an instruction. For example, this may be a result of miss in cache, requiring the instruction to be fetched from the main memory. Such hazards are called as Instruction hazards or Control hazards.

11.Define Structural hazards?

The structural hazards is the situation when two instructions require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is access to memory.

12. What are the classification of data hazards?

Classification of data hazard: A pair of instructions can produce data hazard by referring reading or writing the same memory location. Assume that i is executed before J. So, the hazards can be classified as,

1. RAW hazard
2. WAW hazard

3. WAR hazard

13. Define RAW hazard : (read after write)

Instruction ‘j’ tries to read a source operand before instruction ‘i’ writes it.

14. Define WAW hazard :(write after write)

Instruction ‘j’ tries to write a source operand before instruction ‘i’ writes it.

15. Define WAR hazard :(write after read)

Instruction ‘j’ tries to write a source operand before instruction ‘i’ reads it.

16. How data hazard can be prevented in pipelining?

Data hazards in the instruction pipelining can prevented by the following techniques.

a)Operand Forwarding

b)Software Approach

17. How Compiler is used in Pipelining?

A compiler translates a high level language program into a sequence of machine instructions. To reduce N, we need to have suitable machine instruction set and a compiler that makes good use of it. An optimizing compiler takes advantages of various features of the target processor to reduce the product N*S, which is the total number of clock cycles needed to execute a program. The number of cycles is dependent not only on the choice of instruction, but also on the order in which they appear in the program. The compiler may rearrange program instruction to achieve better performance of course, such changes must not affect of the result of the computation.

18. How addressing modes affect the instruction pipelining?

Degradation of performance is an instruction pipeline may be due to address dependency where operand address cannot be calculated without available informatition needed by addressing mode for e.g. An instructions with register indirect mode cannot proceed to fetch the operand if the previous instructions is loading the address into the register. Hence operand access is delayed degrading the performance of pipeline.

19. What is locality of reference?

Many instruction in localized area of the program are executed repeatedly during some time period and the remainder of the program is accessed relatively infrequently .this is referred as locality of reference.

20. What is the need for reduced instruction chip?

• Relatively few instruction types and addressing modes.

• Fixed and easily decoded instruction formats.

• Fast single-cycle instruction execution.

• Hardwired rather than micro programmed control

21. Define memory access time?

The time that elapses between the initiation of an operation and completion of that operation ,for example ,the time between the READ and the MFC signals .This is Referred to as memory access time.

22. Define memory cycle time.

The minimum time delay required between the initiations of two successive memory operations, for example, the time between two successive READ operations.

23. Define Static Memories.

Memories that consist of circuits capable of retaining the state as long as power is applied are known as static memories.

24. List out Various branching technique used in micro program control unit?

a) Bit-Oaring

b) Using Conditional Variable

c) Wide Branch Addressing

25. How the interrupt is handled during exception?

* CPU identifies source of interrupt

* CPU obtains memory address of interrupt handles

* pc and other CPU status information are saved

* Pc is loaded with address of interrupt handler and handling program to handle it.

26. List out the methods used to improve system performance.

The methods used to improve system performance are

1. Processor clock

2.Basic Performance Equation

3.Pipelining

4.Clock rate

5.Instruction set

6.Compiler

27. What are the ways to build a datapath

28. What are the control schemes available in processors

PART B

1. State and explain the different types of hazards that can occur in a pipeline.

2.Draw and explain the structure of a superscalar processor. Also explain the flow of instruction execution in it.

3. Explain the control implementation scheme in detail

4. Implement basic structure of MIPS

5. Define data hazard and instruction hazard and explain in detail

6. Explain pipelined data path and control path

7. What are the two aspects of machine instruction? Explain it .

8. .Draw and explain the modified three-bus structure of the processor suitable for four -stage pipelined execution. How this structure is suitable to provide four-stage pipelined execution?

UNIT-IV

PARALLELISM

PART A

1. Define parallel processing

Processing data concurrently is known as parallel processing

2. Define multiprocessor system

A computer system with atleast two processor is called multiprocessor system

3. Define parallel processing program

A single program that runs on multiple processors simultaneously

4. What is cluster

A set of computers connected over a local area network that function as single large multiprocessor is called cluster

5. What is multicore

A multicore is an architectural design that places multiple processors on a single computer chip to enhance performance and allow simultaneous process of multiple tasks more efficiently. Each processor is called core

6. What is CMP and SMP

CMP- allow single chip multiprocessing

SMP- share single physical address space

7. State Amdahl's law

It states that performance improvement to be gained from using some faster mode of execution is limited by the fraction of the time the faster mode can be used

8. What is the use of Amdahl's law

It is used to calculate the performance gain that can be obtained by improving some portion of a computer.

9. What is strong scaling

Speed up achieved on a multiprocessor without increasing the size of the problem

10. What is weak scaling

Speed up achieved on a multiprocessor proportional to increase in number of processors

List four major groups of computers defined by Michael.J. Flyn

Single instruction stream – single data stream

Single instruction stream –multiple data stream

Multiple instruction stream – single data stream

Multiple instruction stream – multiple data stream

11. What is SISD

SISD have more than one functional unit, but all functional units are control by a single control unit

12. What is SIMD

SIMD receive same instruction from control unit but operate on different data sets from distinct data stream

13. What is MISD

The several processing units process the same data using different programs.

14. What is data level parallelism

Parallelism achieved by performing the same operation on independent data is known as data level parallelism

15. What is hardware multithreading

Increasing the utiutilization of a processor by switching to another thread when one thread is stalled is called hardware multithreading

16. Compare process switch and thread switch

Process switch	Thread switch
A process switch is an operation that switches the process or control from one process to another	A thread switch is an operation that switches the processor control from one one thread to another within the same process
It is very expensive	It is very cheap

17. Define interleaved or fine grained multithreading

The processor executes two or more threads at a time. It switches from one thread to another at each clock cycle. During execution if a thread is blocked because of data dependencies or memory latencies that thread is skipped and a ready thread is executed

18. Define blocked or coarse grained multithreading

he processor executes instructions of a thread sequentially and if an event causes any delay, it switches to another thread

19. What is UMA processor

UMA- Uniform Memory Access (UMA) Multiprocessors

A processor in which latency to any word in main memory is about the same matter which processor requests the access

20. What is NUMA processor

NUMA- Non Uniform Memory Access (NUMA) Multiprocessors

A type of single address multiprocessor in which some memory accesses are faster than others depending on which processor asks for which word.

PART B

1. Explain Flynn's classification in detail
2. Discuss the principle of hardware multithreading and elaborate its types
3. What are multicore processors and explain it
4. Deduce the challenges faced in parallelism
5. Discuss in detail instruction level parallelism

UNIT-V
MEMORY SYSTEM MEMORY AND I/O SYSTEMS

1. Give the classification of the Optical Media

Optical media can be classified as

CD-ROM – Compact Disk Read Only Memory

WORM – Write Once Read Many

Rewriteable - Erasable

Multifunction – WORM and Erasable

2. What is a Mini Disk?

Minidisk for data (MD-Data) is the data version of the new rewriteable storage format developed by Sony Corporation for both business and entertainment as a convenient medium for carrying music, video and data. MD can be used in three formats to support all potential uses as follows:

--A premastered optical disk

--A recordable magneto-optical disk

--A hybrid that is partially mastered and partially recordable

3. List some applications for WORM.

--Some of the application or WORM devices are

--On-Line catalogs such as automobile party's dealer

--Large Volume Distribution

--Transaction logging such as stock trading company

--Multimedia Archival

4. What are multifunctional drives

A multifunctional drive is a single unit which is capable of reading and writing a variety of disk media. This type of drive provides the permanence of a read-only device as well as full flexibility of a rewriteable device along with the powerful intermediate write once capability

5. What are types of technology used in s multifunctional drive?

Three types of technologies utilized for multifunctional drives are

*Magneto – Optical Disk for both rewriteable and WORM capability

*Magneto- Optical disk for rewriteable and dye polymer disk for WORM capability

*Phase change technology for both rewriteable and WORM capability

6. What is Migration and Archiving?

The process of moving an object from one level in the storage hierarchy to another level in that hierarchy is called migration. Migration of Objects to off-line media and removal of these objects from on-line media is called archiving.

7. What is the use of High water marks in a cache?

Cache design use a high-water mark and a low water mark to trigger cache management operations. When the cache storage fills up to the high – water mark , the cache manager starts creating more space in cache storage. Space is created by discarding objects that have not been modified and writing back those object that have been modified.

8. What are the various cache usage in a LAN –based system?

In a LAN – based system there can be as many as three stages of caches as follows

1. Disk Cache or System memory cache
2. Hard Disk cache for each object server
3. Shared network cache for all object servers

9. What are the multimedia applications which use caches?

Some Multimedia application areas where cache is extensively used are

*Multimedia Entertainment

*Education

*Office Systems

*Audio and video Mail

*Computer Architecture - Set 6

10. Explain virtual memory technique.

Techniques that automatically move program and data blocks into the physical memory when they are required for execution are called virtual memory technique

11. What are virtual and logical addresses?

The binary addresses that the processor issues for either instruction or data are called virtual or logical addresses.

12. Define translation buffer.

Most commercial virtual memory systems incorporate a mechanism that can avoid the bulk of the main memory access called for by the virtual to physical addresses translation buffer. This may be done with a cache memory called a translation buffer.

13. What is branch delay slot?

The location containing an instruction that may be fetched and then discarded because of the branch is called branch delay slot.

14. What is optical memory?

Optical or light based techniques for data storage, such memories usually employ optical disk which resemble magnetic disk in that they store binary information in concentric tracks on electromechanically rotated disks. The information is read as or written optically, however with a laser replacing the read write arm of a magnetic disk drive. Optical memory offer high storage capacities but their access rate is generally less than those of magnetic disk.

15. What are static and dynamic memories?

Static memory is memories which require periodic no refreshing. Dynamic memories are memories, which require periodic refreshing.

18. What are the components of memory management unit?

A facility for dynamic storage relocation that maps logical memory references into physical memory addresses.

A provision for sharing common programs stored in memory by different users.

19. Distinguish Between Static RAM and Dynamic RAM?

Static RAM is fast, but they come at high cost because their cells require several transistors. Less expensive RAM can be implemented if simpler cells are used. However such

cells do not retain their state indefinitely; Hence they are called Dynamic RAM.

20. Distiguish between asynchronies DRAM and synchronous RAM.

The specialized memory controller circuit provides the necessary control signals, RAS And CAS ,that govern the timing. The processor must take into account the delay in the response of the memory. Such memories are referred to as asynchronous DRAMS. The DRAM whose operations is directly synchronized with a clock signal. Such Memories are known as synchronous DRAM.

21. What do you mean associative mapping technique?

The tag of an address received from the CPU is compared to the tag bits of each block of the cache to see if the desired block is present. This is called associative mapping technique.

22. What is SCSI?

Small computer system interface can be used for all kinds of devices including RAID storage subsystems and optical disks for large- volume storage applications.

23. What are the two types of latencies associated with storage?

The latency associated with storage is divided into 2 categories

1. Seek Latencies which can be classified into Overlapped seek,Mid transfer seek and Elevator seek

2. Rotational Latencies which can be reduced either by Zero latency read or Write and Interleave factor.

24. What are the data management activities involved in a storage?

a. **Command queuing** : allows execution of multiple sequential commands with system CPU intervention. It helps in minimizing head switching and disk rotational latency

b. **Scatter – gather** : Scatter is a process whereby data is set for best fit in available block of memory or disk. Gather reassembles data into contiguous blocks on disk or in memory

25. What do you mean by Disk Spanning?

Disk spanning is a method of attaching drives to a single host uadapter. All drives appear as a single contiguous logical unit. Data is written to the first drive first and when the drive is full, the controller switches to the second drive, then the second drive writes until its full.

26. List some objectives for using RAID Systems

-RAID systems are used to meet the following objectives

-Hot backup of disk systems

-Large volume storage at lower cost

-Higher performance at lower cost

-Ease of data recovery

-High MTBF

27. What are the different levels RAID?

There are six discrete levels of RIAD functionality. They are

-Level 0 – Disk Striping

-Level 1 – Disk Mirroring

-Level 2 – Bit Interleaving of Data

-Level 3 – Bit Interleaving with dedicated parity drives

- Level 4 – Sector interleaving of data with dedicated parity drive

-Level 5 – Block interleaving of data.

28.Two Types of storage devices.

1. Primary Memory

2.Secondary Memory

29.Explain very briefly about ESDI Hard Drive

ESDI stands for enhanced small device interface was developed by a consortium of several manufacturers. ESDI converts the data into serial bit streams and uses the RLL encoding chime to pack more bits per sector. ESDI drives store a defect map containing the locations of bad and defective sectors on the drive.

30. Explain in brief about IDE

Integrated device electronics contains an integrated controller with the drive as a single unit. Interface is a simple 16-bit parallel data interface and requires the data to be written and does not need to be told where and how to write the data on the disk. .IDE Interface supports 2 drives – one drive has to be configured as the master and the second as the slave.

31. What is SCSI?

Small computer system interface can be used for all kinds of devices including RAID storage subsystems and optical disks for large- volume storage applications.

32. Define the term RELIABILITY

"Means feature that help to avoid and detect such faults. A realible system does not silently continue and delivery result that include interrected and corrupted data, instead it corrects the corruption when possible or else stops

33.Define the term AVAILABLITY:

"Means features that follow the system to stay operational even offend faults do occur. A highly available system could dis able do the main functioning portion and continue operating at the reduced capacity"

34. How the interrupt is handled during exception?

* cpu identifies source of interrupt
* cpu obtains memory address of interrupt handles
* pc and other cpu status information are saved
* Pc is loaded with address of interrupt handler and handling program to handle it

35. What is IO mapped input output?

A memory reference instruction activated the READ M (or)WRITE M control line and does not affect the IO device. Separate IO instruction are required to activate the READ IO and WRITE IO lines ,which cause a word to be transferred between the address air port and the CPU. The memory and IO address space are kept separate.

36.Specify the three types of the DMA transfer techniques?

--Single transfer mode(cyclestealing mode)

--Block Transfer Mode(Brust Mode)

--Demand Transfer Mode

--Cascade Mode

37. What is an interrupt?

An interrupt is an event that causes the execution of one program to be suspended and another program to be executed.

38. What are the uses of interrupts?

*Recovery from errors

*Debugging

*Communication between programs

*Use of interrupts in operating system

39.Define vectored interrupts.

In order to reduce the overhead involved in the polling process, a device requesting an interrupt may identify itself directly to the CPU. Then, the CPU can immediately start executing

the corresponding interrupt-service routine. The term vectored interrupts refers to allinterrupt handling schemes base on this approach.

40. Name any three of the standard I/O interface.

*SCSI (small computer system interface),bus standards

*Back plane bus standards

*IEEE 796 bus (multibus signals)

*NUBUS & IEEE 488 bus standard

41. What is an I/O channel?

An i/o channel is actually a special purpose processor, also called peripheral processor.The main processor initiates a transfer by passing the required information in the input output channel. the channel then takes over and controls the actual transfer of data.

42. Why program controlled I/O is unsuitable for high-speed data transfer?

In program controlled i/o considerable overhead is incurred. Because several program instruction have to be executed for each data word transferred between the external devices and MM.Many high speed peripheral; devices have a synchronous modes of operation. That is data transfer are controlled by a clock of fixed frequency, independent of the cpu.

47. what is the function of i/o interface?

The function is to coordinate the transfer of data between the cpu and external devices.

48. Name some of the IO devices.

*Video terminals

*Video displays

*Alphanumeric displays

*Graphics displays

* Flat panel displays

*Printers

*Plotters

49. What are the steps taken when an interrupt occurs?

*Source of the interrupt

*The memory address of the required ISP

* The program counter &cpu information saved in subroutine

*Transfer control back to the interrupted program

50. Define interface.

The word interface refers to the boundary between two circuits or devices

51. What is programmed I/O?

Data transfer to and from peripherals may be handled using this mode. Programmed I/O operations are the result of I/O instructions written in the computer program.

52. What is DMA?

A special control unit may be provided to enable transfer a block of data directly between an external device and memory without contiguous intervention by the CPU. This approach is called DMA.

PART B

1. Define cache memory. Explain the mapping process followed in cache memory. Also discuss
2. the relative advantages and disadvantages of the mapping techniques used.
3. What is virtual memory? Why is it necessary to implement virtual memory? Explain the virtual
4. memory address translation.
5. Draw and explain the various types of secondary storage devices.
6. .List the different types of interrupts. Explain briefly about mask able interrupt.
7. What is DMA? Explain the block diagram of DMA .Also describe how DMA is used to
8. transfer data from peripherals.
9. Expalin input/output processors