Mohamed Sathak A J College of Engineering

Department of Electronics and Communication Engineering

EC6601 VLSI Design Question Bank

Unit-I: MOS Transistor Principles

Part – A (2 Marks)

1.	Define threshold voltage.	
2.	What are short channel effects?	
3.	What is meant by velocity saturation?	A/M 18
4.	Define scaling. State its types.	A/M 18
5.	What is meant by channel length modulation in NMOS transistors	A/M 17, A/M 16
6.	Why nMOS is selected as pull down transistor?	N/D 17
7.	What is the need of demarcation?	N/D 17
8.	Define body bias effect	N/D 16, N/D 14
9.	Draw the stick diagram and layout for CMOS inverter	N/D 16
10.	What is meant by CMOS latch-up?	A/M 16
11.	What is meant by subthreshold conduction?	
12.	What are the second order effects of MOS transistor?	
13.	Draw the IV characteristics of NMOS/PMOS transistor	
14.	State the merits and demerits of CMOS technology	
15.	Draw the fabrication view of n-well/pwell and twin tub CMOS transistor	
16.	What is meant by DIBL? State its significance.	
17.	What are guard rings? State their uses.	
18.	What are SPICE models? What are BSIM models?Write SPICE descriptions for CMOS inverter.	
19.	What is meant by full scaling or constant field scaling? What is meant by fixed voltage scaling?	
20.	Define noise margin of CMOS inverter.	

Part B

1.	Explain the dynamic behavior of MOS transistors.	A/M 18
2.	Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistors	N/D 16
3.	Explain the need for scaling. Discuss the principles of constant field and lateral scaling and analyze its effects on device characteristics	A/M 17, N/D 17, A/M 16
4.	Describe the equation for source to drain current in the three regions of operation of a MOS transistor and Draw the VI characteristics	A/M 16

5.	Explain the DC transfer characteristics of a CMOS inverter with necessary conditions for different regions of operation	A/M 17, N/D 17, A/M 16
6.	Explain the different steps involved in the n-well CMOS fabrication process with neat diagrams	N/D 16
7.	Discuss in detail the following second order effects i) Velocity saturation and mobility degradation.ii) Body effect iii) Subthreshold conduction. iv)Channel Length modulation and explain their effect on short channel transistors	N/D 13
8.	Draw the stick diagram and layout diagram of 2 input NAND gate,2 input NOR, 4 input NAND/NOR Y= (AB+C)' (16)	N/D 17, A/M 18, A/M 17
9.	Derive the noise margin of a CMOS inverter (4)	N/D 16
10.	Discuss in detail with a neat layout, the design rules for a CMOS inverter	
11.	Explain the principle of operation of NMOS transistor in all operating regions. (8)	
12.	Discuss in detail various levels of SPICE model for MOS transistors. (8)	

Unit-II: Combinational Logic Circuit

Part – A (2 Marks)

1.	Define rise delay and fall delay.	
2.	List the types of power dissipation	A/M 18, N/D 17
3.	Define Elmore constant. Give Elmore delay expression for propagation delay of an inverter.	A/M 18, A/M 17, N/D 17, A/M 16
4.	Define propagation delay of CMOS inverter.	A/M 17
5.	State the advantages of transmission gates	A/M 17
6.	What is the value of Vout for the figure	N/D 16
7.	State the components of static power consumption & dynamic power consumption.	N/D 16
8.	Draw the switch level schematic of multiplexer based nMOS latch using nMOS onle pass transistors for MUX	A/M 16
9.	Why single phase dynamic logic structure cannot be cascaded? Justify	A/M 16
10.	Draw the equivalent RC model for a 2-input NAND gate.	
11.	Why NAND implementation is preferred over NOR implementation?	
12.	What are all the problems of complementary CMOS logic as fan-in	

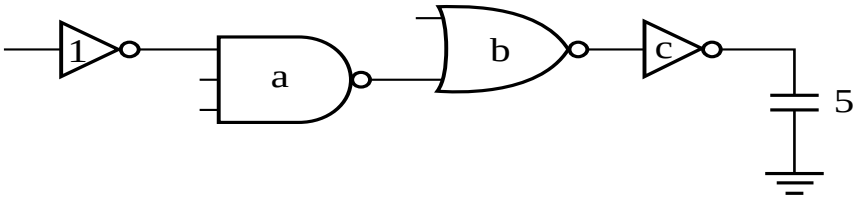
increases? What is meant by progressive transistor sizing? State its significance.

13. What is DCVSL logic? Draw its general structure.
14. What is Ratioed logic? State its merits and demerits.
15. What is pass-transistor logic? State its merits and demerits.
16. What is domino logic? State the properties of domino logic.
17. What is charge leakage and charge sharing?
18. Implement 2-to-1 multiplexer using transmission gate logic.
19. Implement 2-input XOR gate using transmission gate logic.
20. What is transmission gate logic? State its merits and demerits.
21. What is the impact of device sizing on power consumption?
22. What is meant by electrical effort/ logical effort/ gate effort/ branching effort?
23. What is input reordering? State its significance.
24. What is logic restructuring? State its significance.
25. What is clock gating

Part B

1.	Discuss in detail the performance of pass-transistor and transmission gate logic.	A/M 18
2.	What is dynamic logic? What are precharge and evaluation phases? Discuss in detail various signal integrity issues in dynamic logic.	A/M 18, A/M 16
3.	Explain with an example, the operation of domino logic gate.	N/D 17, A/M 16
4.	Compare performance of combinational CMOS digital circuits with regard to area,speed, and power.	A/M 16
5.	Discuss in detail the sources of power dissipation in CMOS circuits with neat diagrams and circuits	A/M 18, A/M 17, N/D 16
6.	Explain about DCVSL logic with suitable example(10)	A/M 17, N/D 13
7.	Write short notes on i)Ratioed Circuits ii)Dynamic CMOS circuits	N/D 16
8.	What is transmission gate? Explain the use of transmission gate	A/M 17, N/D 17
9.	Explain in detail various low power design techniques for combinational logic.	N/D 17
10.	Draw the CMOS logic circuit of the Boolean expression Z = {A(B+C)+DE}' and explain	A/M 18, N/D 17
11.	Estimate the minimum delay of the pth from A to B as shown in figure and Determine the input capacitance to achieve this delay.	A/M 18 (part C) , N/D 16

The initial inverter may present a load of 1C on the input and output load is equivalent to 5C?



12. Design a four input NAND gate and obtain its delay during the transition from high to low — A/M 18 (part C)

Unit-III: Sequential Logic Circuit

Part – A (2 Marks)

1. Compare and contrast synchronous and asynchronous sequential logic circuits? — A/M 17
2. Compare latches with registers(flip-flops). — A/M 18
3. What is meant by pipelining? — A/M 17, N/D 16
4. Draw the schematic of dynamic edge-triggered register. — N/D 16
5. What is Clocked-CMOS register? — A/M 16
6. What is NORA-CMOS? — N/D 17
7. Define clock skew — A/M 18
8. Define clock jitter — N/D 17
9. Define setup time& hold time.
10. Define contamination delay.
11. Compare static memory element with dynamic memory element.
12. What are positive latch and negative latch?
13. What is finite state machine? State its types.
14. What is Moore FSM, Mealy FSM?
15. How do you generate non-overlapping clock signals?
16. What is transition-triggered one-shot.
17. Draw the switch level schematic of CMOS clocked SR flip-flop.
18. What is meant by metastability?

Part – B (8/16 Marks)

1. Discuss about CMOS register concept and Explain the operation of master-slave based edge triggered register. Explain its operation in overlapping periods. — A/M 18, A/M 16
2. Draw and explain the operation of conventional, pulsed and resettable latches(8) — A/M 17

3.	Explain timing issues and pipelining(16)	A/M 17
4.	Explain the operation of SR flip-flops.	A/M 16
5.	Explain the operation of True Single-Phase Clocked Register (TSPCR).(8)	A/M 17, N/D 16
6.	Discuss in detail various static latches and registers	N/D 16
7.	Write short notes on NORA-CMOS Latches	N/D 16
8.	Discuss in detail about the design of sequential circuits and various pipelining approaches to optimize sequential circuits(16)	N/D 17, N/D 13
9.	Explain the timing basics and clocking distribution strategy in synchronous design in detail.(16)	N/D 17,
10.	Explain in detail various low power design techniques for sequential logic.	
11.	Explain memory architecture and its control circuits in detail	A/M 18
12.	Design a clock distribution based on a H tree model for 16 nodes	A/M 18 (part C)

Unit-IV: Design of Arithmetic Building Blocks

Part – A (2 Marks)

1.	What is datapath of the processor? State its functions List out the components of datapath.	A/M 17
2.	What is bit-sliced datapath?	A/M 16
3.	Write full adder output in terms of propagate and generate	A/M 18
4.	Draw the structure of 4x4 barrel shifter	A/M 18
5.	Give an application of high speed adder	A/M 17
6.	What is latency?	N/D 17
7.	How to design a high speed adder? Write the principle of any one fast multiplier	N/D 17, N/D 16
8.	Why barrel shifter is very useful in designing of arithmetic circuits	N/D 16
9.	Derive the Boolean equation for half adder and draw the gate level schematic.	
10.	What is propagation delay of ripple carry adder?	
11.	What is propagation delay of ripple carry adder?	
12.	What is mirror adder?	
13.	What is logarithmic look-ahead adder?	
14.	Determine propagation delay of n-bit carry select adder.	
15.	What is carry select adder?	

16. Determine propagation delay of n-bit carry bypass adder.
17. What is carry bypass adder?
18. Determine propagation delay of n-bit Manchester carry chain in dynamic logic.
19. What are Manchester carry gates?

Part – B (8/16 Marks)

1.	Explain in detail the operation of 4-bit ripple carry adder. How the drawbacks of RCA are overcome by CLA adder(16)	N/D 17
2.	Explain in detail the operation of 4-bit carry look-ahead adder and discuss its types. (10) Discuss the details of area and speed trade off(6)	A/M 18, A/M 17,
3.	Explain in detail the design of Manchester carry chain adder.	A/M 16
4.	Explain in detail the operation of 16-bit carry bypass adder	A/M 16
5.	Explain in detail the operation of 16-bit carry select adder.	N/D 16
6.	Explain in detail mirror implementation of 4-bit carry look-ahead adder.	A/M 18, N/D 13
7.	Explain the concept of modified Booth multiplier with suitable example(16)	A/M 17, N/D 17
8.	Design a multiplier for 5 bit by 3 bit. Explain its operation and summarise the number of adders. Discuss it over Wallace multiplier(16)	A/M 18, N/D 17
9.	Explain the concept of Booth multiplier with suitable example. Justify how it speeds up the process (16)	N/D 16
10.	Explain in detail the operation of 4-bit adder. Describe the different approaches of improving the speed of the adder.(116)	N/D 16

Unit-V: Implementation Strategies

Part – A (2 Marks)

1.	What is System on Chip (SoC)? Give an example.	
2.	What is meant by design automation? State its merits and demerits	
3.	What is meant by CBIC?	A/M 17
4.	Name the elements in a configuration logic block	A/M 17
5.	What are feed-through cells? State their uses.	A/M 16
6.	State the features of full custom design	A/M 16
7.	What is logic synthesis?	
8.	What is an antifuse? State its merits and demerits.	N/D 16

9.	What is placement? State its goals and objectives.	
10.	What is extraction? State its types.	
11.	What is routing? State its types and objectives.	N/D 17
12.	What is ULSI	N/D 17
13.	What is standard cell based ASIC design? State the merits and demerits of standard cell based design	N/D 16
14.	What is programmable interconnect? State its merits and demerits.	
15.	What are compiled cells? State the merits and demerits of compiled cells.	
16.	Differentiate PLA, PAL and PROM	
17.	What are SPLDs? State its types.	
18.	What is CPLD? State its features. Compare features of CPLD with FPGA.	
19.	What is clock routing? Wht are the two different types of routing	A/M 18
20.	What is the role of cell libraries in ASIC design	A/M 18

Part B

1.	Explain in detail full custom design, and standard cell based design.	A/M 18
2.	Write short notes on routing procedures involved in FPGA interconnect(6)	A/M 17
3.	Explain in detail semicustom ASIC with its classification & design flow.	N/D 16, A/M 16
4.	Explain in detail ASIC design flow	
5.	Explain in detail different types of programmable interconnect.Explain in detail programmable interconnect,	
6.	Explain in detail the functions of Xilinx XC4000 IOB.	
7.	Draw and Discuss in detail the building blocks of FPGA and its programming technologies (10)	A/M 18, A/M 17, N/D 17, N/D 16
8.	Discuss in detail various implementation strategies of digital integrated circuits.	
9.	Discuss in detail various ASIC with neat diagram(16)	A/M 18, A/M 17, N/D 17