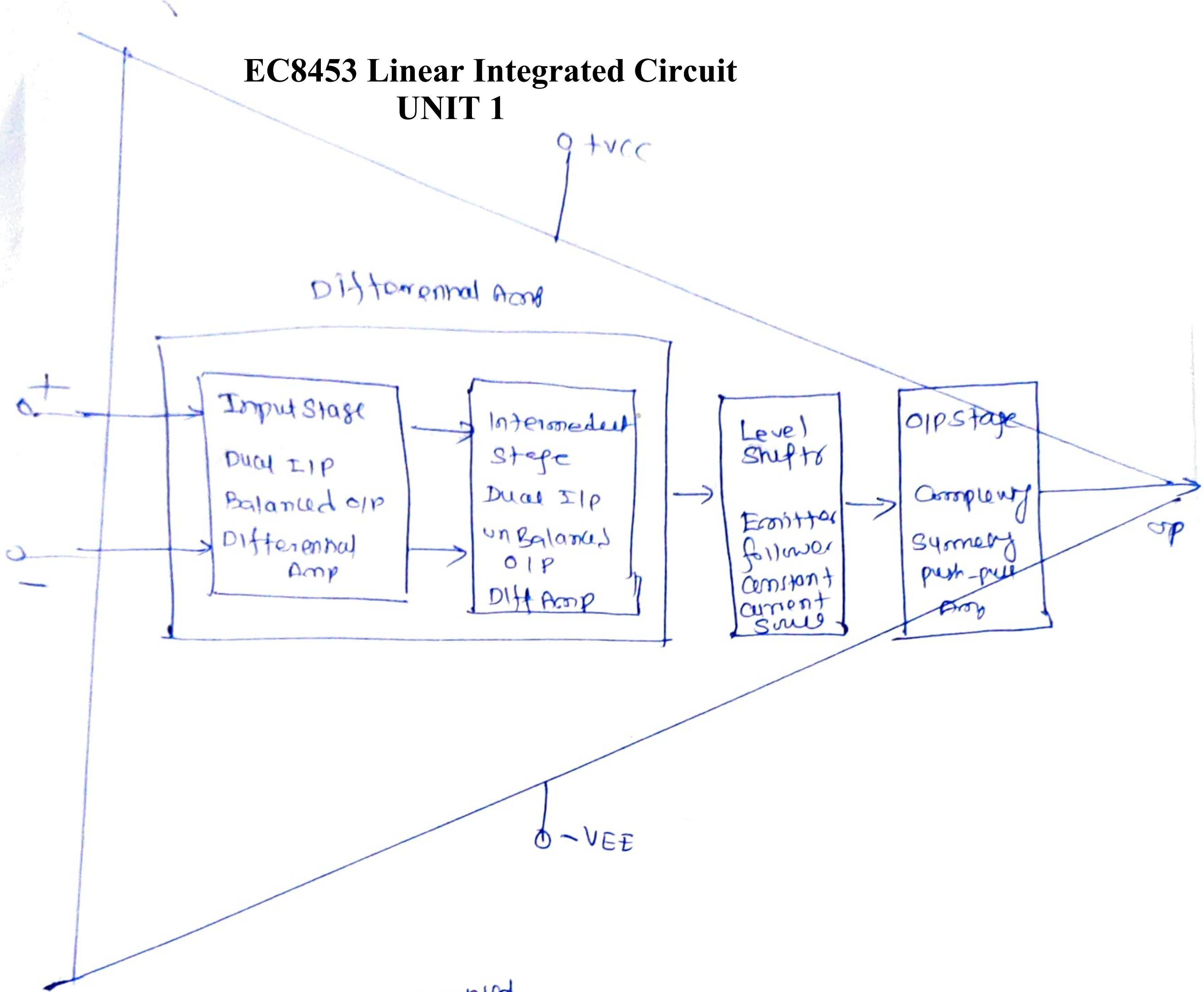
EC8453 Linear Integrated Circuit
UNIT 1



Multi stage direct coupled high gain negative feed back amplifier

The main use of opamp to amplify ac and DC I/p signal

Initially used for Mathematical operations

Now a days, its applications varies

Here Direct coupling is used which makes the DC voltage at o/p of intermediate stage above ground potential.

Therefore DC level at o/p stage must be shifted to ground ie down to 0 voltage with respect to ground

Emitter follower act as level shifter

push pull amp increase the o/p voltage swing and increase the current supplying capability of amp

Characteristics of opAmp

High I/P impedance > 100kΩ

Low o/p impedance < 100 Ω

Amplifies signal with frequency range 0Hz to 1MHz

Low offset voltage and current

Very High voltage gain - about 2,00 000

[Real values about 20,000 to 200000)

Que:
What is the difference between Digital IC and Linear IC?

Digital IC: Digital IC's are complete functioning of logic circuits that are equivalents of basic transistor logic circuits.

→ They are used to form such circuit as gates, counters, multiplexers, shift registers and others. It is a pre designed package, it is usually requires nothing more than a power supply, I/P and O/P.

→ Digital circuits are concerned with only two levels of voltage or current 'high or low'. Therefore, accurate control of operating-region characteristics are not required in digital circuits, so easy to design and low cost.

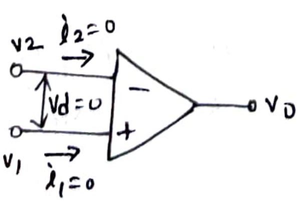
Linear IC: are equivalents of discrete transistor networks such as amps, filters, frequency multipliers and modulators, that often aditional components are required for satisfactory operation.

→ o/p electrical signals vary in proportion to the I/P signal applied.

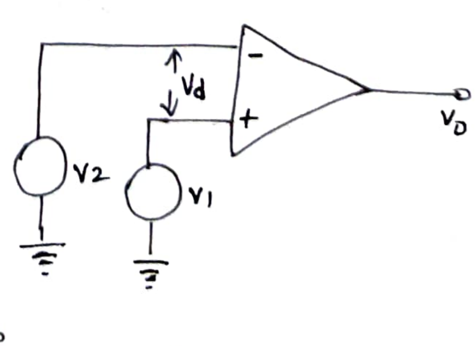
The Ideal operational Amplifier

[Que: Draw the Ideal opamp and List the ideal characteristics of opamp]

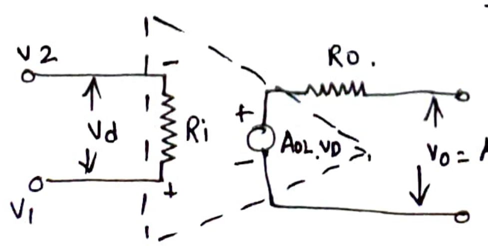
(a) Symbol



(c) open Loop circuit



(b) Equivalent circuit.



$$V_0 = A_{OL}\, V_d$$
$$= A_{OL}(V_1 - V_2)$$

it shows that the opamp amplifies difference between the two I/P voltages.

if $V_1 = 0$, output V_o is 180° out of phase with I/p signal V_2.

,

$V_2 = 0$, output V_o will be in phase with the input signal applied at V_1

Electrical characteristics

1) open loop voltage gain $A_{OL} = \infty$

2) I/P impedance $R_i = \infty$ [so that almost any signal source can drive it and there is no loading of preceding stage]

3) Band width $BW = \infty$ [so that any frequency signal from 0 to ∞ Hz can be amplified without any attenuation]

4) o/p impedance $R_o = 0$ [so that o/p can drive an infinite no of other devices]

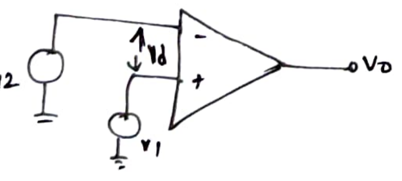
5) Zero offset ie $V_o = 0$ when $V_1 = V_2 = 0$

6) Infinite common-mode rejection ratio so that the o/p common-mode noise voltage is zero

7) Infinite slew rate so that the o/p voltage changes occur simultaneously with I/p voltage changes

open loop operation of opamp

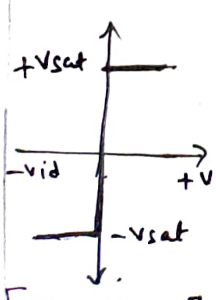
[o/p signal is not fed back in any form as part of I/p terminals]



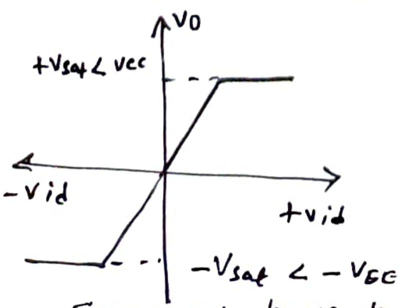
→ Since the gain is ∞

→ o/p voltage is either at its positive saturation voltage (or) -ve saturation voltage ($-V_{sat}$) as $V_1 > V_2$ or $V_2 > V_1$ respectively.

The o/p assumes one of the two possible o/p states, ie $+V_{sat}$ or $-V_{sat}$ and the amplifier act as switch only.



[Scale Value]



[curve not drawn to scale]

ideal voltage transfer curve. (keeping gain constant)

→ o/p voltage is directly proportional to the input difference voltage only until it reaches the saturation voltages and that thereafter output voltage remains constant

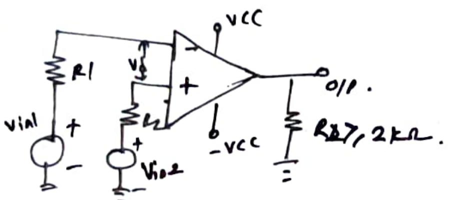
→ ideal voltage transfer curve, ideal because o/p offset voltage is assumed to be zero

[NOTE: In practical o/p o/p offset voltage is near to zero and it ignored for simplicity for calculations]

NOTE

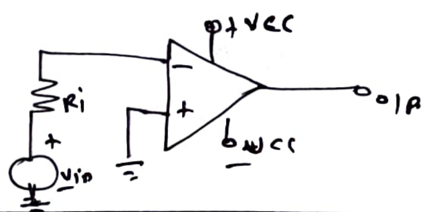
When connected in open-loop configuration, the opamp simply function as a high-gain amplifier. There are three open loop configuration.

1. Differential amplifier ⇒ o/p $v_o = A\,(V_{in1} - V_{in2})$.
2. Inverting amplifier ⇒ o/p $v_o = -A\,v_{in}$
3. Non-inverting amplifier ⇒ o/p $v_o = A \cdot v_{in}$.

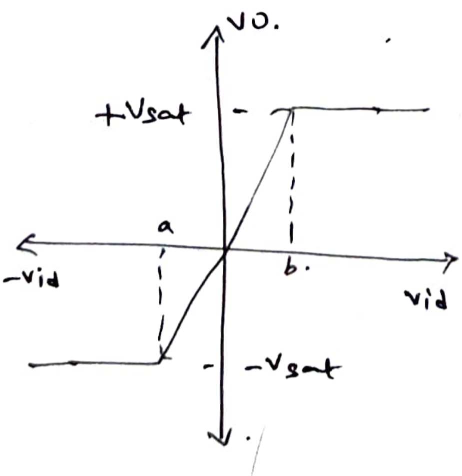


Differential amp (openloop)

Inverting Amplifier



Explain why openloop configuration is not used in linear applications.



→ Since open loop gain is ∞ o/p voltage either +Vsat, V1 > V2 or −Vsat, V2 > V1 respectively.

→ if small noise voltage present at I/p get amplified by the amplifier due to high open loop gain.

→ From graph, only small I/p only it behave as linear

it shows the inability of op-amp to work as a linear small signal amplifier in the open loop mode.

Problem: [open loop]

Determine the o/p voltage for the inverting amp.

V_{in} = 20mv dc , V_{in} = −50 μV peak sine wave , opamp: 741

A: 200,000 , R_i = 2MΩ , R_o = 75Ω , $+V_{CC}$ = +15V , $-V_{EE}$ = −15V.
and o/p swing = ±14v.

V_{in} = 20mvdc

For inverting amp $\boxed{V_o = -A V_{in}}$ = $-(2)(10^5)(20)(10^{-3})$ = −4000V.

This is the Theoritical value, the actual value will be a negative saturation voltge.

$\boxed{V_{in} \; V_o = -A V_{in}}$ = $-2(10^5)(-50)(10^{-6})$ = 10v peak sinewave.

This o/p less than o/p voltage swing.

Feed Back in ideal opamp

By connecting external components around an op-Amp, we create a feed back circuit.

The component Name is Called	:	Feed Back Resistance R_f. [Feed back Network]
Type of Feed Back	:	Negative Feed Back
o/p	:	Not driven into saturation and the circuit behaves in a Linear manner

Assumptions:

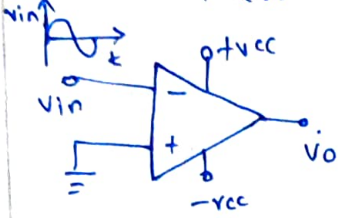
1) The current drawn by either of the input terminals (Non-INV and Inv. I/p terminals negligible.

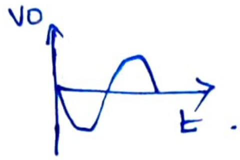
2) The differential I/P voltage V_d between non-inverting and inverting input terminals is essentially zero.

The inverting Amplifier:

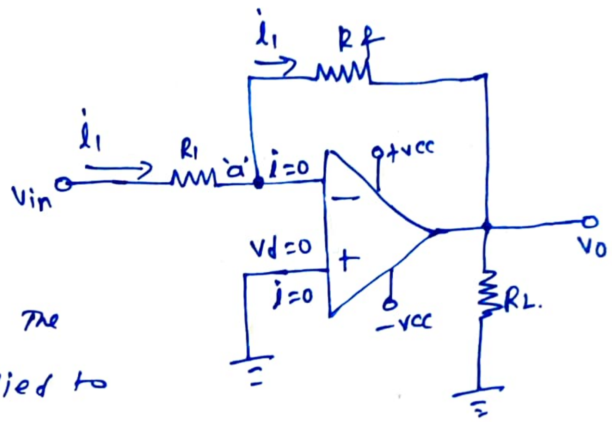
The I/P is applied at the inverting input terminal, the opamp is called as inverting Amplifier.

The o/p ~~is~~ and i/p is antiphase ie 180° phase difference between them.





Circuit Diagram:



The o/p Voltage V_o is fed back to the inverting input terminals through the $R_f - R_1$ network where R_f is the feed back resistor. The input signal V_i (ac or dc) is applied to the inverting I/P through R_1 and non inverting input terminals of op-amp is grounded.

Analysis: Assume an ideal-opamp, As $V_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$\boxed{i_1 = \frac{V_i}{R_1}}$$

Also since opAmp draws no current, all the current flowing through R_1 must flow through R_f. The o/p voltage

$$V_o = -i_1 R_f = -\left(\frac{V_i}{R_1}\right) R_f.$$

Hence, gain of Amp is Closed loop gain is

$$A_{CL} = \frac{V_o}{V_i} = \frac{-\left(\frac{V_i}{R_1}\right) R_f}{V_i} = \left(-\frac{V_i}{R_1}\right) R_f \times \frac{1}{V_i}$$

$$\boxed{A_{CL} = -\frac{Z_f}{Z_1}} \qquad A_{CL} = \boxed{-\frac{R_f}{R_1}} \text{ for idle opAmp.}$$

'−' sign indicates a phase shift of 180° between V_i and V_o.

Also since inverting I/P terminal is at virtual ground, the effect I/P impedance is R_1, it should be large to avoid Loading effect.

The closed Loop gain $\boxed{A_{CL} = -\frac{R_f}{R_1}}$ for ideal Cause.

For a pratical opamp, the expression for the closed loop gain should be calculated using a Low frequency model

For pratical opAmp where $A_{OL} \neq \infty$, $R_i \neq \infty$ and $R_o \neq 0$, The opAmp is a voltage Controlled Source and $A_{OL} V_d$ is equivalent Thevenin voltage Source and R_o is the Thevenin equivalent Resistance.

Analysis: Let we know equivalent circuit of an op-amp is

usually

$R_i > R_1$, so assume

$V_{eq} = v_i$ and $R_{eq} = R_1$

Equivalent circuit

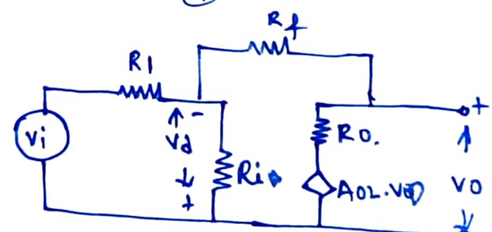
(a)

From Fig(b) output loop

$$V_o = iR_o + A_{OL} V_d \quad — ①$$

Also $$V_d + iR_f + V_o = 0 \quad — ②$$

$$V_d = -(V_o + iR_f) \quad — ③$$



(b) Equivalent ck of pratical opamp inverting amplifier.

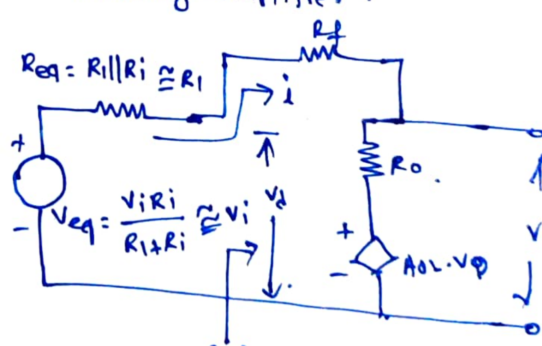
Sub ③ in ①

$$V_o = iR_o + A_{OL}\left[-(V_o + iR_f)\right]$$

$$V_o = iR_o - A_{OL} V_o - iR_f A_{OL}$$

$$V_o + A_{OL} V_o = i(R_o - R_f A_{OL})$$

$$\boxed{\frac{V_o + A_{OL} V_o}{(R_o - R_f A_{OL})} = i} \quad — ④$$



(c) Simplified ckt using Thevenin equivalent

Also the KVL loop equation gives

$$V_i = i(R_1 + R_f) + V_o \quad — ⑤$$

'Sub' (4) in (5)

$$V_i = \frac{V_o + A_{OL} V_o}{(R_o - R_f A_{OL})} \cdot (R_1 + R_f) + V_o$$

Multiply $(R_o - R_f A_{OL})$.

$$V_i (R_o - R_f A_{OL}) = \frac{V_o + A_{OL} V_o}{\cancel{(R_o - R_f A_{OL})}} (R_f + R_1) \cancel{(R_o - R_f A_{OL})} + V_o (R_o - R_f A_{OL})$$

$$V_i (R_o - R_f A_{OL}) = V_o + A_{OL} V_o (R_f + R_1) + V_o (R_o - R_f A_{OL})$$

$$= V_o [1 + A_{OL} (R_f + R_1)] + (R_o - R_f A_{OL})$$

$$= V_o [(R_1 + R_f)(1 + A_{OL})] + (R_o - R_f A_{OL})]$$

$$= V_o [R_1 + R_f + R_1 A_{OL} + \cancel{R_f A_{OL}} + R_o - \cancel{R_f A_{OL}}]$$

$$= V_o [R_o + R_f + R_1 (1 + A_{OL})]$$

$$V_i (R_o - R_f A_{OL}) = V_o [R_o + R_f + R_1 (1 + A_{OL})]$$

$$\boxed{A_{CL} = \frac{V_o}{V_i} = \frac{R_o - R_f A_{OL}}{R_o + R_f + R_1 (1 + A_{OL})}}$$

closed loop gain of pratical opamp in for inverting amplifier.

$A_{OL} >> 1$ and $A_{OL} R_1 >> R_o + R_f$ and negleting R_o.

$$\boxed{A_{CL} = \frac{-R_f}{R_1}}$$

I/P Resistance:

$$R_{if} = \frac{V_d}{i}$$

From loop equations $V_d + i(R_f + R_o) + A_{OL} V_d = 0$

$$V_d[1 + A_{OL}] + i[R_f + R_o] = 0$$

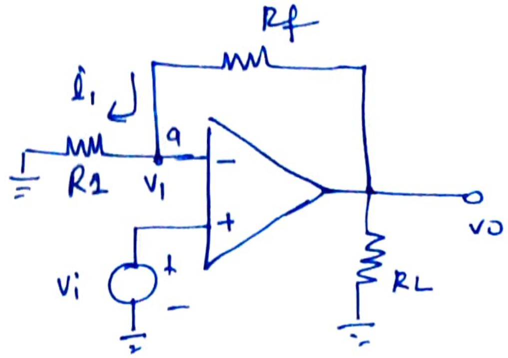
$$V_d \cdot (1 + A_{OL}) = -i(R_f + R_o)$$

$$\boxed{\frac{V_d}{i} = \frac{R_o + R_f}{1 + A_{OL}}}$$

O/P Resistance:

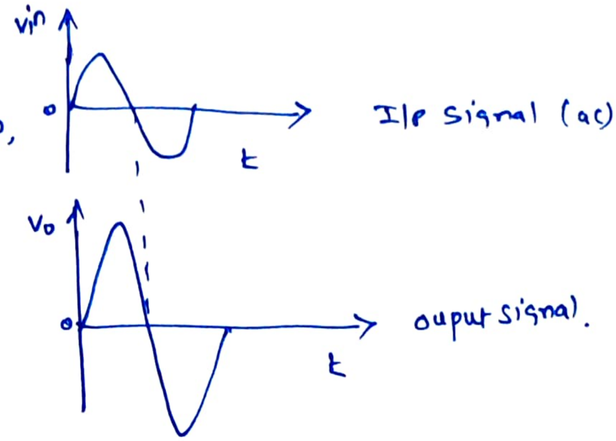
The NON inverting Amplifier

The input Vin is applied to the Non inverting terminal. This circuit gives o/p inphase with the I/p signal.



Vin is either ac or dc.

As the differential voltage Vd at the I/p terminal of op-amp is Zero, the voltage at node 'a' is v_i, same as I/p voltage at non inverting terminal.



Rf and R_1 forms a potential Divider. Hence

$$V_i = \frac{Vo}{R_1 + Rf} R_1 ,$$

as no current flows into the op-amp

$$\frac{Vo}{Vi} = \frac{R_1 + Rf}{R_1} = 1 + \frac{Rf}{R_1}$$

voltage gain $\frac{Vo}{Vi} = \boxed{A_{CL} = 1 + \frac{Rf}{R_1}}$

→ gain can be adjusted to unity or more, by proper selection of resistors Rf and R_1

Also

$$Vo = \left(1 + \frac{Rf}{R_1}\right) Vi$$

$$i_L = \frac{Vo}{RL}$$

$$i_1 = \frac{vi}{R_1}$$

Total current

$$i_o = i_1 + i_L$$

Problem:

① Design an amplifier with a gain of -10 and I/P Resistance equal to $10k\Omega$

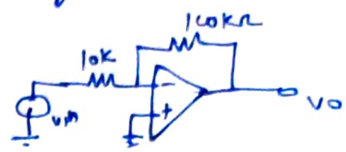
Solution: If gain given in Negative, so inverting amplifier has to be design.

$$A_{CL} = \frac{-R_f}{R_1}$$

$R_1 = 10k\Omega$

$R_f = -A_{CL}R_1$

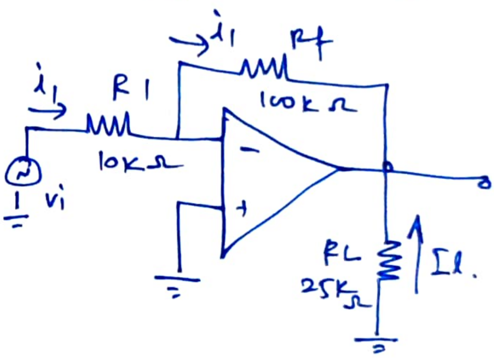
$A_{CL} = 10$



$$R_f = -10 \times 10k\Omega = 100k\Omega$$

② For an inverting amplifier, $R_1 = 10k\Omega$, $R_f = 100k\Omega$, $V_i = 1V$, $R_L = 25K$. Calculate (i) i_1 (ii) V_o (iii) I_L and i_o.

(i) $$i_1 = \frac{V_i}{R_1} = \frac{1V}{10k\Omega} = 0.1mA$$



② $$V_o = -\frac{R_f}{R_1} \cdot V_i = -\frac{100k\Omega}{10k\Omega} \cdot 1V$$

$$= -10V.$$

③. $$i_L = \frac{V_o}{R_L} = \frac{10}{25K} = 0.4mA$$

④ i_o total current $= i_1 + i_L = 0.1mA + 0.4mA = 0.5mA.$

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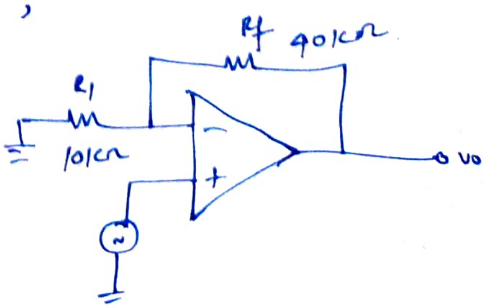
③ Design an amplifier with gain of $+5$ using op amp, $R_1 = 10k$

for Non inverting $\quad A_{CL} = 1 + \frac{R_f}{R_1}$

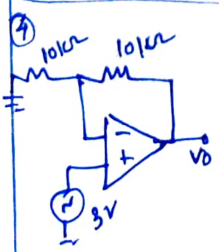
$$5 = 1 + \frac{R_f}{R_1}$$

$$5 = 1 + \frac{R_f}{10k}, \quad 5 - 1 = \frac{R_f}{10k}, \quad 4 \times 10k\Omega = R_f.$$

$$R_f = 4 \times 10k\Omega = 40k\Omega$$



④ Find Vo



$$A_F = 1 + \frac{R_f}{R_1} = 1 + \frac{10k}{10k}$$

$$= 2$$

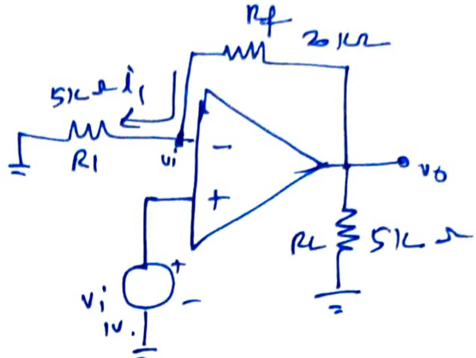
$$A_F = \frac{V_o}{V_{in}}$$

$V_o = A_F \cdot V_{in}$

$V_o = 2 \times 3V = 6V.$

(4) $R_1 = 5k\Omega$, $R_f = 20k\Omega$, $v_i = 1V$, $R_L = 5k\Omega$

Calculate V_o, A_{CL}, i_L and i_o.



(1) $V_o = \left(1+\frac{R_f}{R_1}\right) v_i = \left(1+\frac{20k\Omega}{5k\Omega}\right) 1V = 5V$

(2) $A_{CL} = \frac{V_o}{V_i} = \frac{5V}{1V} = 5$.

(3) $i_L = \frac{V_o}{R_L} = \frac{5}{5k\Omega} = 1mA$

(4) $i_1 = \frac{V_i}{R_1} = \frac{V_o - V_i}{R_f} = \frac{5V - 1V}{20k} = \frac{4}{20k} = 0.2mA$.

(5) $i_o = i_1 + i_L = 1mA + 0.2mA = 1.2mA$.

Voltage Follower: Que [Define voltage follower (or) Explain voltage follower. (or) Non Inverting Buffer.

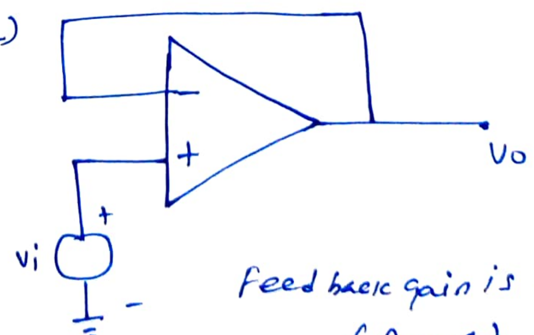
Let we know $\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$ if $R_f = 0$ and $R_1 = \infty$, the circuit becomes.

$\boxed{V_o = V_i}$ ie, the output voltage is equal to I/P voltage, both in magnitude and phase. otherwise o/p voltage follows the I/P voltage. Hence this circuit called voltage follower

I/P impedance is very high (MΩ)

O/P impedance is zero

Therefore, it draws negligible current from the source



Feed back gain is 1 ($A_F = 1$)

Use:

Used as buffer for impedance matching, ie, to connect a high impedance source to a low impedance load.

Formulas:

$A_F = 1$, $R_{iF} = AR_i$, $R_{oF} = \frac{R_o}{A}$, $f_F = Af_o$

$V_{OOT} = \frac{\pm V_{sat}}{A}$

• Differential amplifier:

[Que: Draw the differential amplifier and Drive an expression for Common mode Rejection ratio]

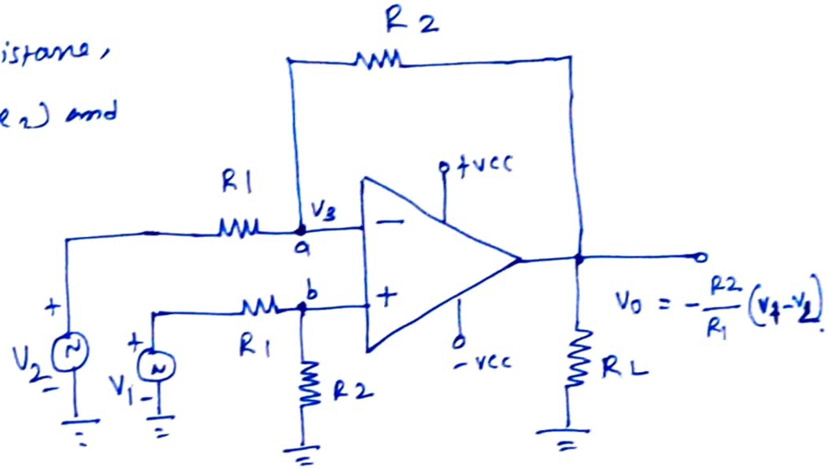
Definition: A circuit that amplifies the difference between two input signals is called a difference (or) differential amplifier.

Use: Used in instrumentation circuits and Industrial applications.

Significance: Importance of differential amplifier is better able to reject common mode (noise) voltage than single I/P circuit &

Circuit consist of I/P resistance, feedback resistance (R_2) and Load Resistance R_L.

I/P are V_2 and V_1



Since, the differential voltage at the I/P terminals of the op-amp is zero, nodes 'a' and 'b' are at same potential, designated as V_3

The nodal equation at 'a' $\quad \frac{V_3 - V_2}{R_1} + \frac{V_3 - V_o}{R_2} = 0 \quad$ —① $\quad \frac{V_3}{R_1} - \frac{V_2}{R_1} + \frac{V_3}{R_2} - \frac{V_o}{R_2} = 0$

" 'b' $\quad \frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0 \quad$ —②

Rearrange the equations ① and ②

$$\left[\frac{1}{R_1} + \frac{1}{R_2}\right] V_3 - \frac{V_2}{R_1} = \frac{V_o}{R_2} \quad \text{—③}$$

$$\left[\frac{1}{R_1} + \frac{1}{R_2}\right] V_3 - \frac{V_1}{R_1} = 0 \quad \text{—④}$$

Sub ③ – ④ $\quad \left[\left(\frac{1}{R_1} + \frac{1}{R_2}\right) V_3 - \frac{V_2}{R_1}\right] - \left[\left(\frac{1}{R_1} + \frac{1}{R_2}\right) V_3 - \frac{V_1}{R_1}\right] = \frac{V_o}{R_2}$

$$\left(\frac{1}{R_1} + \cancel{\frac{1}{R_2}}\right) V_3 - \frac{V_2}{R_1} - \left(\frac{1}{R_1} + \cancel{\frac{1}{R_2}}\right) V_3 + \frac{V_1}{R_1} = \frac{V_o}{R_2}$$

$$\frac{1}{R_1}[V_1 - V_2] = \frac{V_o}{R_2} \qquad \boxed{V_o = \frac{R_2}{R_1}[V_1 - V_2]}$$

$$V_0 = \frac{R_2}{R_1}[V_1 - V_2]$$

voltage Gain $\boxed{A_D = \frac{V_0}{V_1 - V_2} = \frac{R_2}{R_1}}$

Conclusion:

These circuit useful for detecting very small difference in signals. since the gain R_2/R_1 can be chosen to be very large.

For examble, if $R_2 = 100R_1$, then the small difference $V_1 - V_2$ is amplified 100 times.

Difference mode and Common mode gains

Let $V_0 = \frac{R_2}{R_1}[V_1 - V_2]$, if $V_1 = V_2$, the o/p $V_0 = 0$ for ideal op-amp only.

But pratical op-amp, $V_1 = V_2$, we wont get $V_0 = 0$ due to common mode component of I/p signal (voltage)

For examble: V_0 will have different value

Case (i) $V_1 = 100\mu V$, $V_2 = 50\mu V$.

(ii) $V_1 = 1000\mu V$, $V_2 = 950\mu V$.

In Both the causes difference $[V_1 - V_2] = 50\mu V$ But output is different, due to average voltage of I/p signals. that is called Common mode signal.

$$V_{cm} = \frac{V_1 + V_2}{2}$$

$\frac{150}{2} = 75$

$\frac{1950}{2} = 975$

Note: (Important)

For the differential amp,

if $V_1 = V_2$, but voltage at node 'a' and 'b' are different because I/p Resistance at from V_2 source is $\cong R_1$ and from V_1 source is $\simeq (R_2 + R_3)$. The voltage at the positive terminal slightely grater than negative terminal. So out is Not zero

∴ The o/p. therefore must be expressed as

$$\boxed{V_0 = A_1 V_1 + A_2 V_2} \quad \text{--- (1)}$$

Where A_1 is gain when V_1 is applied, $V_2 = 0$

A_2 " " V_2 is applied, $V_1 = 0$.

$$V_{cm} = \frac{V_1 + V_2}{2}, \quad V_d = (V_1 - V_2)$$

I/p Resistance by V_2 is R_1

" by V_1 is $R_1 + R_2$

Variable gain is achieved by varying pot at load.

find V_1

Add (2) and (3)

$$2V_{cm} = V_1 + \cancel{V_2} \quad \text{--- (2)}$$

$$V_d = V_1 - \cancel{V_2} \quad \text{--- (3)}$$

$$2V_{cm} + V_d = 2V_1$$

$$\boxed{V_{cm} + \frac{V_d}{2} = V_1} \quad \text{--- (4)}$$

sub (4) in (3)

$$V_d = V_{cm} + \frac{V_d}{2} - V_2.$$

$$V_2 = V_{cm} + \frac{V_d}{2} - V_d$$

$$\boxed{V_2 = \left[V_{cm} - \frac{V_d}{2}\right]} \quad \text{--- (5)}$$

sub (4) and (5) in (1)

$$V_0 = A_1\left[V_{cm} + \frac{V_d}{2}\right] + A_2\left[V_{cm} - \frac{V_d}{2}\right]$$

$$= A_1 V_{cm} + \frac{A_1 V_d}{2} + A_2 V_{cm} - \frac{A_2 V_d}{2}$$

$$V_0 = V_{cm}\left[A_1 + A_2\right] + V_d\left[\frac{A_1}{2} - \frac{A_2}{2}\right]$$

$$V_0 = V_{cm} \cdot A_{cm} + V_d A_{DM}$$

voltage gain. $\boxed{A_{cm} = A_1 + A_2}$, $\boxed{A_{DM} = \frac{1}{2}\left[A_1 - A_2\right]}$

Common mode Rejection Ratio (CMRR)

(a) Define CMRR)

It is defined as the ratio of difference mode signal to common mode signal is called CMRR and gives the figure of merit ρ for the differential amplifier.

So CMRR is given by

$$\boxed{\rho = \left| \frac{A_{DM}}{A_{CM}} \right|} \quad \text{in dB}$$

$\mu A741$ minimum CMRR 70dB.

$\mu A725A$ is 120dB.

For ideal opamp A_{DM}, A_{CM} is should be zero.

So the higher value of CMRR, better is the op-amp

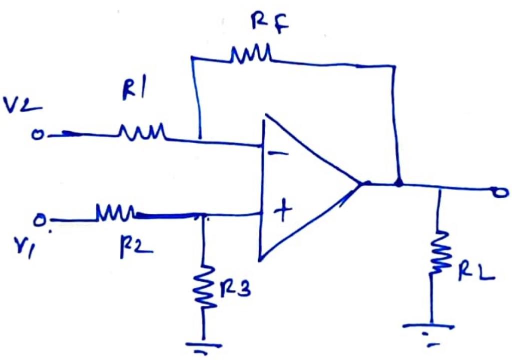
For practical amp CMRR in dB = $20 \log \left| \frac{A_D}{A_C} \right|$ dB.

Problem In circuit

$R_1 = R_2 = 1k\Omega$

$R_F = R_3 = 10k\Omega$ and

opamp is $\mu A741C$.



① What are the gain and input resistance of amplifier?

② Find V_0 if $V_2 = 2.7\,V_{pp}$

$V_1 = 3V_{pp}$ sine wave at 100Hz:

$$\text{gain } A_D = \frac{-R_f}{R_1} = -\frac{10k\Omega}{1k\Omega} = -10.$$

Resistance by source V_2 is R_1, so R_i by source $V_2 = 1k\Omega$

" V_1 is (R_3+R_1), so R_i by source $V_1 = 1k\Omega + 10k\Omega$
$= 11k\Omega$.

$$A_D = \frac{V_0}{V_1 - V_2} =$$

$$V_0 = A_D(V_1 - V_2) = -10(3 - 2.77)$$
$$=$$

Differential Amplifier [BJT differential Amplifier] (or) Emitter Coupled Differential Amp

Definition

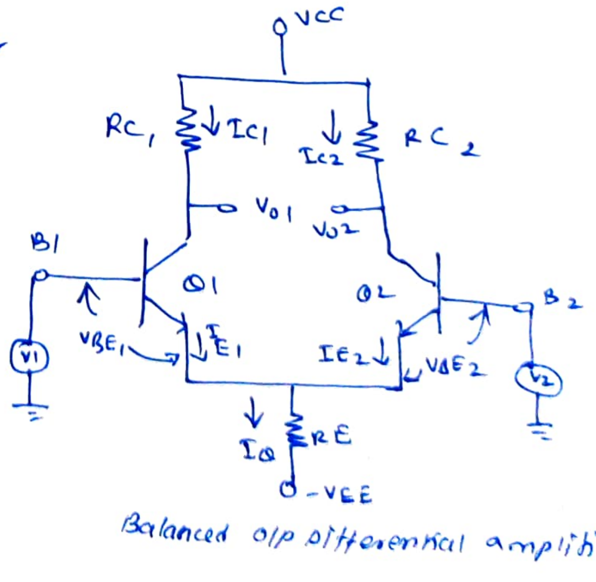
The Differential amplifier used to amplifies the difference between two Input Signals. It is designed to provide high gain and high I/P impedance. The main purpose of this amplifier is to provide high gain to the difference mode signal and Cancel the common mode signal.

Features:

1) High Differential voltage gain
2) High CMRR
3) High I/p impedance
4) Low offset voltage and currents
5) Low Common mode gain.
6) Large Bandwidth.
7) Low o/p impedance.
9) Low drift

Basic Differential Amp [principle]

1) It uses emitter Couple Configuration
2) Transister Q1 and Q2 are similler Characteristics
3) $R_{C1} = R_{C2}$
4) $R_{E1} = R_{E2}$
5) magnitude of Vcc and −VEE are same.
6) Balanced output amplifier.

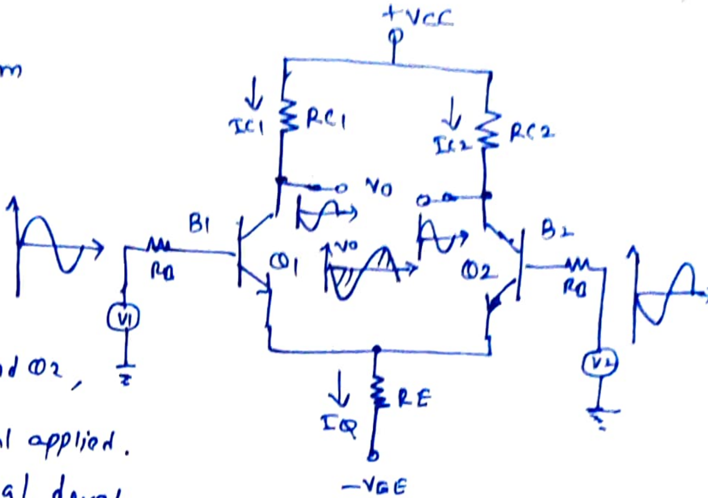


Balanced o/p Differential amplifier

It has two Input terminals, terminal B_2 is the inverting I/p terminal and B_1 is the non-inverting I/p terminal.

Modes of operation:

Differential mode of operation



1) Two I/P signals are different from each other, Same maganitude but 180° out of phase.

operation:

* I/P signals are applied at B_1 and B_2 of Transistors Q_1 and Q_2,

it works: (1) At Base 2 : +ve signal applied.
at ~~B1~~: amplified Negative going signal develops at on collector of Q_1, Due to +ve I/P, positive voltage drop across RE. ~~and~~ amplified positive ~~signal~~ develops ~~on collector~~ of ~~Q2 and it develop~~

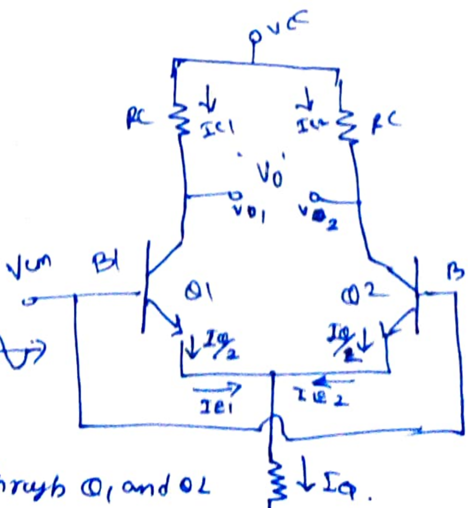
(2) At Base 2 : When Negative signal applied, amplified positive signal develops on collector of Q_2. Due to Negative I/P Negative voltage drop across RE.

So signal voltage across R_E is equal magnitude and 180° out of phase, due to symmetry of transistors, Hence these two signals are cancel each other and no signal across RE. So there is no ac signal flowing RE.

O/P : The o/p is taken at collector of both the transistors, equal magnitude but out of phase. And Vo is the difference between two signals.

eg: $10 - (-10) = 20\,V$.

Common mode operation



Base of both transistors B_1 and B_2 Joined togather and connected to a voltge Vcm called common mode voltage

$V_1 = V_2 = V_{cm}$, Q_1 and Q_2 ~~forward~~ forward Biased and matched, due to symmetry of the circuits, the current I_Q divides equaly through Q_1 and Q_2

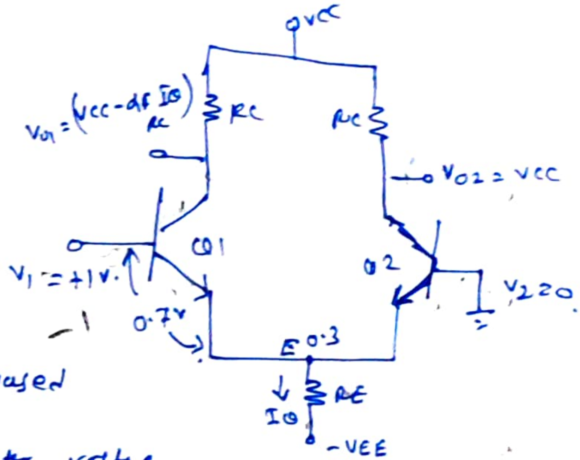
ie $I_{E1} = I_{E2} = I_Q/2$, $I_{C1} = I_{C2} = \alpha_F \frac{I_Q}{2}$, The voltage at Collectors will be $V_{CC} - \alpha_F \frac{I_Q}{2} R_C$ and therefore $V_{o1} - V_{o2} = 0$. Even if the Vcm value is Changed, voltage across Collectors will not change. So it rejects Common mode signals

Differential mode operation

if

$V_1 = 1V$, $V_2 = 0$, Q1 - ON, Q2 - OFF

The entire current flow through Q1. Since Q1 is on, the voltage at its emitter will be 0.3V.



This makes B-E junction of Q2 Reverse Biased and Q2 will remain OFF. The collector voltage of Q1 i.e V_{01} will be $(V_{CC} - \alpha_F I_0 R_C)$, $V_{02} = V_{CC}$.

Case ii) If $V_1 = -1V$, $V_2 = 0$, Q1 will be off and entire current I_0 will flow through Q2. The voltage at the common emitter point 'E' will be 0.7V which makes Q1 OFF and Q2 ON. The collector voltage will be $V_{01} = V_{CC}$, $V_{02} = V_{CC} - \alpha_F I_0 R_C$.

Conclusion:

The diff amplifier i.e pair responds only to the difference mode signals and reject common mode signals.

Differential Amplifier with Active Load

The open circuit voltage gain of an opamp should be as large as possible and this achieved by cascading gain stages. However, this increase the phase shift too and amplifier becomes more susceptible to breaking out into oscillations.

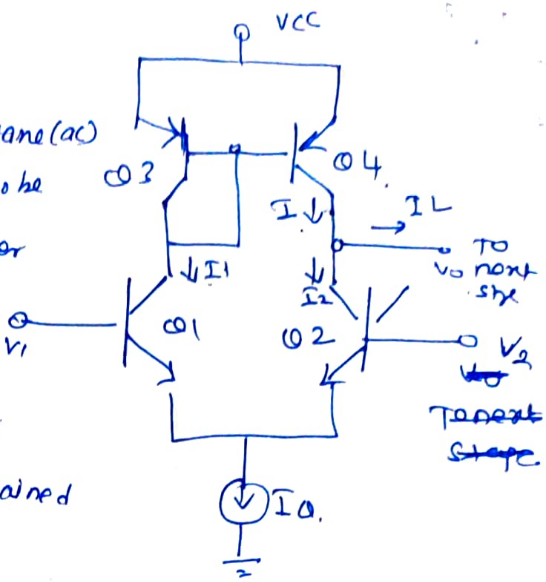
Idea to increasing gain by putting large value of RC. However, there are limitations to use of the maximum RC.

Limitations:

1. Large value of Resistance requires a large chip area.
2. For large RC, drop across RC increases and hence power supply required to maintain a given quiescent collector current.

This difficulties are circumvented by using a current ~~source~~ mirror as load in the place of RC

The current mirror when act as an ~~active Load~~ current source, its dynamic resistance (ac) is very high. Hence current mirror can also be used as an active Load. for an amplifier to obtain a very Large voltage gain.



From circuit Q3 and Q4 act as current mirror. The constant current IQ may also be obtained from a current mirror.

Under the quiescent conditions. [No signal Applied But power supply is ON]

$$V_1 = V_2 = 0.$$

Q1 and Q2 are same so $I_1 = I_2 = I_Q/2$

Where base current are assumed to be neglected.

Since Q3 and Q4 form a current mirror, $I = I_1 = I_2$

The Load current IL entering in the Next stage is

$$\boxed{I_L = I - I_2 = 0}$$

However when V_1 is increased over V_2, I_1 increases whereas I_2 decreases. Since

$$I_1 + I_2 = I_Q \text{ (constant)}.$$

Also the current I always remain equal to I_1 due to current mirror. The Load current

$$I_L = I - I_2 = I_1 - I_2$$

$$= g_m v_1 - g_m v_2 = g_m(v_1 - v_2)$$

$$\boxed{I_L = g_m V_d}$$

The circuit thus behave as transconductance Amplifier

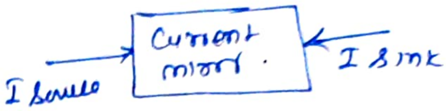
What is the purpose of using differential Amplifier with active Load?

① To provide an high voltage gain to the differential input signal and single ended o/p ie referenced to the ground is obtained.

Current mirror circuit: (Constant current source)

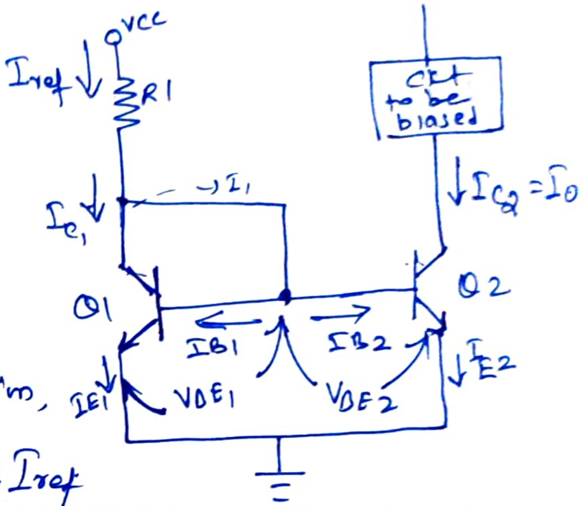
Definition: The circuit in which the o/p current forced to equal to input current is called current mirror. In a circuit, the output current is the mirror image of the input current.

→ Q_1 and Q_2 are symmetrical.



$I_{source} = I_{sink}$.

The I/p current I_{ref} flows through the diode connected transistor Q_1 and thus establishes a voltage across Q_1. This voltage in turn develop a voltage between B-E of Q_2.



I_E of $Q_2 \approx I_E$ of Q_1, which is approximately equal to I_{ref}.

As long as Q_2 maintain active region, it collector current $I_{C2} = I_0 \simeq I_{ref}$

Since the o/p current I_0 is a reflection or mirror of the reference current I_{ref}. The mirror effect is however, valid only for large values of β

Analysis:

$$I_{E1} = \alpha_F I_{ES} e^{V_{BE1}/V_T} \quad — (1)$$

$$I_{C2} = \alpha_F I_{ES} e^{V_{BE2}/V_T} \quad — (2)$$

(2)/(1) $$\frac{I_{C2}}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T}$$

Since $V_{BE1} = V_{BE2}$ we obtain

$$I_{C1} = I_{C2} = I_C = I_0$$

Also $\boxed{\beta_1 = \beta_2 = \beta}$ (Both the transistor equal)

KCL at the collector of Q_1 gives

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

$$I_{ref} = I_C + \frac{I_C}{\beta_1} + \frac{I_C}{\beta_2} \qquad \boxed{\beta_1 = \beta_2 = \beta}$$

$$I_{ref} = I_C\left[1 + \frac{2}{\beta}\right] = I_C\left[\frac{\beta + 2}{\beta}\right]$$

$$\boxed{I_C = \left[\frac{\beta}{\beta + 2}\right] I_{ref}} \quad — (3)$$

from circuit

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \simeq \frac{V_{CC}}{R_1}$$

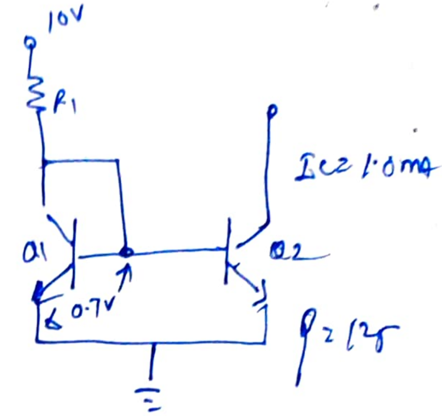
From equation (3) for $\beta \gg 1$, $\beta/\beta+2$ is almost unity

So $\boxed{I_C = 1 \cdot I_{ref}}$ for R1 constant.

Typically I_0 varies by about 3% for $50 \le \beta \le 200$

Problem in current mirror:

Que: The current mirror is to provide a 1.0mA current with VCC = 10V. Assume $\beta = 125$ and $V_{BE} = 0.7V$. Determine value of R_1



$$\boxed{\text{Let } I_C = \frac{\beta}{\beta+2} I_{ref} \qquad I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}}$$

$$= 1.0\,mA = \frac{125}{125+2} \times \frac{10V - 0.7V}{R_1}$$

$$R_1 = 9.15\,k\Omega.$$

Draw Back in Basic current mirror

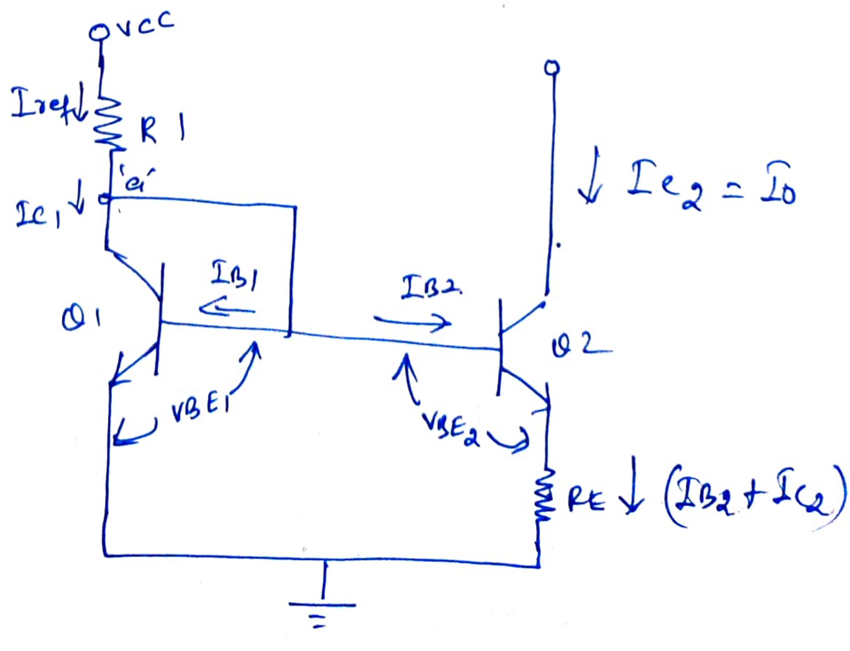
The Ratio of current o/p to I/p i.e. $\frac{I_o}{I_{ref}}$ is much depend on β, if β is low $I_o \neq I_{ref}$.

Widlar current Source:

Limitation of Basic current mirror: whenever, we need low value of current source, the value of the Resistance R_1 required sufficiently high and can not be fabricated economically in IC circuits.

This Limitation is overcome by including R_E in the Emitter Lead of Q_2. Due to R_E, $V_{BE2} < V_{BE1}$ and consequently current I_o is smaller than I_{C1}

Analysis / circuit Diagram



Analysis: (widlar current source)

Let $I_{C1} = \alpha_F I_{ES}\, e^{V_{BE1}/V_T}$, $I_{C2} = \alpha_F I_{ES}\, e^{V_{BE2}/V_T}$

Ratio
$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T} \quad \text{——— (1)}$$

Take Natural Log on both the sides

$$\ln\left[\frac{I_{C1}}{I_{C2}}\right] = \frac{V_{BE1} - V_{BE2}}{V_T}$$

$$V_T \ln\left[\frac{I_{C1}}{I_{C2}}\right] = V_{BE1} - V_{BE2} . \quad \text{——— (2)}$$

Apply KVL for the emitter loop.

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2}) R_E$$

$$V_{BE1} - V_{BE2} = (I_{B2} + I_{C2}) R_E$$

$$= I_{C2}\left(1 + \frac{I_{B2}}{I_{C2}}\right) R_E$$

$$V_{BE1} - V_{BE2} = I_{C2} R_E \left[1 + \frac{1}{\beta}\right] \quad \text{——— (3)}$$

$\beta = \frac{I_{C2}}{I_{B2}}$.

$\beta I_{B2} = I_{C2}$

$I_{B2} = \frac{I_{C2}}{\beta}$

$\left(\frac{I_{C2}}{\beta} + I_{C2}\right) R_E$

$I_{C2}\left(1 + \frac{1}{\beta}\right) R_E$

From (2) and (3)

$$I_{C2} R_E \left[1 + \frac{1}{\beta}\right] = V_T \ln\left[\frac{I_{C1}}{I_{C2}}\right]$$

$$\boxed{R_E = \frac{V_T}{\left(1 + \frac{1}{\beta}\right) I_{C2}} \ln \frac{I_{C1}}{I_{C2}}.}$$

Relation between I_{C1} and I_{ref}:

Apply KCL at node 'a' at Collector of Q_1

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

$\beta_1 = \beta_2 = \beta$.

$$I_{ref} = I_{C1}\left[1 + \frac{1}{\beta}\right) + \frac{I_{C2}}{\beta}$$

In widlar current source, $I_{C2} << I_{C1}$, therefor $\frac{I_{C2}}{\beta}$ is may be neglected.

So $I_{ref} = I_{C1}\left[1 + \frac{1}{\beta}\right]$, $\boxed{I_{C1} = \frac{\beta}{\beta+1} I_{ref}}$ $\beta >> 1$ so $\boxed{I_{C1} \cong I_{ref}}$

$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}$.

Improved current source circuits:

A good current source must meet two requirements

① o/p current I_o should not be dependent upon β.

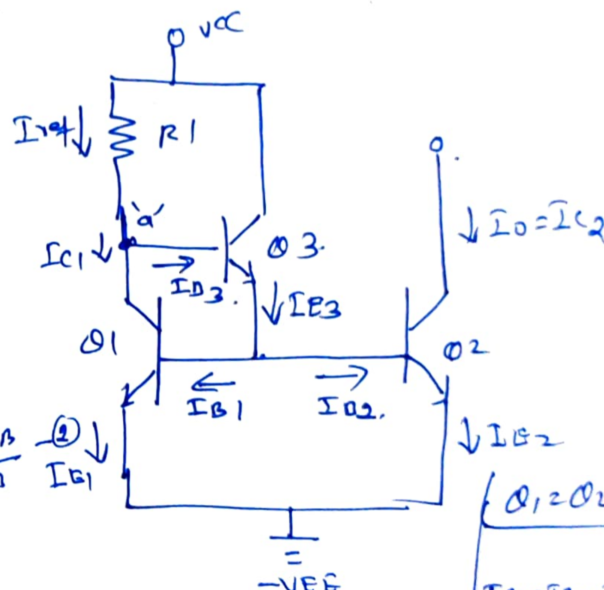
② o/p Resistance of the current source should be very high

Need for High Resistance Current Source: 'Reduce common mode gain'

Also, All differential amplifiers invariably use current source as a load. Thus to obtain high voltage gain a large o/p resistance load is required.

To Reduce dependence on β (or) increased o/p Resistance two current source is used.

① A current source with gain.



$$I_{ref} = I_{C1} + I_{B3}$$

$$= I_{C1} + \frac{I_{E3}}{1+\beta} \quad -①$$

The I_E of Q3 is

$$I_{E3} = I_{B1} + I_{B2}$$

$$I_{E3} = I_B + I_B = 2I_B \quad ②$$

$$= (1+\beta) I_{B3},$$

$$I_{B3} = \frac{2I_B}{1+\beta} \quad ②$$

Sub ② in ①

$$I_{ref} = I_{C1} + \frac{2I_B}{1+\beta}$$

$$= I_C + \frac{2I_C}{\beta(1+\beta)}$$

Take com:

$$I_C\left[1 + \frac{2}{\beta(1+\beta)}\right]$$

$$I_{ref} = I_C\left[\frac{\beta(1+\beta)+2}{\beta(1+\beta)}\right] = I_C\left[\frac{\beta+\beta^2+2}{\beta(1+\beta)}\right]$$

$$= \beta(1+\beta) I_{ref} = I_C[\beta+\beta^2+2]$$

$$\boxed{I_{ref}\left[\frac{\beta(1+\beta)}{\beta+\beta^2+2}\right] = I_C} = I_o$$

Where

$$I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1}$$

$Q_1 = Q_2$

$I_{B1} = I_{B2} = I_B$ Because Transistors are identical.

$I_B = \frac{I_C}{\beta}$

$I_{C1} = I_C$

$\boxed{I_{E3} = (1+\beta) I_{B3}}$

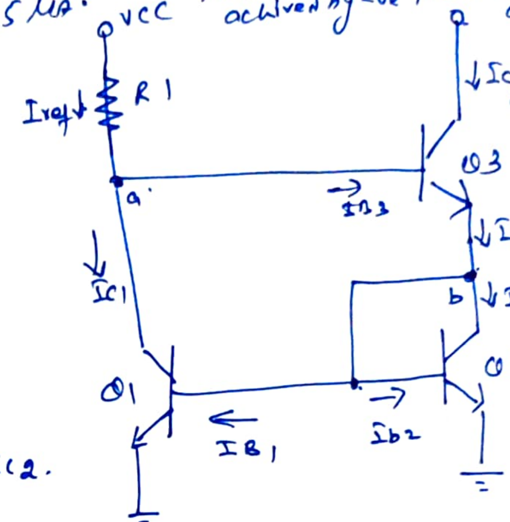
$I_{C1} = I_{C2} = I_O$

$I_E = (1+\beta) I_B$

$$\frac{I_o}{I_{ref}} = \frac{\beta(1+\beta)}{\beta+\beta^2+2}$$

Conclusion: The ratio $\frac{I_O}{I_{ref}}$ still not equal to 1, But this ratio much less depend on β. In β smaller or larger which would not affect the current ratio.

Wilson current source: special current source, less sensitive to base, provides output current I_o, which is very nearly equal to I_{ref} and also exhibits a very high output resistance. Collector current of the order of 5 μA. High o/p resistance of the circuit achieved by -ve feedback in Q3.



Analysis:

since $V_{BE1} = V_{BE2}$

$I_{C1} = I_{C2}$ and $I_{B1} = I_{B2} = I_B$

At node 'b'

$I_{E3} = I_{B1} + I_{B2} + I_{C2}$

$I_{E3} = I_B + I_B + I_{C2} = 2I_B + I_{C2}$.

$I_{E3} = 2\left(\frac{I_{C2}}{\beta}\right) + I_{C2} = I_{C2}\left[1 + \frac{2}{\beta}\right]$ —— (1).

I_{E3} is also equal to

$I_{E3} = I_{C3} + I_{B3} = I_{C3} + \frac{I_{C3}}{\beta} = I_{C3}\left[1 + \frac{1}{\beta}\right]$ —— (2)

From eq (1) and (2)

$$I_{C3}\left[1 + \frac{1}{\beta}\right] = I_{C2}\left[1 + \frac{2}{\beta}\right]$$

$$I_{C3} = I_{C2}\left[\frac{\beta+2}{\cancel{\beta}}\right] \times \left[\frac{\cancel{\beta}}{\beta+1}\right]$$

$\boxed{I_{C3} \text{ equal to } I_o}$

$$I_o = I_{C3} = I_{C2}\left[\frac{\beta+2}{\beta+1}\right]$$ —— (3)

since $I_{C1} = I_{C2}$

$$\boxed{I_o = I_{C1}\left[\frac{\beta+2}{\beta+1}\right]}$$ —— (4)

$I_o = I_{C2}\left[\frac{\beta+2}{\beta+1}\right]$

$I_o\left[\frac{\beta+1}{\beta+2}\right] = I_{C2} = I_{C1}$

$I_{C1} = I_o \cdot \frac{\beta+1}{\beta+2}$

$I_{B3} = \frac{I_{C3}}{\beta} = \frac{I_o}{\beta}$

At node a

$$I_{ref} = I_{C1} + I_{B3} = \frac{\beta+1}{\beta+2} I_o + \frac{I_o}{\beta} = I_o\left[\frac{\beta+1}{\beta+2} + \frac{1}{\beta}\right]$$

$$I_{ref} = \frac{\beta^2+2\beta+2}{\beta^2+2\beta} I_o, \quad \boxed{I_o = I_{ref} \cdot \frac{\beta^2+2\beta}{\beta^2+2\beta+2}}$$

Where $I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1}$

The difference $I_O - I_{ref}$.

$$I_O = \left[\frac{\beta^2+2\beta+2-2}{\beta^2+2\beta+2}\right] I_{ref}$$

$$= I_{ref}\left[\frac{\cancel{\beta^2+2\beta+2}}{\cancel{\beta^2+2\beta+2}} - \frac{2}{\beta^2+2\beta+2}\right]$$

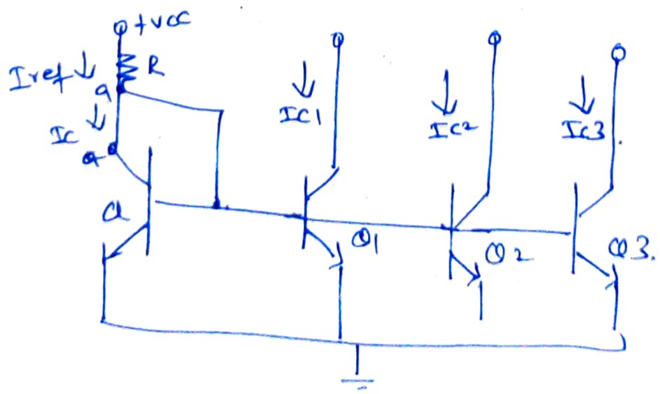
$$I_{C2} \text{ or } \boxed{I_O = I_{ref}\left[1 - \frac{2}{\beta^2+2\beta+2}\right]}$$

This above equation shows differe between $I_O - I_{ref}$ and the reference current differ by only a factor which is of the order of $2/\beta^2$. The o/p Resistance is greater than simple current mirror.

The o/p current $I_O = I_{C2}$ has lower sensitivity to base currents of transistor. Therefore $I_O \cong I_{ref}$ for wilson current source.

<u>current Repeater</u> (or) <u>multiple current source</u>

When there is a need to supply constant current (Reference) to multiple parts of a same or different circuits, multiple current sources are used. This reduces the component area, as it replaces many individual current sources. A single reference current is copied to multiple collector of transistors connected in cascade



$$I_{ref} = I_C + I_O + n I_B$$

$$I_C = I_{ref}\left(\frac{\beta}{n+1+\beta}\right)$$

$I_{ref} = (n+1) I_B + I_C$

$I_{ref} = (n+1) I_B + \beta I_B$

$I_{ref} = (n+1+\beta) I_B$

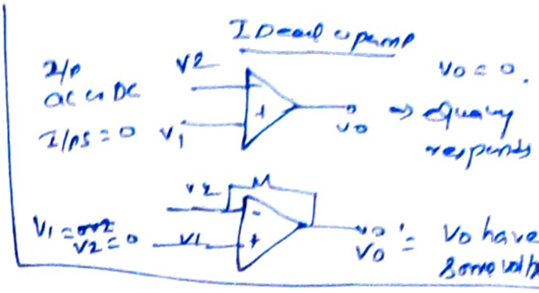
$I_{ref} = (n+1+\beta) \frac{I_C}{\beta}$

no of Transistors $n = 3$

28

Op-Amp characteristics

① DC characteristics
② AC characteristics



Let we know, ideal - op-amp responds equally well to both ac and DC inputs voltage. However, a pratical opamp not like this way, pratical opamp has some DC voltage at the output even with both inputs are zero (or) grounded.

DC characteristics

* An Ideal opamp draws no current from the source and it response is also independent of temperature.

Real opamp:

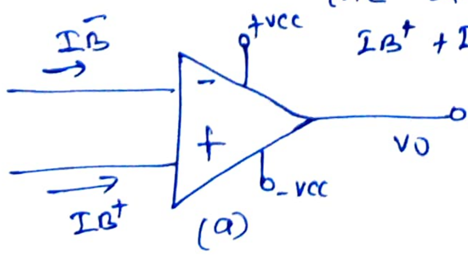
* current is taken from the source into the op-amp inputs, to bias the I/P transistors.
* Also the two I/Ps respond differently to current and voltage due to mismatch in transistors.
* Real op-amp also shifts it operation with Temperature.

These non-Ideal dc characteristics that add error to the dc o/p voltage are.

1) Input Bias current
2) I/P offset current
3) I/P offset voltage
4) Thermal drift.

1) I/P Bias current: An I/P Bias current is defined as the average of two input bias currents, $I_B^+ + I_B^-$.

$$I_B = \frac{I_B^+ + I_B^-}{2}$$



(a)

where

I_B^+ = DC Bias current flowing into non inverting I/P

I_B^- = DC Bias current flowing to inverting I/P.

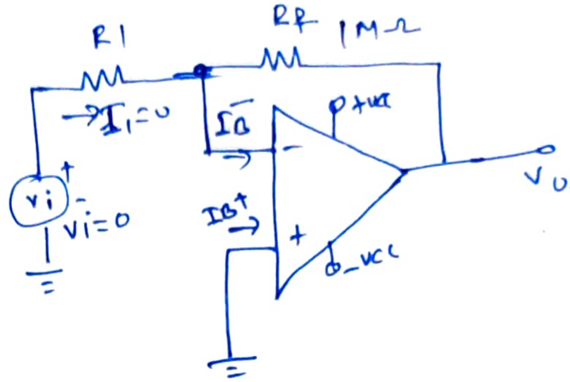
[I_B^+ and I_B^- are Base Bias currents of the transistors]

Eventhough both the transistors are identical, ~~I_B^- and I_B^+~~ it is not possible to have I_B^- and I_B^+ exactly equal to each other because of the internal imbalance between the two I/Ps.

Since $\boxed{I_B = I_B^- = I_B^+}$, $\boxed{I_B \text{ for a opamp 741 is 500 nA}}$ BJT or less

Consider, inverting amp,

If $V_i = 0V$, the o/p voltage V_o should also be zero, But, we find that the o/p voltage is offset by



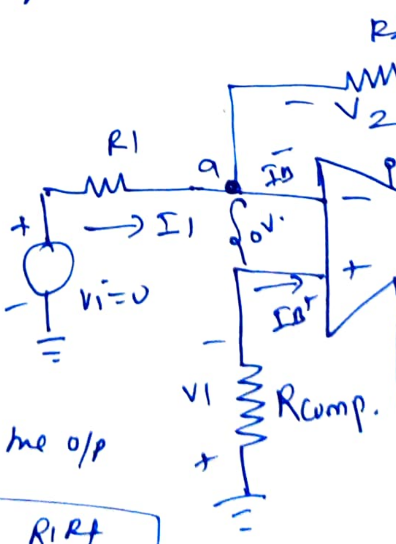
$$\boxed{V_o = I_B^- \cdot R_f}$$

$$V_o = 500nA \times 1M\Omega = 500mV.$$

The o/p is driven to 500mV with zero input because of bias currents, this is totally unacceptable.

Compensation: This effect can be compensated using Rcomp resistor has been added non inverting terminal and Ground. The current I_B^+ flowing through the Rcomp develops voltage V_1 across Rcomp and thereby cancel the voltage V_2 at node 'a'

By KVL

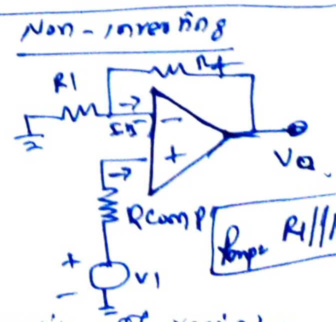


$$-V_1 + 0 + V_2 - V_o = 0$$

$$V_o = V_2 - V_1$$

By selecting proper value of Rcomp, V_2 can be cancelled with V_1 and the o/p will be zero.

The value of $\boxed{R_{comp} = \frac{R_1 R_f}{R_1 + R_f}}$



$\boxed{R_{comp} = R_1 \| R_f}$

The compensating Resistor should be parallel combination of resistor tied to the inverting I/P terminals

I/P offset current:

The Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.

ie $I_B^+ = I_B^-$ = will work

since the I/P transistors can not be made ~~equal~~ identical, there will always be some small differences between bias currents.

Definition: The input offset current I_{os} is defined as the algebraic ~~sum~~ difference between two input bias currents I_{B1} and I_{B2}

$$\boxed{|I_{os}| = I_B^+ - I_B^-}$$

$|I_{os}|$ = absolute value sign indicates that there is no way to predict which of the bias currents will be large

For 741, $I_{os} = 200nA$, Even though bias current compensation, offset current will produce an output voltage when the input voltage V_i is zero

Even R_{comp} is provided, $V_i = 0$, I_{os} produce some o/p

$$\boxed{\begin{aligned} V_o &= R_f\left[I_B^- - I_B^+\right] \\ &= R_f I_{os} \end{aligned}}$$

$$V_o = 1M\Omega \times 200nA = 200mV.$$

Finding vo

Refering Bias current compensation circuit.

$V_1 = I_B^+ R_{comp}$, and $I_1 = V_1/R_1$

Apply KCL at Node 'a'

$$I_2 = (I_B^- - I_1) = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1}\right)$$

$$V_o = I_2 R_f - V_1 = I_2 R_f - I_B^+ R_{comp}.$$

$$= \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1}\right) R_f - I_B^+ R_{comp}.$$

after substituting R_{comp} and some manipulation

$$V_o = R_f\left[I_B^- - I_B^+\right],$$

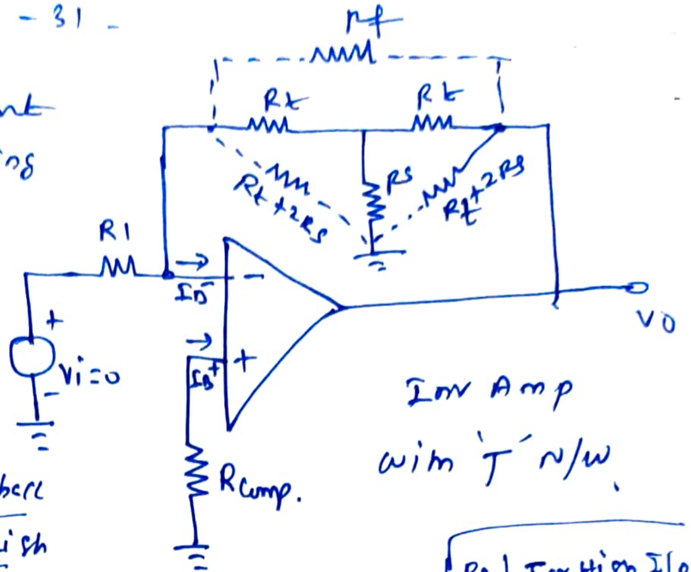
$$\boxed{V_o = R_f I_{os}}$$

Compensation

Compensation

The effect of offset current can be minimized by keeping feed back resistance small. unfortunaly, to obtain High I/P impedance, R_1 must be large.

With R_1 Large, the feed back resistance R_f must also be high so as to obtain Reasonable gain.



Inv Amp with 'T' N/W.

$R_f \downarrow$ For High I/P imp
$-R_1 \uparrow$ R_f also $\uparrow$,
so go for 'T' Net cir

For this situation, the 'T' Feed back N/w is good solution to minimise the offset current.

This will allow the large feed back resistance, while keeping the resistance to ground low; it act like single feed back Resister

$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}.$$

$$R_t << \frac{R_f}{2}$$

$$R_s = \frac{R_t^2}{R_f - 2R_t}$$

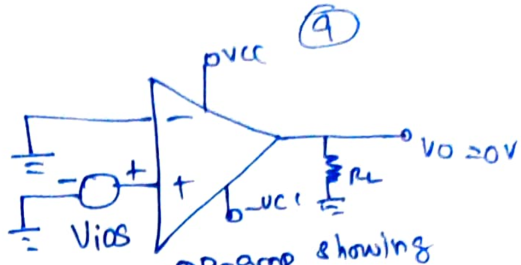
I/P offset voltage:

Inspite of the use of ~~ab~~ different Compensation techquies, it is found that the o/p voltage may still not be zero with Zero I/P voltage ~~because~~ due to unavoidable imbalances inside the opamp.

Definition: It is defined as the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero

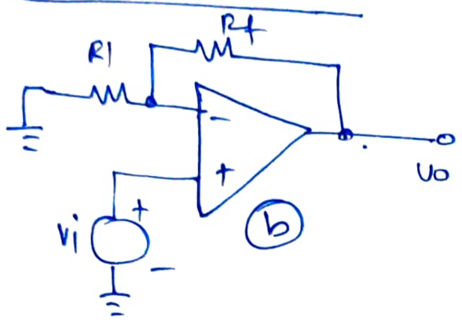
Effect of I/P offset voltage at o/p voltage

Vios is applied at the I/p terminal to make the output is zero.

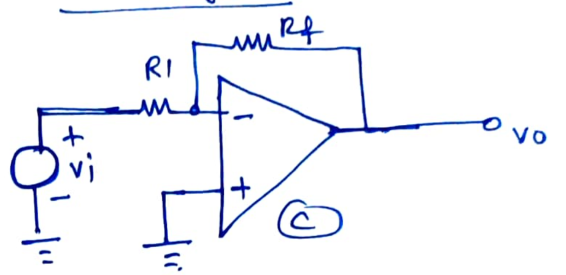


op-amp showing I/p offset voltage.

Non inverting amp

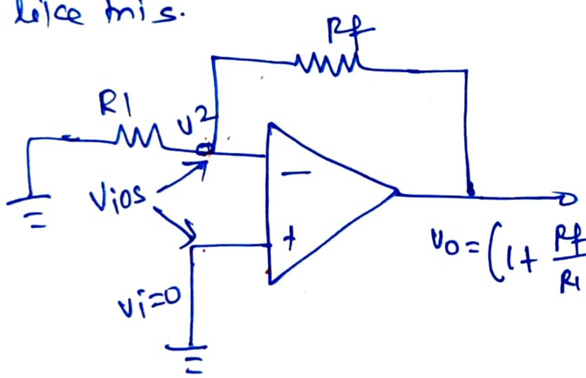


Inverting Amp



We see the effect of Vios on the I/p of Inv and non-inve amp.

When $V_i = 0$, the above (b) and (c) circuits become like this.



$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{ios}.$$

The voltage at V_2 is $V_2 = \left[\frac{R_1}{R_1 + R_f}\right] V_o$.

$$V_o = \left[\frac{R_1 + R_f}{R_1}\right] V_2 = \left(1 + \frac{R_f}{R_1}\right) V_2$$

since $|V_{ios}| = |V_i - V_2|$ and $V_i = 0$

$$\boxed{V_{ios} = |0 - V_2| = V_2}$$

or

$$\boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) V_{ios}}$$

o/p offset voltage of opamp in closed-loop configuration.

Total output offset voltage

Definition

Total o/p offset voltage defined as the sum of ~~tot~~ o/p offset voltage due to I/P offset voltage and ~~input~~ o/p voltage due to bias current IB

V_{OT} ↑↓ than offset voltage produces at the o/p due to IB or V_{IOS}

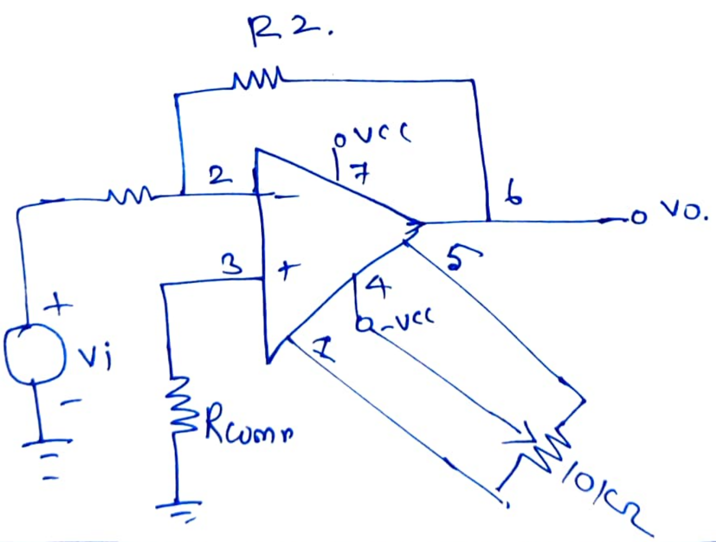
$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_B.$$

However, with Rcomp in the ckt, the total o/p offset voltage is given by

$$V_{OT} = \left[1 + \frac{R_f}{R_1}\right] V_{ios} + R_f I_{os}.$$

ckt for nullity the o/p offset voltage ~~nullity~~

The manufacture recommends 10kΩ pot and be placed across offset null pins 1 and 5 and the wiper be connected to pin 4. The position of the wiper is adjusted to nullify the o/p offset voltage.



Thermal Drift : Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain so when the temp rises 35°C, This is called drift

Reduce: Careful design of PCB, forced air cooling stabilize the temperature.

Ac characteristics

The factors that influence performance of opamp when AC input signal is applied are AC performance characteristics

Important characteristics

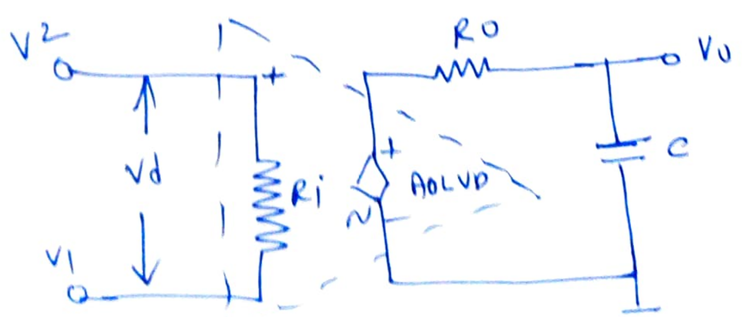
1. Frequency Response of op-amp
2. Stability of opamp
3. Frequency compensation of op-amp
4. Slew rate of op-amp

Frequency Response of opamp:

For an Ideal opamp should have infinite BW. This means that, if its open-loop gain is 90 db with dc signal, its gain should remain the same 90 dB through AC signal and on to higher radio frequencies. The pratical opamp gain, decreases at higher frequency. The way in which the gain of the opamp responds to frequency is called as frequency response.

The decrease in gain is due to the capacitive component in equivalent circuit of opamp. This capacitance due to physical characteristics of device (BJT or FET) used in the internal construction of op-amp

The single capacitor C representing all capacitance effect introduces one corner frequency. This model represents high frequency model of the opamp with one corner frequency



High frequency model of opamp with one corner frequency.

Key

For pratical opamp

frequency ↑ gain ↓ (Higher)

⇓ due to

Capacitance effect

⇓

physical characters of BJT & FET in construction

The open loop gain with single corner frequency is obtained by as

$$V_o = \frac{-jX_C}{R_o - jX_C} A_{OL} \cdot V_d$$

$$A = \frac{V_o}{V_d} = \frac{-jX_C}{R_o - jX_C} A_{OL}$$

sub $X_C = \frac{1}{2\pi f C}$, $-j = \frac{1}{j}$ and $j = \sqrt{-1}$, $j^2 = -1$

$$A = \frac{\frac{-j}{2\pi f C}}{R_o - j\left(\frac{1}{2\pi f C}\right)} \cdot A_{OL}$$

$$= \frac{\frac{-j}{2\pi f C}}{\frac{2\pi f R_o C - j}{2\pi f C}} A_{OL}$$

$$= \frac{\frac{1}{j}}{2\pi f R_o C - j} A_{OL}$$

$$= \frac{1}{j\,2\pi f R_o C - j^2} A_{OL}$$

$$A = \frac{1}{1 + j\,2\pi f R_o C} A_{OL}$$

This can be rewritten as

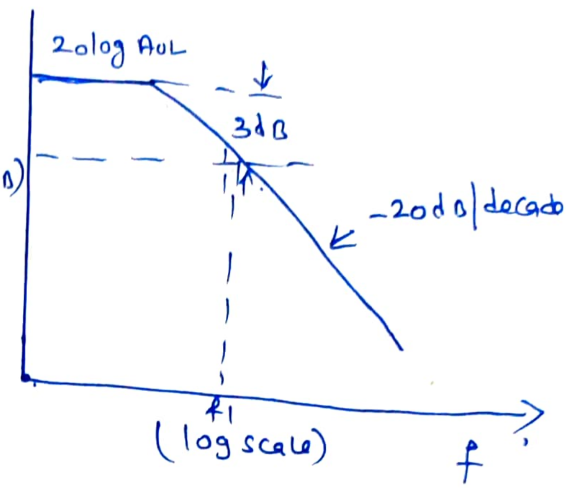
$$A = \frac{A_{OL}}{1 + j\left(\frac{f}{f_1}\right)}$$ where $f_1 = \frac{1}{2\pi R_o C}$ is the corner frequency

The magnitude and phase angle of A is

$$\boxed{|A| = \frac{A_{OL}}{\sqrt{1 + \left(\frac{f}{f_1}\right)^2}} \text{ and } \phi = -\tan^{-1}\left(\frac{f}{f_1}\right)}$$

The magnitude and phase characteristics, it can be seen that

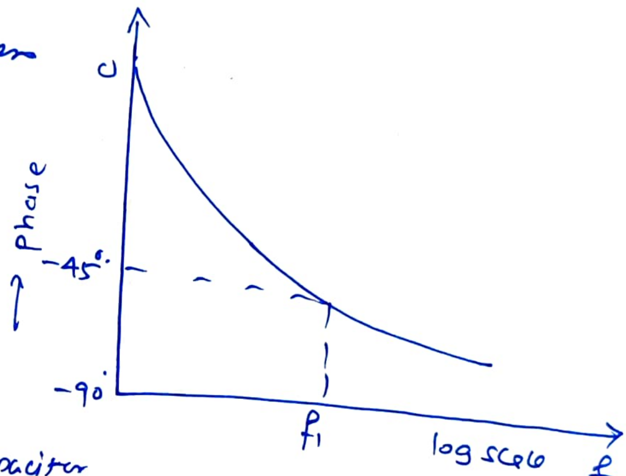
* For frequency $f << f_1$, the magnitude of gain is $20 \log A_{OL}$ in dB
* At frequency $f = f_1$, the gain is 3dB down from the dc value of A_{OL} in dB. This frequency is called corner frequency
* For $f >> f_1$ the gain decrease at the rate of -20 dB/decade



Magnitude Characteristics.

Phase characteristics

* at $f = 0$, ($f << f_1$) Phase angle is zero
* at f_1, ($f = f_1$) Phase angle is $-45°$
* at $f = \infty$, ($f >> f_1$) phase angle is $-90°$
* This shows that a maximum of $90°$ phase change can occur in an opamp with single capacitor



Phase characteristics

The transfer function of opamp with more number of corner frequencies is given by

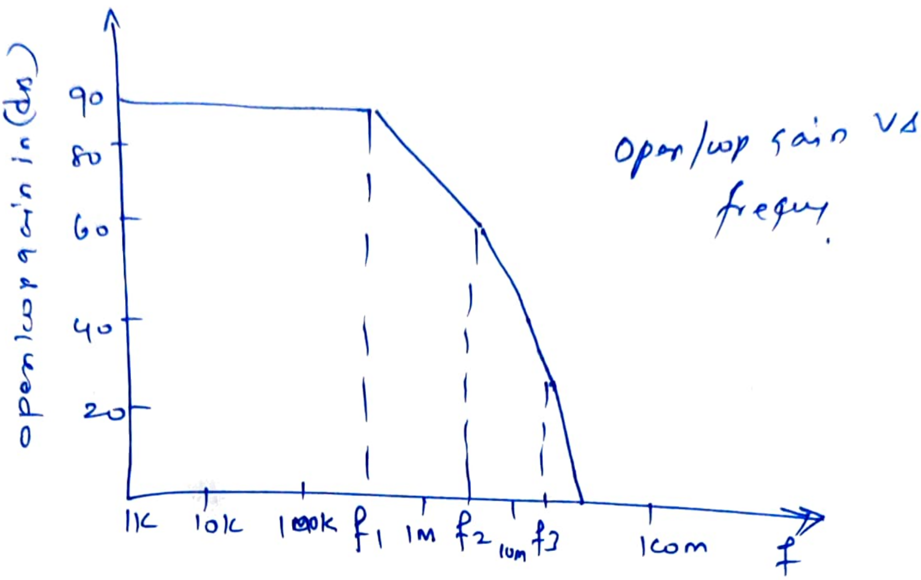
$$A = \frac{A_{OL}}{\left(1+j\left(\frac{f}{f_1}\right)\right)\left(1+j\left(\frac{f}{f_2}\right)\right)\left(1+j\frac{f}{f_3}\right)}, \quad 0 < f_1 < f_2 < f_3.$$

$$A = \frac{A_{OL}\,\omega_1\,\omega_2\,\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}, \quad 0 < \omega_1 < \omega_2 < \omega_3$$

Approximation of open loop gain vs frequency curve

* open loop frequency Response is flat (90dB) from low frequency to 200 KHz, the first break frequency
* From 200KHz to 2MHz, gain drops from 90 dB to 70 dB, which is at -20 dB/decade

* frequy 2MHz to 20MHz, the gain roll-off rate is -40dB/decade.



Conclusion

from above freq characteristics, as frequy is increasing, Cascading effect of RC pairs come into effect and roll-off rate increases successively by -20dB/decade at each corner frequy. Each RC pole pair also introduces a lagging phase of maximum upto -90°

Frequency compensation Techniques

Where we need 1) Larger Bandwidth and lower closed loop gain.

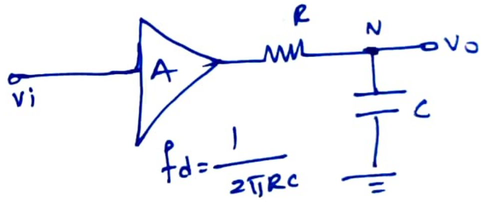
* External Compensation
* Internal Compensation.

External frequency compensation: The compensating N/w alter the open-loop gain so that the roll-off rate is -20 dB/decade over a wide range of frequency.

* common methods
  * Dominant-pole compensation
  * pole-zero (lag) compensation.

Dominant-pole compensation

The dominant-pole compensation is carried out by introducing Dominant pole by adding RC-network in series with op-amp.



The compensated Transfer function A' becomes

$$A' = \frac{V_o}{V_i}$$

Find Vo

$$V_o = \frac{-jX_C}{R - jX_C}$$

where $-j = \frac{1}{j}$, $j = \sqrt{-1}$, $j^2 = -1$, $X_C = \frac{1}{2\pi f C}$ producing a corner frequency or dominant frequency $f_d = \frac{1}{2\pi RC}$.

$$A' = \frac{V_o}{V_i} = \frac{A_{OL}}{1 + j\left(\frac{f}{f_d}\right)}$$

With three corner frequencies inside op-amp A' is given by.

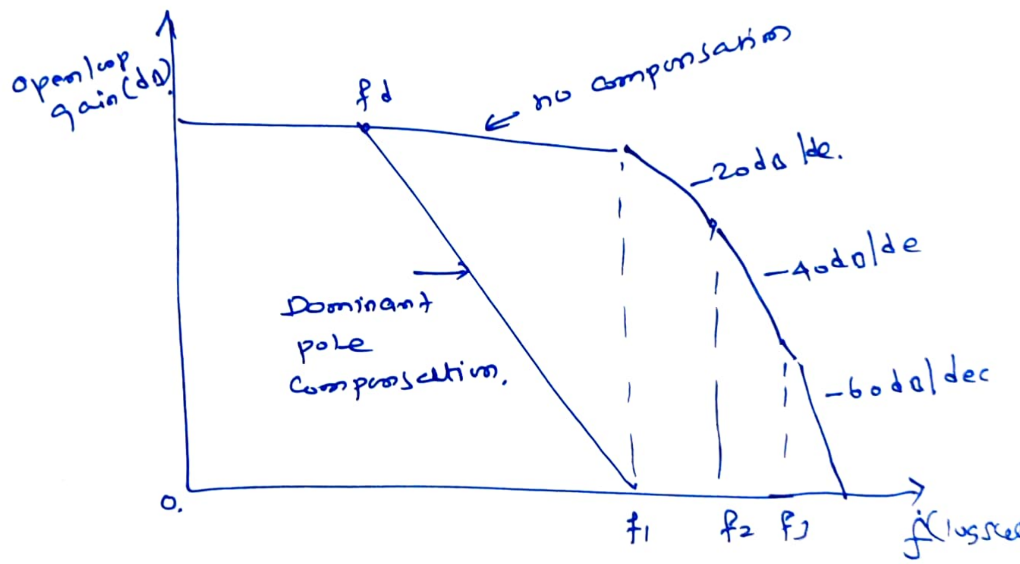
$$A' = \frac{A_{OL}}{\left(1 + j\frac{f}{f_d}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + \frac{jf}{f_3}\right)} \quad ; \; f_d < f_1 < f_2 < f_3$$

The value of f_d from R and C are selected such that, its slope passes through the first corner frequency f_1. This is done by introducing a pole (denominator polynomial in A') at f_1. So the gain has single roll-off -20 dB/dec as compared with three roll-offs in an uncompensated op-amp.

Disadvantage: It reduces the open-loop BW drastically. But the noise immunity of the system is improved since the noise frequency components outside the BW are eliminated.

~~pole-zero compensation~~

~~Here the uncompensated transfer function~~ is altered by ~~adding pole and zero~~



Gain vs frequency curve for Dominant pole compensation

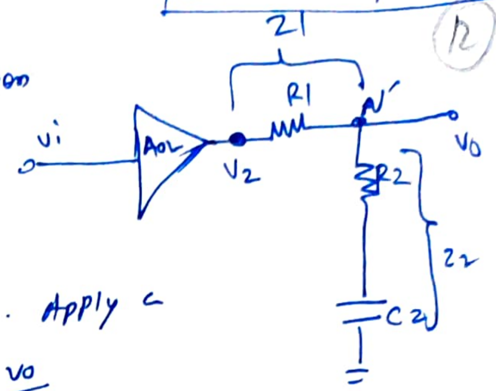
pole zero compensation [Definition]

The Dominant pole compensation has drawback that, " because of introduction of f_d, Bandwidth reduce drastically. "

The Reduction in Bandwidth can be improved by adding both pole and a zero. This technique is called pole-zero compensation.

pole-zero compensation

(12)



Here $Z_1 = R_1$, $Z_2 = R_2 - jX_{C2}$ —— (1)

The compensated transfer function A' is given by.

$$A' = \frac{V_o}{V_i} = \frac{V_o}{V_2}\cdot\frac{V_2}{V_i} \quad \text{—— (2)}$$

$\frac{V_2}{V_i} = A_{OL}$ and $\frac{V_o}{V_2}$ depends on Z_1 and Z_2. Apply a potential divider rule at node N' to find $\frac{V_o}{V_2}$

$$\frac{V_o}{V_2} = \frac{Z_2}{Z_1 + Z_2}. \quad \text{—— (3)}$$

sub (1) in (3)

$$\frac{V_o}{V_2} = \frac{R_2 - jX_{C2}}{R_1 + R_2 - jX_{C2}}$$

$$= \frac{R_2 - j\cdot\frac{1}{2\pi f C_2}}{R_1 + R_2 - j\frac{1}{2\pi f C_2}}$$

$$= \frac{\frac{2\pi f C_2 R_2 - j}{\cancel{2\pi f C_2}}}{\frac{2\pi f C_2 R_1 + R_2 2\pi f C_2 - j}{\cancel{2\pi f C_2}}}$$

$$= \frac{2\pi f C_2 R_2 - j}{2\pi f C_2 R_1 + R_2 2\pi f C_2 - j}$$

$$\boxed{-j = \frac{1}{j},\ j^2 = -1}$$

$$= \frac{2\pi f C_2 R_2 + \frac{1}{j}}{2\pi f C_2 R_1 + R_2 2\pi f C_2 + \frac{1}{j}}$$

j = cancel

$$= \frac{j2\pi f C_2 R_2 + 1}{j2\pi f C_2 R_1 + jR_2 2\pi f C_2 + 1}$$

$$\boxed{\frac{V_o}{V_2} = \frac{1 + j\left(\frac{f}{f_1}\right)}{1 + j\left(\frac{f}{f_o}\right)}}$$

$\frac{V_2}{V_i} = A$

where $f_1 = \frac{1}{2\pi R_2 C_2}$, $f_o = \frac{1}{2\pi(R_1+R_2)C_2}$

$$\frac{V_o}{V_2} = \frac{1 + j\left(\frac{f}{f_1}\right)}{1 + j\left(\frac{f}{f_o}\right)} \quad \text{—— (4)}$$

Sub equation (4) and $\frac{V_2}{V_i} = A_{OL}$ in equation (2) then

$$A' = \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \cdot \frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_o}}$$

$$\therefore A' = \frac{A_{OL}}{\left(1 + j\frac{f}{f_o}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

with $0 < f_o < f_1 < f_2 < f_3$

Conclusion (K)

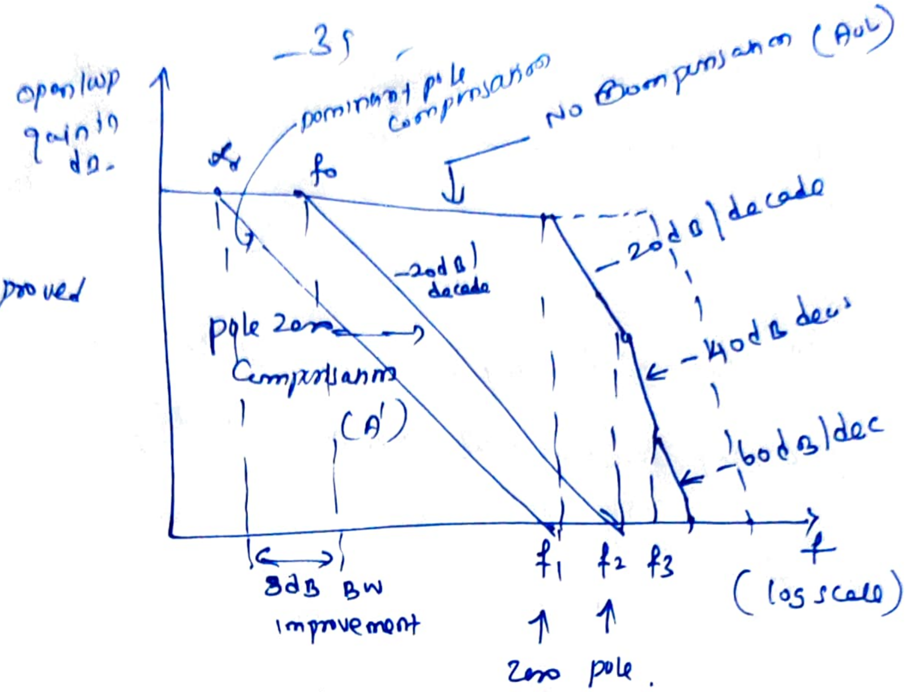
Thus the compensated transfer function A' shows the introduction of a zero at corner frequency f_1 $\left(1 + j\frac{f}{f_1}\right)$. So the slope of new frequency f_o passes through f_2, as a pole was introduced at corner frequency f_2.

The component values are selected such that, the slope is made to pass through f_2 rather than f_1.

— 35 —

Advantge

Bandwidth improved



Pole-zero compensation

Slewrate

o/p

Definition: It is defined as the maximum rate of change of o/p voltage caused by a step input voltage and usually specified in V/μs

$$SR = \frac{dv_o}{dt}$$

Meaning of slew rate: (It tells how fast a op-amp o/p ~~reacts~~ changes to the given input voltage) For ideal op-amp, Slewrate is infinite. So the o/p voltage responds instantaneously to any change in input voltage. But the practical op-amp the o/p voltage do not respond immediately with respect to input voltage due to slew rate.

Example:

A opamp with 1V/μs slewrate means that the o/p rises or falls by 1V in one microsecond. Similarly, a op-amp with 1000V/μs slew rate means, the o/p raises or falls by 1000V in one micro second of time (ie) respons immediately.

Slewrate is frequeny related and function ~~of~~ to temperature, generaly decreases with an increase in temperature.

What causes slew rate?

Usually a capacitor within or outside op-amp which to prevent oscillations. It is this capacitor which prevents the output voltage from responding immediatly to a fast changing i/p. The rate at which the voltage across the capacitor changes is given an slew rate

$$SR = \frac{dv_o}{dt} = \boxed{\frac{dv_c}{dt} = \frac{I_{max}}{C}}$$

I_{max} => maximum current flowing from to capacitor C

From equation, for obtaining faster slew rate, op-amp should have either a higher current or a small compensating capacitor.

Example: For 741 IC, the maximum current flows is limited to about 15 μA. and a 30 pF internal capacitor C_1 is used for frequency compensation. Therefore slew rate is

$$SR = \frac{dv_c}{dt} = \frac{dv_o}{dt} = \frac{I_{max}}{C_1} = \frac{15\,\mu A}{30\,pF} = 0.5\,V/\mu s$$

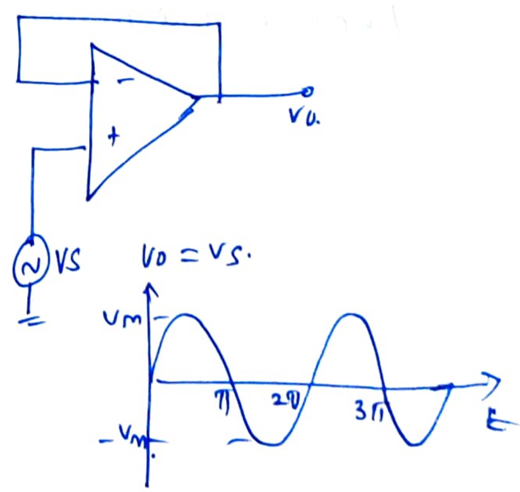
SR = 0.5 V/μs is slow speed op-amp.

$SR < 100\,V/\mu s \rightarrow$ slow speed op-amp

$SR > 100\,V/\mu s \rightarrow$ High speed opamp

Effect of Slew Rate for Sine wave I/P

Let I/p is Large amplitude, Higher frequency



$V_s = V_m \sin \omega t$

$V_o = V_m \sin \omega t$

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t$$

$$SR = \left.\frac{dv_o}{dt}\right|_{max} = \omega \cdot V_m$$

ie max Rate of Change of o/p occurs when $\cos \omega t = 1$

$\therefore$ slew Rate $= 2\pi f V_m$ V/s

$$SR = \frac{2\pi f V_m}{10^6}\ V/\mu s.$$

f: I/p frequency (Hz)

V_m = peak o/p amplitude.

$$SR = \frac{2\pi f V_m}{10^6} \, V/\mu s.,$$

In the above equation, right hand side parameter is less than slew rate of op-amp, then output will be distorted. If frequency or amplitude of I/P signal is increased to exceed the slew rate of op-amp, the O/P will be distorted.

How to obtain undistorted o/p: Thus the maximum I/P frequency f_{max} at which we can obtain an undistorted output voltage of peak value V_{in} is given by

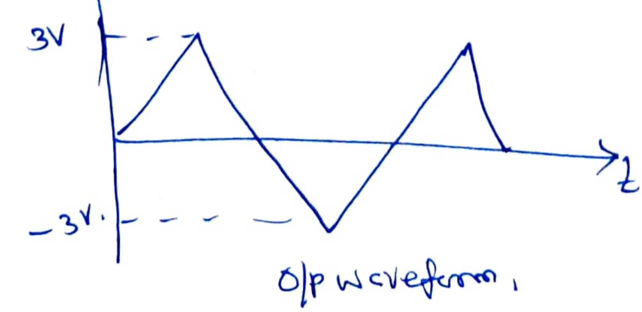
$$\boxed{f_{max}(Hz) = \frac{\text{slew rate}}{6.28 \times V_m} \times 10^6}$$

It is the maximum frequency of a large amplitude sine wave with which op-amp can have without distortion

Example 2: Que: The o/p of op-amp voltage follower is triangular wave for a square wave I/P of frequency 2 MHz and 8 V peak to peak Amplitude. What is the slew rate of op-amp?

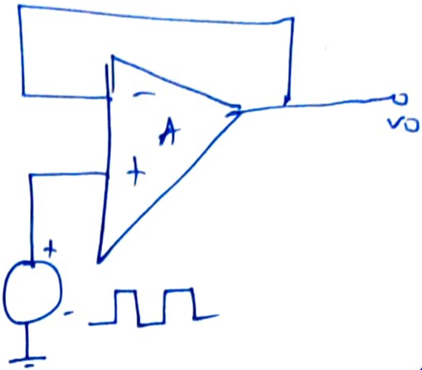
Slew rate is defined as the maximum rate of change of the output.

So, $SR = \frac{2\pi f V_m}{10^6} V/\mu s = \frac{6V}{(0.5/2)\mu s} = 24 V/\mu s.$



O/P waveform.

Effect of square wave I/p:



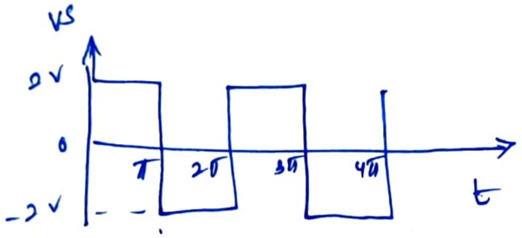
$A_{CL} = 1 + \frac{R_f}{R_1}$, $R_f = 0$, $R_1 = \infty$ with respect to ground.

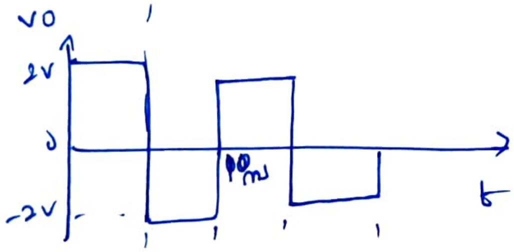
$A_{CL} = 1 = \frac{v_o}{v_i} = \frac{v_o}{v_s}$

if $v_o = v_s$ indicates that o/p voltage v_o just follows the input voltage V_s.

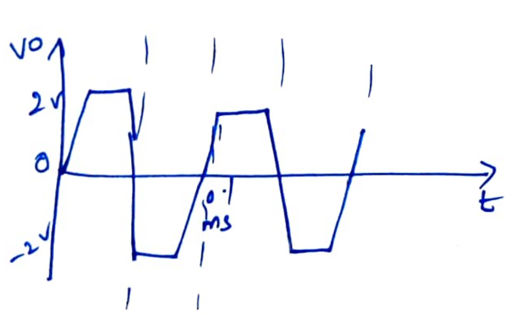
Thus the output terminals must produce a square wave for square wave I/p. But the slew rate limit the performance, as the frequency of I/P signal increases.

Effect of o/p with different frequency of I/p square wave

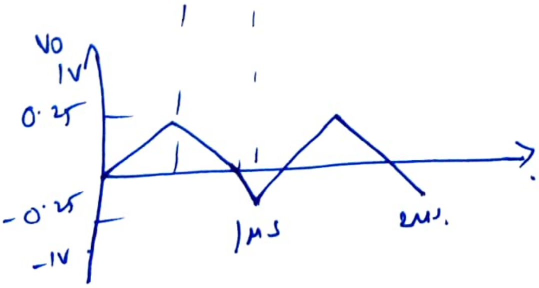




for 100 Hz of square wave I/p, o/p is distortion less o/p.



10 KHz square wave I/p, o/p is distorted.



Due to limited slew rate, for 1 MHz I/p square wave the o/p becomes distorted into sawtooth. This has occurred because of predominance of capacitance present in the circuit at high frequencies, RC pair are in cascade and the time constants are high compared to high frequency square wave I/p.

Methods to improve the slew Rate

The gain BW product of op-amp is given by

$$f_t = \frac{g_m}{2\pi C}$$

$$S = 2\pi \frac{I_o(sat)}{g_m} \cdot f_t$$

From the above exp, the methods of improving slew rate can be given.

1. Increasing f_t → To increase f_t, the internal capacitor value must be reduced.

2. Increasing $I_{o(sat)}$ - To increase $I_{o(sat)}$, programmable op-amps can be used. The operating point of the device can be set by the user with external current I_{sat}.

3) Reducing 'g_m' - To reduce g_m suitable series resistance with emitters of differential input transistor can be used and using FET-opamps

4) Frequency compensation can be used

Prm: A 741C op-amp is used as inverting amp with a gain of 50. The voltage gain Vs freq curve of 741 is flat upto 20 kHz. What maximum peak to peak input signal can be applied without distorting the o/p?

Slew rate for 741C is 0.5 V/μs, so max o/p voltage at 20kHz is

$$0.5 = \frac{(2\pi)(20\times10^3)(V_m)}{10^6}$$

$V_m = 3.98$ peak

$V_o = 7.96$ V peak to peak

45

Find the max frequ for an opamp with sine wave output voltage 10V peak and slew rate is 2V/μs

$$SR = \frac{2\pi f V_m}{10^6} V/\mu s$$

$$f_{max} = \frac{SR \times 10^6}{2 \times \pi \times V_m} Hz = \frac{2 \times 10^6}{2 \times \pi \times 10} = 31.83 KHz$$

---

why is frequ compensation is required in op-amp

(i) To achive Large desired BW

(ii) To Reduce the Closed-loop gain

(iii) To improve the behavior of opamp at higher frequencie

(iv) To ensure a roll-off of −20 dB/dec with single corner frequency and to avoid instability at high frequy.

2) What is the advantges of current mirror?

1) Keep the o/p current constant regardless of loading

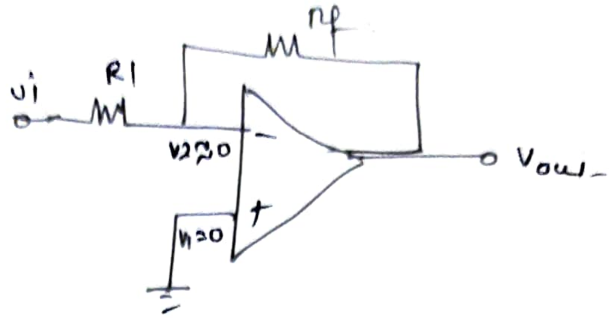
2) o/p current not affected by any other external parameters

3) It can act as a active Load, thereby producing Large differential mode gain and thus CMRR

4) occupies Less space in an IC compare to R Load i.e passive Load circuit.

Define PSRR: power supply rejection ratio: It is defined as the change in I/P offset voltage V_{io} with change in supply voltage is given by $\frac{\Delta V_{io}}{\Delta V}$.

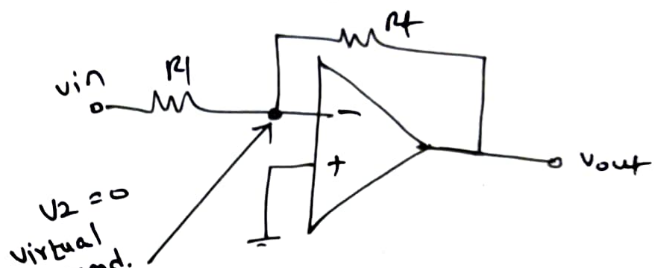
Virtual ground concept in inverting amp



Gain = $\frac{Vo}{vi}$, if vin = 0 , gain is infinite

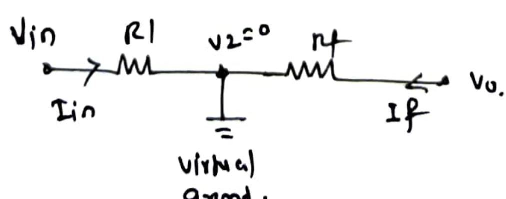
$vi = V_2 - V_1$

In the above circuit V_1 is connected to ground, so $V_1 = 0$.
Thus V_2 also will ~~be~~ be at ground potential.



Why we need virtual grnd?

~~us~~ It needed to analyze the op-amp when negative feedback is employed. It will simply a lot of calculations and derivations.



The V_2 voltage is approximately zero, not able to sink infinite current.

A Differential amplifier has CMRR = 1000. Differential inputs $V_1 = 1100\,\mu V$ and $V_2 = 900\,\mu V$. calculate the difference in output voltage if the differential gain $A_D = 25000$

$V_1 = 1100\,\mu V$ $\quad V_2 = 900\,\mu V$, CMRR = 1000, $A_D = 25000$

$$V_o = A_d V_{id} + A_c V_{ic}$$

$$V_o = A_d V_{id}\left[1 + \frac{A_c}{A_d}\,\frac{V_{ic}}{V_{id}}\right]$$

$$= A_d V_{id}\left[1 + \frac{1}{(A_d/A_c)}\,\frac{V_{ic}}{V_{id}}\right]$$

$$\boxed{V_o = A_d V_{id}\left[1 + \frac{1}{CMRR}\cdot\frac{V_{ic}}{V_{id}}\right]}$$

Let $V_{id} = V_1 - V_2 = 1100\,\mu V - 900\,\mu V = 200\,\mu V.$

$$V_{ic} = \frac{V_1 + V_2}{2} = \frac{1100\,\mu V + 900\,\mu V}{2} = \frac{2000}{2} = 1000\,\mu V.$$

$$V_o = 25000\cdot \cancel{1000}^{200}\,\mu V\left[1 + \frac{1}{1000}\cdot\frac{\cancel{1000}^{5}\,\mu V}{\cancel{200}\,\mu V}\right]$$

$$= 25000 \times 200\left[1 + \frac{5}{1000}\right]$$

$$= 5000000\,[1.005]$$

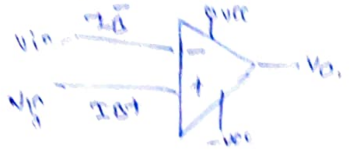
$$V_o = 5025000\,\mu V.$$

Explain the significance of virtual ground.

In opamps the term virtual ground means that the voltage at that particular node is almost equal to ground voltage (0V). It is not physically connected to ground.

Opamp DC characteristics

1) I/p Bias current: Average of two Inputs Bias currents $I_B = \frac{I_B^+ + I_B^-}{2}$



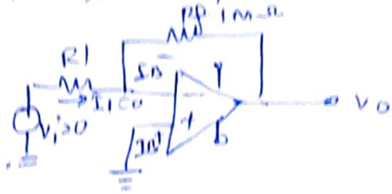
Due to imbalances of internal circuit $I_B^+ \neq I_B^-$

When $v_i = 0$, o/p should be zero, but due to Bias current some o/p voltage at the o/p terminal

For example

$V_o = I_B^- R_f$

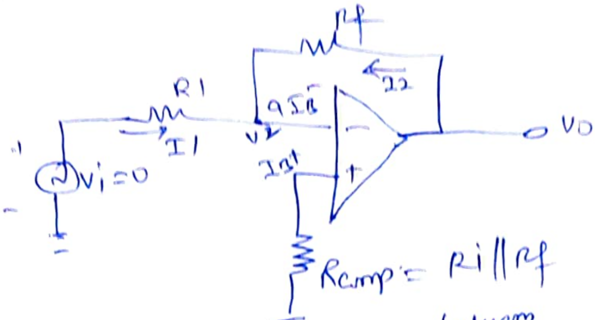
$500\,nA \times 1M\Omega = 500\,mV$.



This 500mv occur Due to Bias current even though $V_i = 0$.

Compensation: To Compensate this voltage, Connect R_{comp} resistor in noninverting terminal it will cancel the voltage V_2 at node 'a'

$R_{comp} = R_1 \| R_f$



2) I/p offset current:

Defined as the algebric sum of difference between I/p Bias currents I_B^+ and I_B^-

NOTE: Even though compensation provided for Compensat I/p Bias currents, there is a o/p voltage due to I/p offset current when $V_i = 0$.

$$\boxed{|I_{os}| = I_B^+ - I_B^-}$$

For 741, $I_{os} = 200\,nA$, there is a offset current at o/p

$V_o = \cancel{R_{cnf}}\, R_f\, [I_B^- - I_B^+]$

$= R_f I_{os}$

$= 1M\Omega \times 200\,nA = 200\,mV$.

So we have to provide compensation circuit.

Compensation

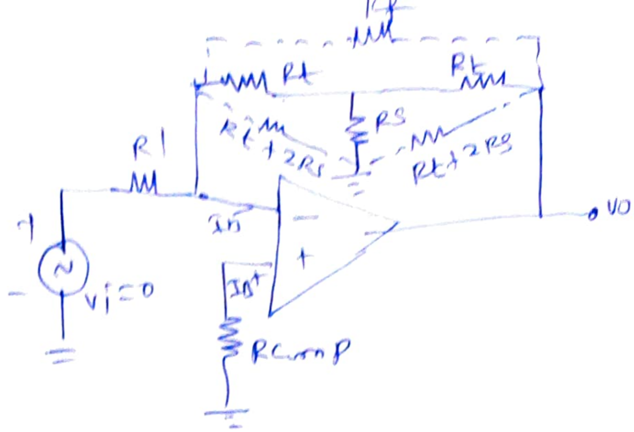
NOTE: The ~~ef~~ effect of offset current Can be minimized by keeping feedback resistance small. unfortunally to obtain High I/p impedence R_1 must be large. with R_1 large, the feedback resistance R_f ~~R_f~~ must also be High. So as to obtain Reasonable gain.

For this situation we use T Feed back N/w to minimize the offset current. This will allow the large feed back resistance while keeping the resistance to ground low, and it act like a single feed back resister.

$$R_f = \frac{R_t^2 + 2R_t R_s}{R_s}$$

$$R_t << \frac{R_f}{2}$$

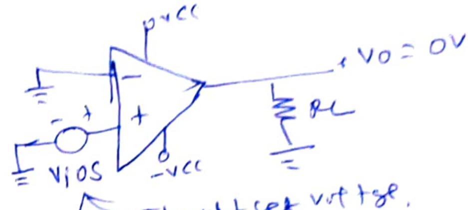
$$R_s = \frac{R_t^2}{R_f - 2R_t}$$



3) Input offset voltage

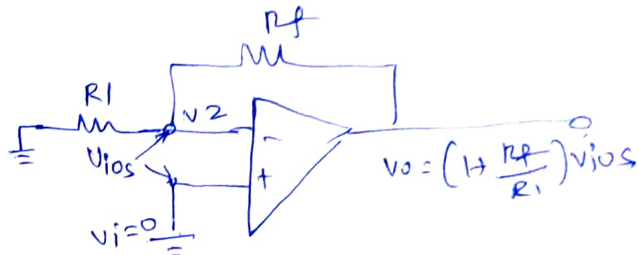
Definition: The amount of I/p voltage that should be applied between the input terminals in order to force the output voltage to zero.

VIos applied between the I/p terminal to make the o/p is zero.



For Inverting and Non Inverting OpAmp

The effect of Vios when $v_i = 0$, the circuit becomes like below.



The voltage at V2 is

$$V_2 = \left[\frac{R_1}{R_1 + R_f}\right] V_o$$

$$V_o = \left[\frac{R_1 + R_f}{R_1}\right] V_2 = \left(1 + \frac{R_f}{R_1}\right) V_2$$

Since $V_{ios} = |v_i - V_2|$ and $v_i = 0$,

$V_{ios} = |0 - V_2| = V_2$ or $V_o = \left[1 + \frac{R_f}{R_1}\right] V_{ios}$

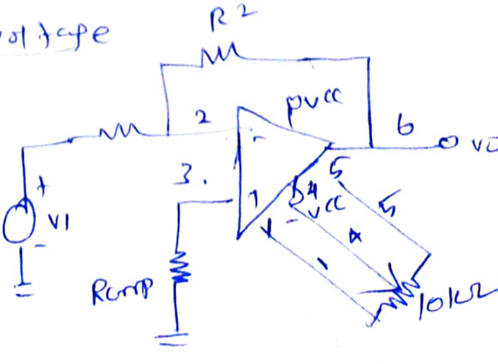
Total o/p offset voltage: Sum of o/p offset voltage due to I/p offset voltage and o/p voltage due to Bias current I_B.

$$V_{OT} = \left[1 + \frac{R_f}{R_1}\right] V_{ios} + R_f I_B$$

with Rcomp: $V_{OT} = \left[1 + \frac{R_f}{R_1}\right] V_{ios} + R_f I_{os}$

Circuit for nullify the o/p offset voltage

~~The~~ put 10k pot between offset null pin 1 and 5 and the wiper be connected to pin 4. The position of wiper is adjusted to nullify the o/p offset voltage.



Ac characterisiics : The factors that influence performance of opamp when Ac input signal is applied are Ac performance characterisnics

Important characteristics are:

① Frequency Response ② Slew rate ③ Stability ④

④ Frequency compensation.

1) Frequency Response: The variation of operating frequency will case variation in gain magnitude and its phase angle.

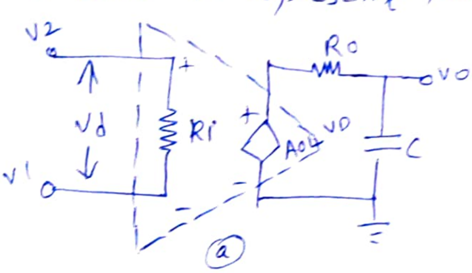
The way in which the gain of the opamp responds to different frequencies is called frequency Response.

* Why does op-amp gain decreases at high frequency?

At higher frequencies, the internal junction capacitor of transistor come into play, thus reducing the output and therefore gain is decreases:

Let $X_C = \frac{1}{2\pi f C}$ if frequency is increased, capacitive Reactance decreases so it bypass the majority of o/p. so gain decreases at higher frequency

Figure below shows the low frequency model with single capacitor 'C' at out-put to represent the capacitor effect.



ⓐ

The open loop gain with single corner frequency is given by

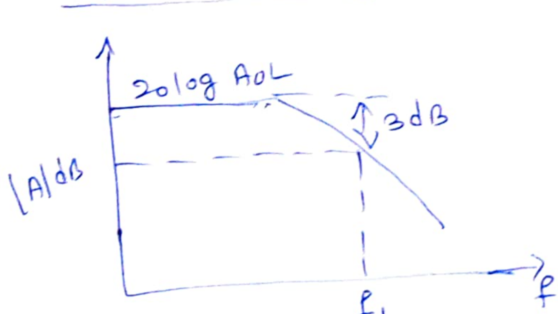
The magnitude $|A| = \frac{A_{OL}}{\sqrt{1+\left(\frac{f}{f_1}\right)^2}}$

phase $\phi = -\tan^{-1}\left(\frac{f}{f_1}\right)$

$$\boxed{\text{Gain } A = \frac{A_{OL}}{1+j\left(\frac{f}{f_1}\right)}} \quad f_1 = \frac{1}{2\pi R_o C}$$

Note: if possible Drive the equation refer Notes

Magnitude Response



(log scale)

ⓑ

From Response ⓑ

$f << f_1$, the magnitude gain is $20 \log A_{OL}$ in dB

$f = f_1$, the gain is 3dB down from the dc value of A_{OL} in dB

This frequency is called corner frequency.

$f > f_1$, the gain decreases at the rate of -20 dB/decade.

Phase characteristics

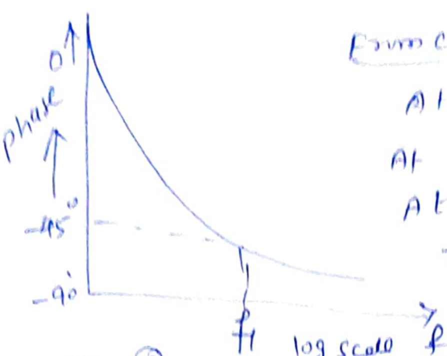


Fig (C)

From characteristics (C)

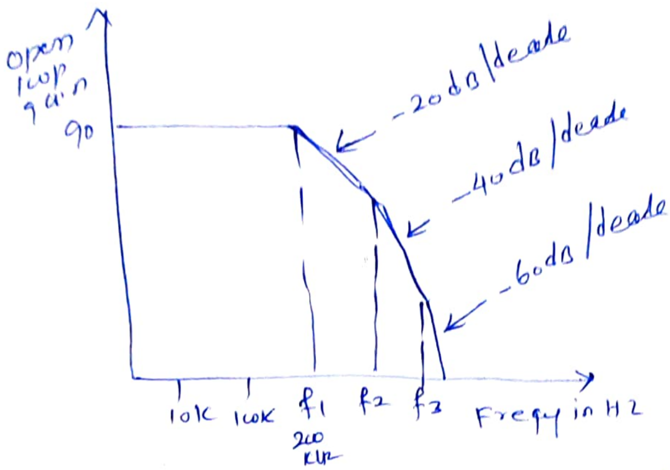
At $f = 0$ phase angle is 0 [$f << f_1$]

At $f = f_1$ phase angle is $45°$ ($f = f_1$)

At $f = \infty$, phase angle is $-90°$ [$f >> f_1$]

This shows that maximum of $90°$ phase change can occur in an opamp with single capacitor.

The ~~tran~~ Approximation of open loop gain vs frequency Response curve



* 0 - 200 KHz open loop response is Flat (90dB) the first break corner frequency.
* From 200KHz to 2MHz gain drops from 90dB to 70dB, which is at -20dB/decade.

Conclusion: From above characteristics, as frequency is increases cascading effect of RC pairs come into effect and roll-off rate increases successively by -20dB/decade at each corner frequency. Each RC pole pair also introduce a lagging phase of maximum up to $-90°$

Transfer function of opamp with more corner frequency is given by

$$A = \frac{A_{OL}}{1+j\left(\frac{f}{f_1}\right)\left(1+j\left(\frac{f}{f_2}\right)\right)\left(1+j\left(\frac{f}{f_3}\right)\right)}$$

Slew Rate:

Definition: It is the rate at which the opamp can detect voltage changes

(or)

The rate at which the voltage across the capacitor changes is given as slew rate.

$$SR = \frac{dv_o}{dt} = \frac{dv_c}{dt} = \frac{I_{max}}{C}$$

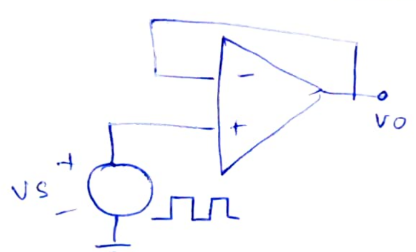
I_{max} → maximum current flowing from to capacitor 'C'

Note 1: For ideal opamp slew rate is ∞, so the o/p voltage responds (or) changes instantaniously to any change in I/p but pratical opamp, the output voltage does not respond immediatey with respect to I/P voltage change due to slew rate.

What causes the slew rate? : Because of capacitor is inside or outside opamp prevents the output voltage from responding immediatey to a fast changing the I/P voltage.

Note 2: For $\mu A741$ slew rate is $0.5V/\mu s$ it means that output raises or falls by 0.5V in one micro seconds

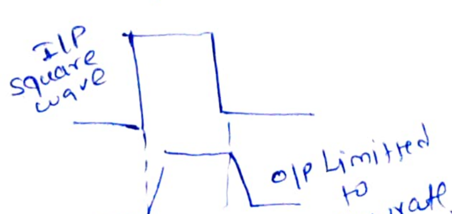
Effect of slew rate for square wave as I/P



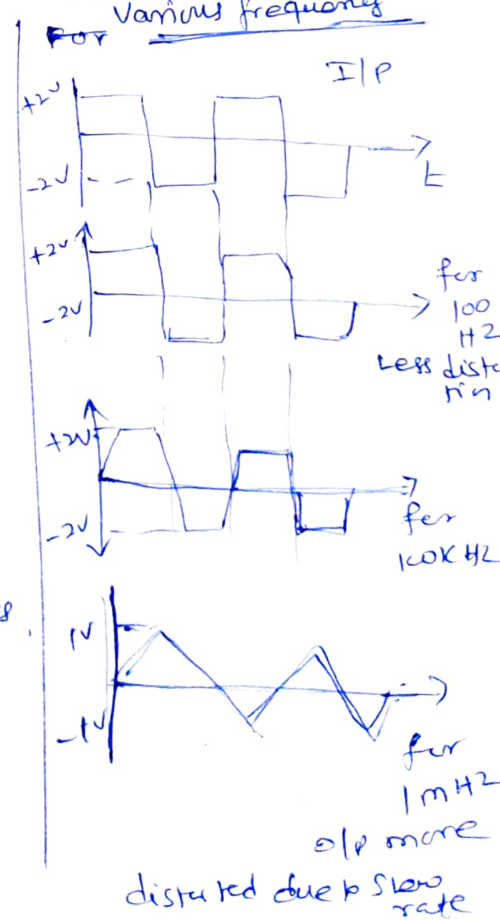
$A_{CL} = 1 + \frac{R_f}{R_1}$, $R_f = 0$, $R_1 = \infty$.
with respect to ground.

so $A_{CL} = 1 = \frac{V_o}{V_i} = \frac{V_o}{V_s}$.

if $V_o = V_s$, indicate the o/p voltage 'V_o' just follow the I/P But the slew rate limit the performance as the frequeny of I/p signal increases.



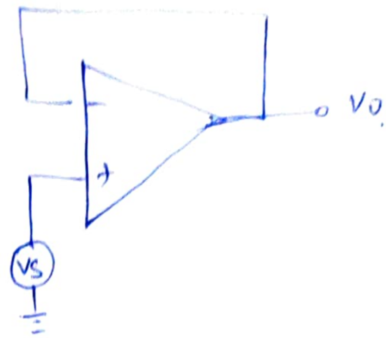
Effect of slew rate for various frequency



Effect of slew Rate for sine wave I/P

If the opamp is operated above its slew rate limit, signals will become distorted.

it can be see by using sine wave form.



Let $V_s = V_m \sin \omega t$

$V_o = V_m \sin \omega t$

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t$$

$$SR = \left.\frac{dv_o}{dt}\right|_{max} = \omega \cdot V_m \quad \text{when } \cos \omega t = 1$$

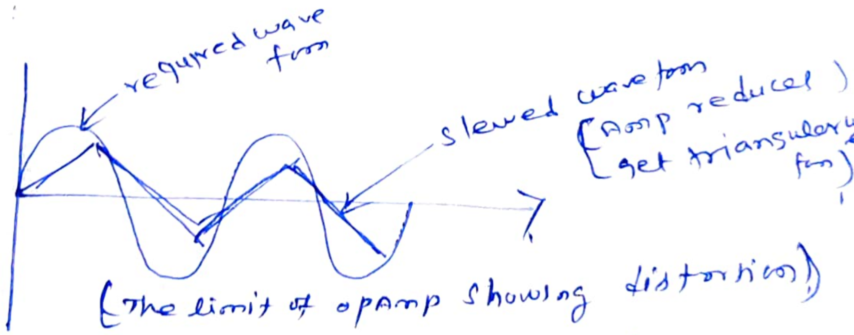
ie max Rate of change of O/P occurs

Slew Rate calculation, = $SR = 2\pi f V_m$ V/s,

$$SR = \frac{2\pi f V_m}{10^6} \text{ V}/\mu s.$$

For ex: f = Hz, peak voltage = ~~volt~~ 'V' volts ~~required~~

require an opamp with slew rate of $\boxed{2\pi f V}$



(The limit of opamp showing distortion)

NOTE: If the frequency of opamp even less able to keep up and therefore the amplitude of the o/p wave form will decrease.

Slew ~~Rate~~, may also not ~~linear~~ be linear over the whole range but it can raise and fall.

The o/p of operational Amp can only change by a certain amount of given time. This limit is called the slew rate of opamp.

UNIT - II APPLICATIONS OF OPERATIONAL AMPLIFIER

INTRODUCTION:

Two types of Applications.

1. Linear Applications ⇒ O/p voltage varies linearly with respect to i/p voltage
   ⇒ Negative f/b is used from the amplifier o/p to inverting i/p terminal
   ⇒ Examples: Voltage follower, Adder, subtractor, Instrumentation amp. Integrator, differentiator

2. Non-linear Applications:
   ⇒ a f/b is provided from o/p to non-inverting i/p terminal or to the inverting i/p terminal using non-linear elements like diode transistors etc.,
   ⇒ Examples: precision rectifier, log & antilog amplifiers, Comparators, Schmitt trigger circuits.

Two assumptions are used to simplify the analysis of Op-amp circuits

(i) Zero i/p Current → (ie) I drawn by either of i/p terminals is zero

(ii) Virtual Ground ⇒ Differential i/p Voltage V_d b/w two

Example:

If o/p V is 10V & A_{OL} (open loop gain) is 10^4, then

$$V_o = V_d A_{OL}$$

$$\therefore V_d = \frac{V_o}{A_{OL}} = \frac{10}{10^4} = 1mV$$

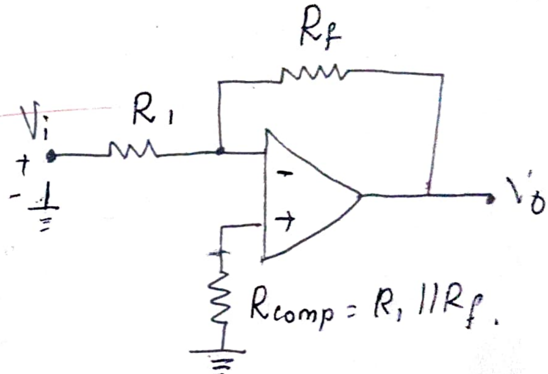
As $A_{OL} \to \infty$, $V_d \to 0$ & realistically assumed to be zero for analyzing the circuit.

$$V_d = \frac{V_o}{A_{OL}} = \frac{V_o}{\infty} = 0$$

$$\therefore V_1 - V_2 = 0 \quad \therefore V_1 = V_2$$

Scale changer ($R_f/R_1 = k$)
Phase inverter ($R_f/R_1 = 1$)

SIGN CHANGER



In ideal inverting amp,
if $R_f = R_1$ then gain $A_{CL} = -1$

$$\left\{ A_{CL} = \frac{-R_f}{R_1} = \frac{-R_1}{R_1} = -1 \right\}$$

Thus mag. of o/p is same as that of i/p but its sign is opposite to that of i/p

$$\boxed{V_o = -V_{in} \text{ for } R_f = R_1}$$

sign changer / Phase inverter;

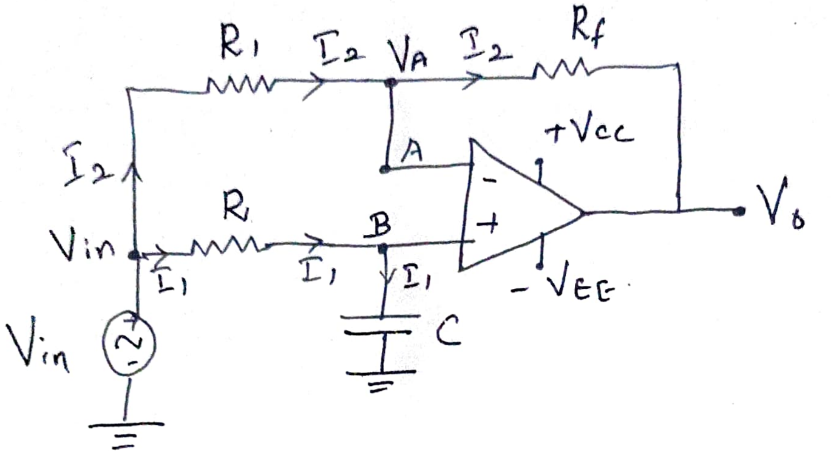
SCALE CHANGER

In ideal inverting amp, if $R_f \neq R_1$ then $A_{CL} = -k$ where $k = R_f/R_1$. Thus circuit is used to multiply i/p by a constant k called scaling factor

$$\boxed{V_o = -kV_{in}}$$

PHASE SHIFT CIRCUITS

A phase shifter circuit is one in which all signals are transmitted from i/p to o/p without change in amplitude but the circuit introduces a phase shift as signal transmits from i/p to o/p.



Phase shifter Circuit.

Mathematical Analysis

As op-amp i/p I is zero, I_1 flows thro' C while I_2 flows thro' R_f. While due to virtual ground $V_A = V_B$

from fig,: $V_B = \frac{1}{C}\int I_1\,dt$

using Laplace transform, $V_B(s) = \frac{1}{SC} I_1(s)$

While $I_1(s) = \frac{V_{in}(s) - V_B(s)}{R}$

sub $I_1(s)$, then get

$$\therefore V_B(s) = \frac{V_{in}(s) - V_B(s)}{SCR}$$ ← sub $V_B(s)$

$$V_B(s)\left[1 + \frac{1}{SCR}\right] = \frac{V_{in}(s)}{SCR}$$

$$\therefore V_B(s) = \frac{V_{in}(s)}{SCR\left[1 + \frac{1}{SCR}\right]} = \frac{V_{in}(s)}{SC/R\left[\frac{SCR+1}{SC/R}\right]} = \frac{V_{in}(s)}{1+SCR}$$

$$\boxed{V_B(s) = \frac{V_{in}(s)}{1+SCR}}$$

from branch R_1, $I_2(s) = \frac{V_{in}(s) - V_A(s)}{R_1} = \frac{V_{in}(s) - V_B(s)}{R_1}$

from branch R_f, $I_2(s) = \frac{V_A(s) - V_o(s)}{R_f} = \frac{V_B(s) - V_o(s)}{R_f}$

$\{ \because V_A =$

$$\therefore \frac{V_{in}(s) - V_B(s)}{R_1} = \frac{V_B(s) - V_o(s)}{R_f}.$$

$$\frac{V_o(s)}{R_f} = V_B(s)\left[\frac{1}{R_1} + \frac{1}{R_f}\right] - \frac{V_{in}(s)}{R_1}. \longrightarrow (3)$$

Sub equ (2) in equ (3)

$$\frac{V_o(s)}{R_f} = \frac{V_{in}(s)}{1+sCR}\left[\frac{R_1+R_f}{R_1R_f}\right] - \frac{V_{in}(s)}{R_1}$$

$$V_o(s) = R_f\left\{V_{in}(s)\left[\frac{R_1+R_f}{R_1R_f}\left(\frac{1}{1+sCR}\right) - \frac{1}{R_1}\right]\right]$$

$$= V_{in}(s)\left[\frac{R_1+R_f}{R_1}\left[\frac{1}{1+sCR}\right] - \frac{R_f}{R_1}\right]$$

$$= V_{in}(s)\left\{1 + \frac{R_f}{R_1}\left(\frac{1}{1+sCR}\right) - \frac{R_f}{R_1}\right.$$

Select $R_f = R_1$

$$\therefore V_o(s) = V_{in}(s)\left[\frac{2}{1+sCR} - 1\right] = V_{in}(s)\left[\frac{2-1-sCR}{1+sCR}\right.$$

$$\frac{V_o(s)}{V_{in}(s)} \Rightarrow \frac{1-sCR}{1+sCR}$$

Put $s = j\omega$, $\therefore \frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{1-j\omega CR}{1+j\omega CR}$

$$\left|\frac{V_o(j\omega)}{V_{in}(j\omega)}\right| = \frac{\sqrt{1+\omega^2C^2R^2}}{\sqrt{1+\omega^2C^2R^2}} = 1 \quad \therefore |V_o| = |V_{in}|.$$

$$\phi = \angle\left[\frac{V_o(j\omega)}{\quad}\right] = -\tan^{-1}\left(\frac{\omega CR}{1}\right] - \tan^{-1}\left(\frac{\omega CR}{1}\right)$$

5

3

Voltage to Current Converter

It is also called Transconductance amplifier. accepts an i/p voltage V_i & yields an o/p current of the type $i_o = AV_i$.
where A - gain or sensitivity of the circuit, amps/V

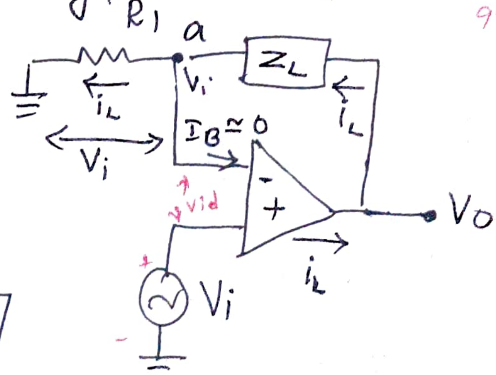
Two types of V to I Converter

Rₗ is not Connected ↑ Gnd

1. V-I Converter with floating load
2. V-I Converter with grounded load.
   ↳ One end of R_L is Connected to Gnd

V-I Converters with floating load [Current Series Negative FeedBack opamp)

Here, load resistor R_L is floating. ie R_L not connected to ground.



Since Voltage at node 'a' is V_i,

$\therefore V_i = i_L R_1 \quad \{as\ I_B = 0\}$

$i_L = \frac{V_i}{R_1}$ $\quad \boxed{\therefore I_L \propto V_i}$

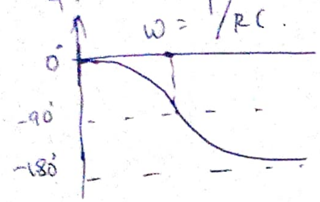
The same Current flows thro' the signal source & load
$\therefore$ Signal source should be capable of providing load I

Applications: Low voltage ac and dc voltmeters, Diode match finders, LED & zener diode Testing

Note:

If the load is a capacitor, it'll Charge or discharge at a constant rate. Hence such circuits are used to generate sawtooth or triangular waveforms. The proportionality const is $1/R_1$ & hence this circuit is Transconductance amplifier (or) Voltage Controlled Current Source (VCCS)

ϕ $\omega = 1/RC$

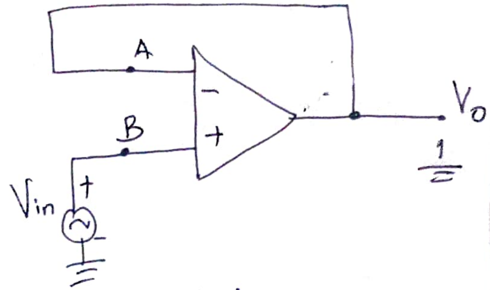


The angle ϕ is the phase shift introduced by the circuit as signal passes from i/p to o/p.

As ω varies from 0 to ∞, ϕ varies from 0° to −180°. Due to −ve sign, it is called phase lag.

Voltage Follower

A circuit in which the o/p voltage follows the i/p voltage is called voltage follower circuit.



From fig, Node B is at potential Vin

∴ Node A is also at potential Vin — ①

∴ $V_A = V_B = V_{in}$, since node A is directly connected to o/p, $V_o = V_A$ — ②

from eqn ① & ② $\boxed{\therefore V_o = V_{in}}$

Note:

This circuit is also called Source follower, Unity gain amplifier, buffer amp (or) isolation amp

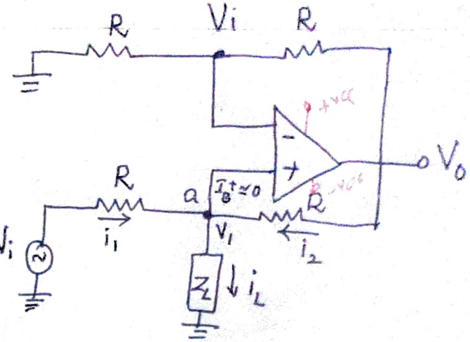
Adv:

1. Very large i/p R, (MΩ)
2. low o/p impedance, almost zero. Hence it is used to connect high Z source to low Z load, as buffer
3. Large BW

follows i/p without phase shift.

Voltage to Current Converter with Grounded load

Here, one end of load resistor R_L is grounded. It is also known as 'Howland Current Converter' from the name of its inventor.



Analysis:

Let V_1 be the voltage at node 'a'.

Apply KVL, we get $i_1 + i_2 = i_L$ (or)

① Step 1 Determine V_1

② Establish relationship b/t V_i and I_L

$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$V_i + V_o - 2V_1 = i_L R$$

$$\therefore V_1 = \frac{V_i + V_o - i_L R}{2} \quad \text{— ①}$$

Since op-amp is used in non-inverting mode, the gain of the circuit is $A = 1 + \frac{R_f}{R_1} = 1 + \frac{R}{R} = 2$

∴ o/p voltage is $\boxed{V_o = 2V_1}$

∴ from eqn ①, $V_o = V_i + V_o - i_L R$

$$V_i = i_L R$$

$$\boxed{i_L = \frac{V_i}{R}}$$

∴ load I depends on i/p V_i & Resistor R

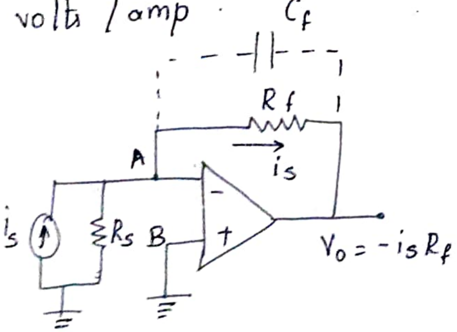
Adv: As i/p Z of non-inverting amplifier is very high this circuit has advantage of drawing very little current from source

Applications :

1. Low voltage dc voltmeter
2. Low voltage ac voltmeter
3. LED
4. Zener diode tester

Current to Voltage Converter

I - V converter, also called trans resistance amplifier, accepts an i/p current i_I & yields an o/p voltage of the type $V_o = Ai_L$, where A is the gain of circuit in volts / amp.



Analysis :

* Since (-) i/p terminal is at virtual ground, no I flows thro' Rs & current is flows thro' f/b resistor Rf.

* Hence $V_A = 0$, $i_s = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f}$

$\boxed{\therefore V_o = -i_s R_f}$ $\quad \therefore V_o \propto I_i$

Thus o/p V is proportional to i/p I.

* Lowest I that this circuit can measure will depend upon bias current I_B of op-amp. to reduce high frequency noise & possibility of oscillations R_f is shunted with C_f

ADDER [Inverting ADDER or summer]

$V_A = 0$

Now from I/p side, Apply KCL

$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1}$ —— (1)

$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2 - 0}{R_2} = \frac{V_2}{R_2}$ —— (2)

$I_3 = \frac{V_3 - V_0}{R_3} = \frac{V_3 - 0}{R_3} = \frac{V_3}{R_3}.$ —— (3)

Let $I = I_1 + I_2 + I_3$. [I/p side] —— (4)

From output side

$I = \frac{V_A - V_o}{R_f} = \frac{0 - V_o}{R_f} = -\frac{V_o}{R_f}$ —— (5)

Sub: (1), (2), (3), (5) in equation (4)

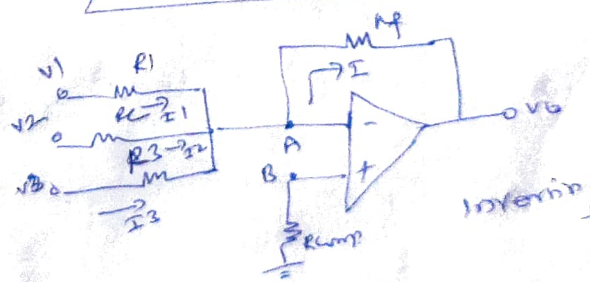
$$\frac{-V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right]$$

The Resistor $R_1 = R_2 = R_3 = R_f$

$$V_o = -\left[\frac{\cancel{R_1}}{\cancel{R_1}} V_1 + \frac{\cancel{R_f}}{\cancel{R_2}} V_2 + \frac{\cancel{R_f}}{\cancel{R_3}} V_3\right]$$

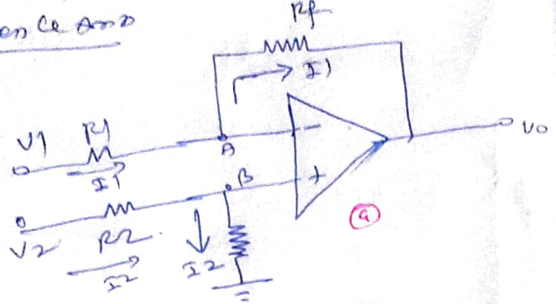
$$\boxed{V_o = -[V_1 + V_2 + V_3]}$$



Inverting Summing

SUBTRACTOR (or) Difference Amp

To find Relation between I/p and o/p Let us use Superposition principle



Assume

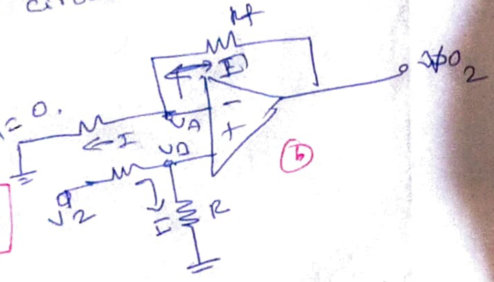
V_1 = acting, $V_2 = 0$, o/p is V_{o1} [Inverting Amp]

V_2 acting, $V_1 = 0$, o/p is V_{o2}

Case(i) with $V_2 = 0$, circuit act as inverting Amp.

Hence $\boxed{V_{o1} = -\frac{R_f}{R_1} \cdot V_1}$

Case ii with $V_1 = 0$, the circuit reduces to below (b)



Apply voltage Divider rule to the I/p V2 loop.

$$\boxed{V_B = \frac{R}{R_2+R} \cdot V_2} \quad \text{— (1)}$$

$$I = \frac{V_A}{R_1} = \frac{V_B}{R_1} \quad \text{— (2)}$$

and I = from o/p side $\frac{V_{o2}-V_A}{R_f} = \frac{V_{o2}-V_B}{R_f}$ — (3)

equate (2) and (3)

$$\frac{V_B}{R_1} = \frac{V_{o2}-V_B}{R_f} \quad \text{i.e}$$

$$\frac{V_B}{R_1} R_f = V_{o2} - V_B$$

$$\frac{V_B}{R_1} R_f + V_B = V_{o2}$$

$$\boxed{V_B\left[1+\frac{R_f}{R_1}\right] = V_{o2}} \quad (4)$$

Sub equation V_B in equation (4)

$$V_{o2} = \left[1+\frac{R_f}{R_1}\right]\left[\frac{R}{R_2+R}\right]V_2$$

Hence using superposition principle

$$\boxed{V_o = V_{o1}+V_{o2}}$$

$$= -\frac{R_f}{R_1}V_1 + \left[1+\frac{R_f}{R_1}\right]\left[\frac{R}{R_2+R}\right]V_2$$

if $R_1 = R_2$

$$= -\frac{R_f}{R_1}V_1 + \left[1+\frac{R_f}{R_1}\right]\left[\frac{R}{R_1+R}\right]V_2$$

$$= -\frac{R_f}{R_1}V_1 + \frac{R_f}{R_1}V_2, \quad \boxed{V_o = +\frac{R_f}{R_1}(V_2-V_1)}$$

Differential amplifier: (or) SUBTRACTOR (or) Difference Amp

[Que: Draw the differential amplifier and prove an expression for Common mode Rejection Ratio]

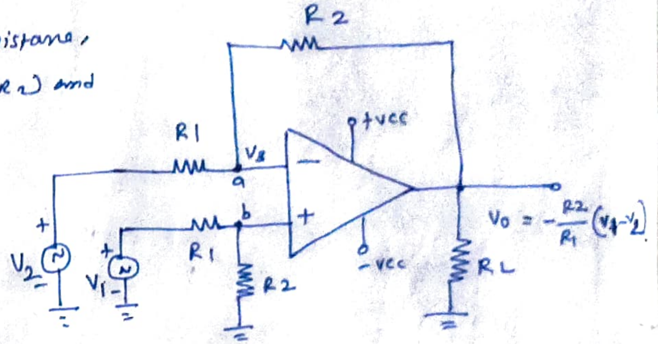
Definition: A circuit that amplifies the difference between two input signals is called a difference (or) differential amplifier.

Use: Used in instrumentation circuits and Industrial applications.

Significance: importance of differential amplifier is better able to reject common mode (noise) voltage than single I/p circuit &

Circuit consist of I/p resistance, feedback resistance (R_2) and Load Resistance R_L.

I/p are V_2 and V_1



Since, the differential voltage at the I/p terminals of the op-amp is zero, nodes 'a' and 'b' are at same potential, designated as V_3

The nodal equation at 'a' $\frac{V_3-V_2}{R_1}+\frac{V_3-V_o}{R_2}=0$ — (1)

$\frac{V_3}{R_1}-\frac{V_2}{R_1}+\frac{V_3}{R_2}-\frac{V_o}{R_2}=0$

" 'b' $\frac{V_3-V_1}{R_1}+\frac{V_3}{R_2}=0$ — (2)

Rearrange the equations (1) and (2)

$$\left[\frac{1}{R_1}+\frac{1}{R_2}\right]V_3 - \frac{V_2}{R_1} = \frac{V_o}{R_2} \quad \text{— (3)}$$

$$\left[\frac{1}{R_1}+\frac{1}{R_2}\right]V_3 - \frac{V_1}{R_1} = 0 \quad \text{— (4)}$$

Sub (3)-(4) $\left[\left(\frac{1}{R_1}+\frac{1}{R_2}\right)V_3 - \frac{V_2}{R_1}\right] - \left[\left(\frac{1}{R_1}+\frac{1}{R_2}\right)V_3 - \frac{V_1}{R_1}\right] = \frac{V_o}{R_2}$

$$\left(\frac{1}{R_1}+\cancel{\frac{1}{R_2}}\right)V_3 - \frac{V_2}{R_1} - \left(\frac{1}{R_1}+\cancel{\frac{1}{R_2}}\right)V_3 + \frac{V_1}{R_1} = \frac{V_o}{R_2}$$

$$\frac{1}{R_1}[V_1-V_2] = \frac{V_o}{R_2} \qquad \boxed{V_o = \frac{R_2}{R_1}[V_1-V_2]}$$

$$V_0 = \frac{R_2}{R_1}\left[V_1 - V_2\right]$$

$$\boxed{\text{voltage Gain } A_D = \frac{V_0}{V_1 - V_2} = \frac{R_2}{R_1}}$$

Conclusion:

These circuit useful for detecting very small difference in signals. since the gain R_2/R_1 can be chosen to be very large.

For example, if $R_2 = 100R_1$, then the small difference $V_1 - V_2$ is amplified 100 times.

Difference mode and Common mode gains

Let $V_0 = \frac{R_2}{R_1}\left[V_1 - V_2\right]$, if $V_1 = V_2$, the o/p $V_0 = 0$ for ideal op-amp only.

But pratical op-amp, $V_1 = V_2$, we wont get $V_0 = 0$ due to common mode component of I/p signal (voltage)

For example: V_0 will have different value

Case i) $V_1 = 100\mu V$, $V_2 = 50\mu V$

(ii) $V_1 = 1000\mu V$, $V_2 = 950\mu V$.

In Both the causes difference $[V_1 - V_2] = 50\mu V$ But output is different, due to average voltage of I/p signals. that is called Common mode signal.

$$V_{cm} = \frac{V_1 + V_2}{2}$$

$\frac{150}{2} = 75$

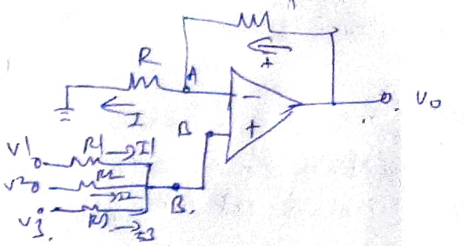
$\frac{1950}{2} = 975$

NOTE: (Important)

For the differential amp.

if $V_1 = V_2$, but voltage at node 'a' and 'b' are different because of ~~I/P~~ I/P Resistance at from V_2 source is $\cong R_1$ and from V_1 source is $\simeq (R_2 + R_3)$. The voltage at the positive terminal slightly grater than Negative terminal. So out is Not zero

Non-inverting ADDER



Let voltage of node B is VB.

Node A is at same potential as that of B, due to virtual ground.

$V_A = V_B$.

From I/P side

$I_1 = \frac{V_1 - V_B}{R_1}$ and $\frac{V_2 - V_B}{R_2}$

But I/p current of opamp is zero

$I_1 + I_2 = 0$.

$\frac{V_1 - V_B}{R_1} + \frac{V_2 - V_B}{R_2} = 0$, $\frac{V_1}{R_1} + \frac{V_2}{R_2} = V_B\left[\frac{1}{R_1} + \frac{1}{R_2}\right]$

$$\boxed{\therefore V_B = \frac{R_2 V_1 + R_1 V_2}{R_1 + R_2}} \quad —— (1)$$

Now at node 'A' $I = \frac{V_A}{R} = \frac{V_B}{R}$ as $V_B = V_A$ —— (2)

and through Rf

$I = \frac{V_0 - V_A}{R_f} = \frac{V_0 - V_B}{R_f}$ —— (3)

equate (2) and (3)

$\frac{V_B}{R} = \frac{V_0 - V_B}{R_f}$, $\frac{V_0}{R_f} = V_B\left[\frac{1}{R} + \frac{1}{R_f}\right]$.

$$\boxed{V_0 = V_B\frac{[R + R_f]}{R}} \quad —— (4).$$

sub: equation (1) in equation (4).

$$V_0 = \frac{R_2 V_1 + R_1 V_2}{(R_1 + R_2)} \frac{[R + R_f]}{R}.$$

$$V_0 = \frac{R_2(R + R_f)}{R(R_1 + R_2)} \cdot V_1 + \frac{R_1(R + R_f)}{R(R_1 + R_2)} V_2$$

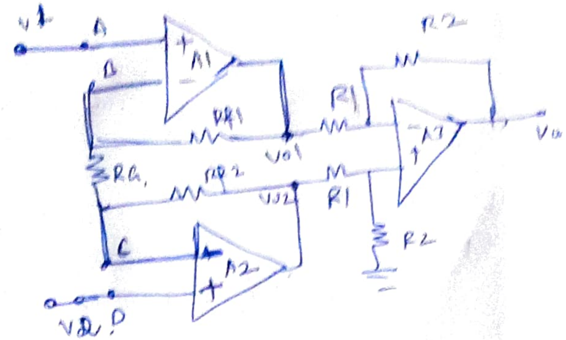
The o/p is weighted sum of I/Ps.

$R_1 = R_2 = R = R_f$ so $\boxed{V_0 = V_1 + V_2 + V_3}$

Instrumentation Amp

The node A potential of op-amp A1 is V_1 also at B is V_1

At node D is V_2 also at C is V_2



The o/p stage of Instrumentation amplifier is Difference Amp and o/p equ's given by

$$\boxed{V_o = \frac{R_2}{R_1}(V_{o2} - V_{o1})}$$

Applying ohms Law: between E and F

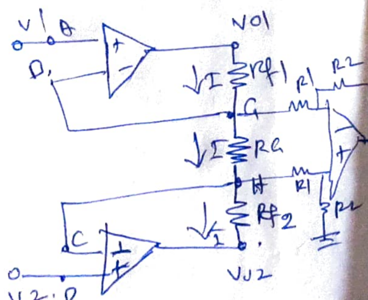
$$I = \frac{V_{o1} - V_{o2}}{R_{f1} + R_G + R_{f2}}$$

$R_{f1} = R_{f2} = R_f$

$$I = \frac{V_{o1} - V_{o2}}{2R_f + R_G} \quad \text{——— (1)}$$

At node G and H.

$$I = \frac{V_G - V_H}{R_G} = \frac{V_1 - V_2}{R_G} \quad \text{——— (2)}$$



equate (1) and (2)

$$\frac{V_{o1} - V_{o2}}{2R_f + R_G} = \frac{V_2 - V_1}{R_G}$$

$$\frac{V_{o2} - V_{o1}}{2R_f + R_G} = \frac{V_1 - V_2}{R_G}$$

$$V_{o2} - V_{o1} = \frac{(2R_f + R_G)(V_2 - V_1)}{R_G}$$

$$V_o = \frac{R_2}{R_1}\left[\frac{2R_f + R_G}{R_G}\right](V_2 - V_1)$$

$$\boxed{V_o = \frac{R_2}{R_1}\left(1 + \frac{2R_f}{R_G}\right)(V_2 - V_1)}$$

Advantages

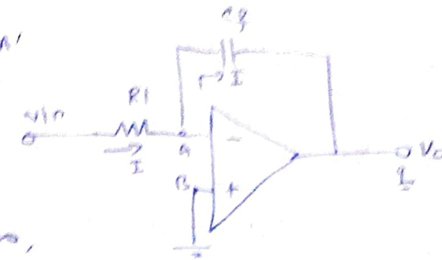
1) Half of R_G gain can be easily varied
2) I/p impedance is high
3) High CMRR

Integrator

o/p voltage is the integration of the input voltage

Ideal Active op-amp integrator

The node B is grounded, Node A also grounded due to virtual ground



Ideal op-amp integrator

$$\therefore V_A = V_B = 0$$

As I/p current of op-amp is zero, the entire current I flowing through R_1, also flows through C_f

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1} \quad \text{——— (1)}$$

From output side, we can write

$$I = C_f \frac{d(V_A - V_o)}{dt} \quad \text{——— (2)}$$

$$I = -C_f \frac{dV_o}{dt} \quad \text{——— (2)}$$

equating (1) and (2),

$$\frac{V_{in}}{R_1} = -C_f \frac{dV_o}{dt}$$

Integrating both the sides, we get

$$\int_0^t \frac{V_{in}}{R_1}\,dt = -C_f \int \frac{dV_o}{dt}\,dt$$

ie $$\int_0^t \frac{V_{in}}{R_1}\,dt = -C_f V_o$$

$$\boxed{\therefore V_o = -\frac{1}{R_1 C_f}\int_0^t V_{in}\,dt + V_o(0)} \quad \text{——— (3)}$$

Where $V_o(0)$ is the initial constant of integration, indicating the initial output voltage

The o/p is $-1/R_1C_f$ times the integral of I/p and R_1C_f is called time constant

The Negative sign indicates phase shift of 180° between input and output.

Advantage

Large Time constant

By Miller's theorem the effective capacitance between input terminal A and the ground becomes

$$C_f(1 - A_V)$$

'A' is gain of opamp which is very Large!

Due to large effective capacitance, time constant is very Large and thus a perfect integration results due to this circuit.

$R_{comp} = R_1$ provides Bias compensation

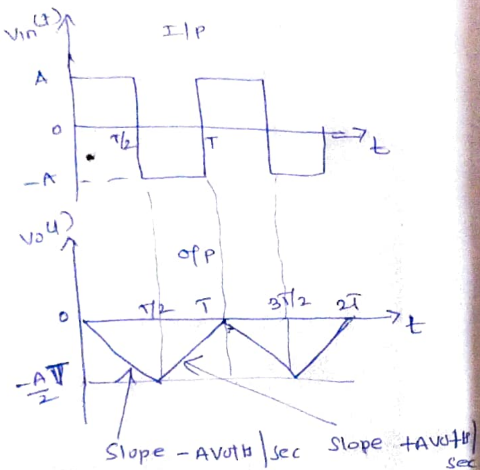
For square wave I/P (integrator)

$V_{in}(t) = A \quad 0 < t < T/2$

$\quad = -A, \; T/2 < t < T$

$V_o(t) = -A \quad 0 < t < T/2$

$\quad +A \quad T/2 < t < t$



For sine wave I/P

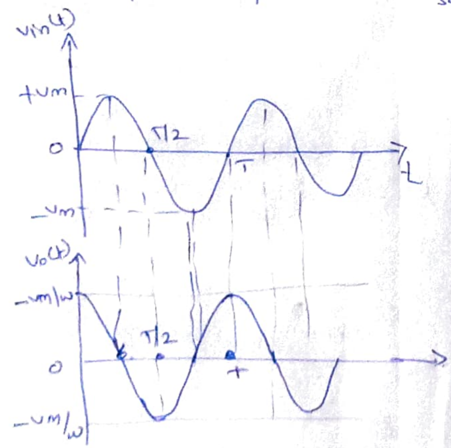
$V_{in}(t) = V_m \sin \omega t$

$V_o(t) = -\int v_{in} dt$

$= -\int V_m \sin \omega t \, dt$

$= -V_m \left[\frac{1}{\omega}(-\cos \omega t)\right]$

$$\boxed{V_o(t) = -\frac{V_m}{\omega}(-\cos \omega t)}$$

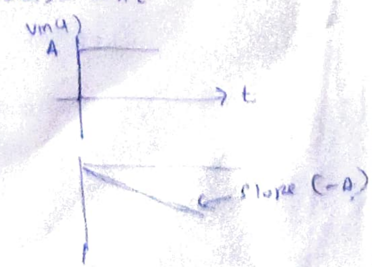


NOTE For step I/P

$V_{in}(t) = A \text{ for } t > 0$

$\quad 0 \text{ for } t < 0$

$V_o(t) = -At$



Errors in an Ideal Integrator

In absence of I/P voltage or at zero frequency (dc), op-amp gain is very high. The I/P offset voltage gets amplified and appears at the o/p as an error voltage. The bias currents also results in a capacitor charging current and adds its effect in a o/p error vge.

* ~~The~~ Depending on polarities of offset voltage and/or bias current o/p to ramp up or down. After some time o/p goes to saturation level due to these two errors. Very difficult to pull opamp out of saturation.

of I/P offset voltage amplified at o/p
error due to bias current

NOTE

① In ideal integrator, absence of I/P, due to offset voltage o/p goes to negative or positive saturation level.

In presence of I/P voltage also, o/p of opamp get distorted ~~we~~ due to I/P offset voltage and bias current. We won't get true integration o/p.

② BW is very small. So it can be used for a very small frequency range of I/P only.

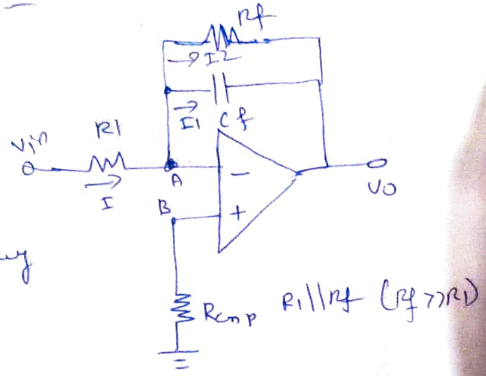
Due to above limitations, an ideal integrator not used in practice, so we go for practical integrator.

Pratical Integrator

→ R_f parallel with C_f

→ R_{comp} is also used to overcome the error due to the bias current

→ R_f reduces the low frequency gain of opamp.



Analysis:

As the I/P current of op-amp is zero, the node B is still at ground potential, Hence the node A also in ground potential

$V_A = V_B = 0$

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1}$$

$$I_1 = C_f \frac{d(V_A - V_o)}{dt} = -C_f \frac{dv_o}{dt} \quad \text{—(1)}$$

and

$$I_2 = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f} \quad \text{—(2)}$$

At node A, applying KCL,

$I = I_1 + I_2$

$$\frac{v_{in}}{R_1} = -C_f \frac{dv_o}{dt} - \frac{v_o}{R_f}$$

Taking laplace, we get

$$\frac{V_{in}(s)}{R_1} = -sC_f V_o(s) - \frac{V_o(s)}{R_f}$$

$$\frac{V_{in}(s)}{R_1} = -V_o(s)\left[sC_f + \frac{1}{R_f}\right]$$

$$\frac{V_{in}(s)}{R_1} = \frac{-V_o(s)[1 + sC_fR_f]}{R_f}$$

$$\therefore V_o(s) = -\frac{R_f}{R_1[1 + sC_fR_f]} \cdot V_{in}(s) \quad (3)$$

$\div R_f$

$$\therefore V_o(s) = -\frac{1}{\left(sR_1C_f + \frac{R_1}{R_f}\right)} \cdot V_{in}(s)$$

When R_f is very large than R_1/R_f can be neglected and hence circuit behave like an ideal integrator

$$V_o(s) = -\frac{1}{sR_1C_f} V_{in}(s).$$

$$\boxed{\text{ie } V_o(t) = -\frac{1}{R_1C_f}\int V_{in}(t)\,dt}$$

as $\frac{1}{s} = \int dt$ →(4).

Frequency Response of pratical Integrator

Frequency response of pratical integrator: To Derive FR bring gain as a function of frequency

Let take

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_f/R_1}{1 + sC_fR_f}$$

put $s = j\omega$

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-R_f/R_1}{1 + j\omega C_fR_f}$$

$$\therefore A = -\frac{R_f/R_1}{1 + j2\pi f C_f R_f} = \text{gain as function of frequency)}$$

$$A = \frac{R_f/R_1}{1 + j\frac{f}{f_a}}$$

Where $f_a = \frac{1}{2\pi C_f R_f}$

f_a is corner frequency

The Magnitude of the gain A is given by

$$\boxed{|A| = \frac{R_f/R_1}{\sqrt{1 + \left(\frac{f}{f_a}\right)^2}}}$$

At $f = 0$ ie dc condition

$|A| = R_f/R_1$

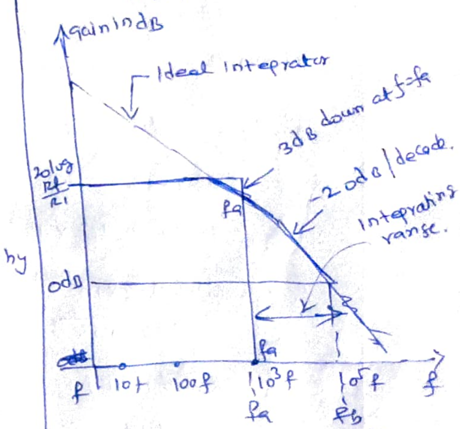
$= 20\log\left(\frac{R_f}{R_1}\right)$ dB.

Thus infinite dc gain of opamp in case of ideal, gets limited to R_f/R_1 in the pratical integrator.

if $f = f_a$.

$$|A| = \frac{R_f/R_1}{\sqrt{1+1}} = 0.707\frac{R_f}{R_1}$$

ie $20\log|A| = -3\text{dB} + \text{dc gain}$.



$f = f_a$ magnitude of gain drops by 3dB.

For integration frequency response must be straight line slope, it occur between f_a and f_b. So integration taking place between f_a and f_b below f_a does not integrate

Designe pratical integrator ckt with a dc gain of 10, to integrate a square wave of 10 KHZ.

Given

$|A|_{dc} = \frac{R_f}{R_1}$ &

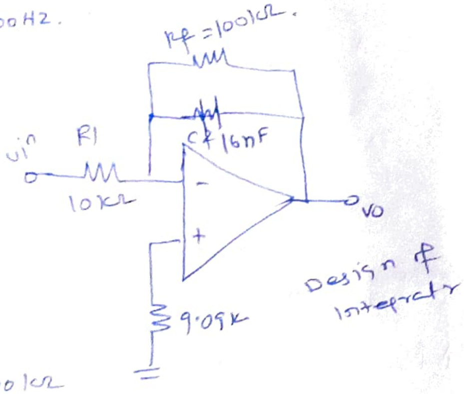
$10 = \frac{R_f}{R_1}$

$f = 10KHz$.

For proper integration $f \geq 10 f_a$

$\frac{f}{f_a} = 10$.

$f_a = \frac{f}{10} = \frac{10 \times 10^3}{10} = 1000Hz$.



Design of integrator

For pratical integrator

$f_a = \frac{1}{2\pi R_f C_f}$

$1000 Hz = \frac{1}{2\pi R_f C_f}$.

$\therefore R_f C_f = 1.5915 \times 10^{-4}$

Choose $R_1 = 10k\Omega$

$R_f = 10 R_1 = 10 \times 10^3 = 100k\Omega$

$C_f = \frac{1.5915 \times 10^{-4}}{100 \times 10^3} = 16nF$

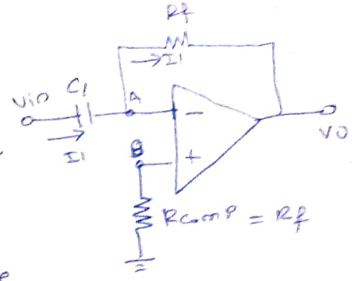
$R_{comp} = R_1 || R_f$

$= \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 100}{10 + 100} = 9.09k\Omega$

Differentiator

The circuit which produces the differentiation of the input voltage at its output is called differentiator.

Ideal opamp differentiator



From circut node 'B' is grounded so $V_A = 0$

As i/p current of opamp is zero, entire current I_1 flows through resistance R_f.

Analysis:

From input side, we can write

$I_1 = C_1 \frac{d(v_{in} - V_A)}{dt} = C_1 \frac{dv_{in}}{dt}$ —① $\boxed{V_A = 0}$

From output side, we can write

$I = \frac{(V_A - V_o)}{R_f} = -\frac{V_o}{R_f}$ —②

equate ① and ②

$C_1 \frac{dv_{in}}{dt} = \frac{-V_o}{R_f}$, $\boxed{V_o = -C_1 R_f \frac{dv_{in}}{dt}}$ —③

Equation ③ ie output shows the output is $C_1 R_f$ times the differentiation of input.

$\boxed{C_1 R_f \text{ is called time constant}}$

'—' sign in output equation indicates there is a 180° phase shift between input and output

By miller's theorem, the effective resistance between input node 'A' and ground becomes

$\frac{R_f}{1 + A_V} \simeq \frac{R_f}{A_V}$, A_v = gain, which is a very large

So R_f become very small and hence the condition $R_f C_1 << T$ get satisfied at all the frequencies.

Choose: $\boxed{\text{In practice } R_{comp} = R_f}$

For sine wave I/P

Let chose Vin is sine waveform

Let $V_o(t) = -\frac{dV_{in}(t)}{dt}$

For $R_fC_f = 1$ $= -\frac{d}{dt}(V_m \sin \omega t)$

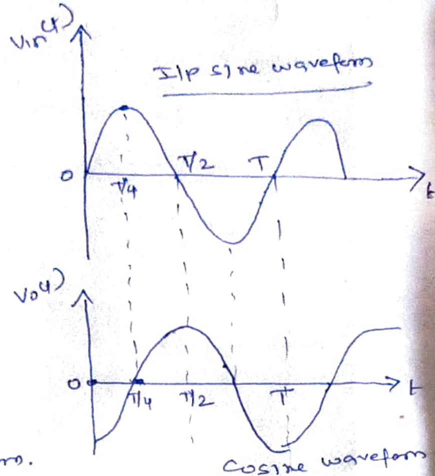
$V_o(t) = -V_m \cos\omega t \cdot \omega$

So at $t = 0$ $V_o(t) = -V_m\omega$

$t = T/4$ $V_o(t) = 0$

$t = T/2$ $V_o(t) = +V_m\omega$ and so on.

So o/p of differentiator is cosine waveform.

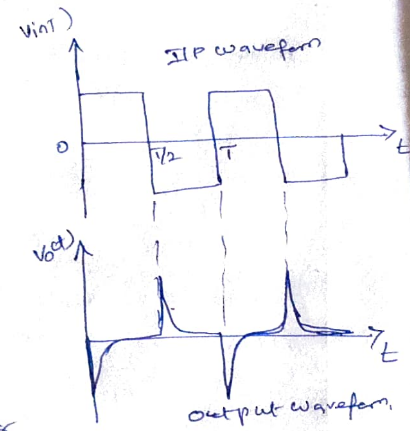


For square wave I/P

$V_{in}(t) = A \quad 0 < t < T/2$

$\qquad\quad -A \quad T/2 < t < T$

Differentiator behave similar to its step input. So total o/p for square wave input is in the form of train of impulses or spikes.



Frequency Response of ideal differentiator

Let $V_o(t) = -R_fC_1 \frac{dv_{in}}{dt}$

Taking Laplace Transform

$V_o(s) = -sR_fC_1 V_{in}(s)$

To get Frequency Response, Replace $s = j\omega$

$V_o(j\omega) = -j\omega R_fC_1 V_{in}(j\omega)$

Gain $= \frac{V_o(j\omega)}{V_{in}(j\omega)} = -j\omega R_fC_1$

To get frequency Response, take magnitude of gain.

$A = \left|\frac{V_o(j\omega)}{V_{in}(j\omega)}\right| = |-j\omega R_fC_1|$

$A = \omega R_fC_1 = 2\pi f R_fC_1$

for Low frequency such as dc ($f = 0$) so gain $= 0$. If and frequency increases gain also increases.

$\boxed{A = \frac{f}{f_a}}$, $f_a = \frac{1}{2\pi R_fC_1}$

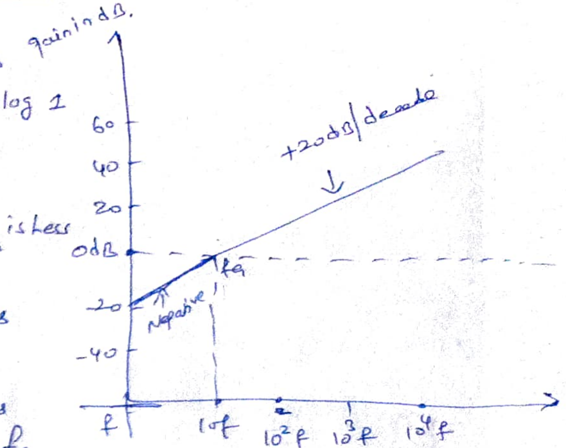
Frequency Response of ideal differentiator

f_a is the frequency at which gain becomes 1 or $20\log 1$ ie 0dB

$\boxed{f < f_a}$, the ratio of f/f_a is less than unity.

Hence $20\log(f/f_a)$ is Negative

if $f = f_a$, gain becomes 0dB and frequencies f_a onwards, gain increases with a rate of 20dB/decade.



Disadvantages of an Ideal differentiator

* The gain of the differentiator increases as frequency increases. at some high frequency, it may become unstable and break into ~~saturation~~ the oscillations. There is a possibility that opamp may go to into saturation.

* $X_{C1} = \frac{1}{2\pi f C_1}$, if frequency increases, Reactance of capacitance decreases. This makes circuit is very much sensitive to noise. At high frequency noise get amplified due to high gain. So noise completely overrides the differentiated output.

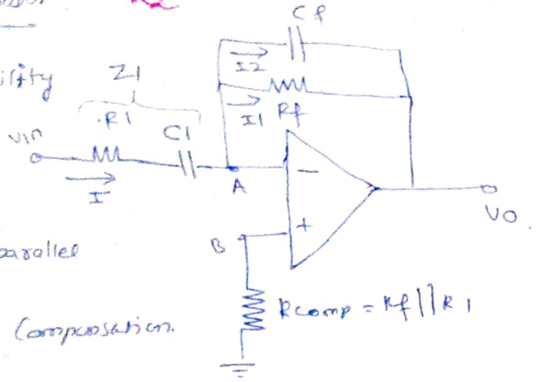
Limitation

Circuit suffers on its instability and noise problems, at high frequencies. This can be corrected by adding some additional parameter. Such a circuit is called practical differentiator.

Practical Differentiator

The noise and stability at high frequency can be corrected, using R_1 series with C_1 and C_f parallel with R_f.

R_{comp} used for Bias Compensation.



Analysis:

As the op amp input current is zero there is no current at 'B' due to ground

so $V_B = 0$, $V_A = 0$

From input side, current I, we can write

$$I = \frac{V_{in} - V_A}{Z_1} = \frac{V_{in}}{Z_1}$$

where $Z_1 = R_1$ in series with C_1

Take Laplace transform

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{1+sR_1C_1}{sC_1}$$

$$\therefore I = \frac{V_{in}}{Z_1} = \frac{sC_1 V_{in}(s)}{(1+sR_1C_1)} \quad \text{—(1)}$$

Now current I_1 is

$$I_1 = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f}$$

Laplace

$$I_1 = \frac{-V_o(s)}{R_f} \quad \text{—(2)}$$

Now current I_2 is

$$I_2 = C_f \frac{d(V_A - V_o)}{dt} = -C_f \frac{dv_o}{dt}$$

Laplace

$$I_2 = -sC_f V_o(s) \quad \text{—(3)}$$

Apply KCL at Node 'A'

$$I = I_1 + I_2$$

$$\frac{sC_1 V_{in}(s)}{(1+sR_1C_1)} = \frac{-V_o(s)}{R_f} + (-C_f V_o(s))$$

$$= \frac{-V_o(s)}{R_f} - C_f V_o(s)$$

$$\frac{sC_1 V_{in}(s)}{(1+sR_1C_1)} = -V_o(s)\left[\frac{1+sR_fC_f}{R_f}\right]$$

$$-V_o(s) = \frac{\dfrac{sC_1 V_{in}(s)}{(1+sR_1C_1)}}{\dfrac{1+sR_fC_f}{R_f}}$$

then

$$V_o(s) = \frac{-sR_fC_1V_{in}(s)}{(1+sR_fC_1)(1+sR_1C_1)}$$

if $R_fC_f = R_1C_1$, then

$$V_o(s) = \frac{-sR_fC_1V_{in}(s)}{(1+sR_1C_1)^2} \quad \text{—(4)}$$

The time constant R_fC_1 is much greater than R_1C_1 or R_fC_f and hence equation (4) becomes reduced to

$$V_o(s) = -sR_fC_1 V_{in}(s)$$

i.e. $V_o(t) = -R_fC_1 \dfrac{d\,v_{in}(t)}{dt}$ $\quad \left[s = \dfrac{d}{dt}\right]$

The output voltage R_fC_1 times the differentiation of I/P.

Frequency Response of practical differentiator

To determine frequency response, let us obtain gain in terms of frequency.

Let $V_o(s) = \dfrac{-sR_fC_1V_{in}(s)}{(1+sR_1C_1)^2}$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{-sR_fC_1}{(1+sR_1C_1)^2}$$

$s = j\omega$

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-j\omega R_fC_1}{(1+j\omega R_1C_1)^2}$$

$\omega = 2\pi f$

$$\frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-j2\pi f R_fC_1}{(1+j2\pi f R_1C_1)^2}$$

Now Let

$$f_b = \frac{1}{2\pi R_1C_1}$$

$$f_a = \frac{1}{2\pi R_fC_1}$$

$$\therefore \frac{V_o(j\omega)}{V_{in}(j\omega)} = \frac{-j\left[\frac{f}{f_a}\right]}{\left[1+j\frac{f}{f_b}\right]^2}$$

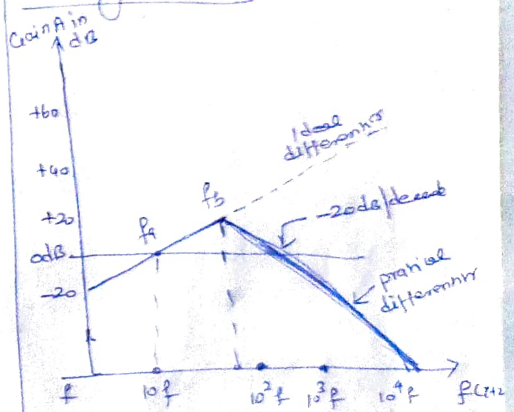
$$A = \left|\frac{V_o(j\omega)}{V_{in}(j\omega)}\right| = \frac{\left(\frac{f}{f_a}\right)}{\left[\sqrt{1+\left(\frac{f}{f_b}\right)^2}\right]^2}$$

$$\therefore A = \frac{f/f_a}{1+\left(\frac{f}{f_b}\right)^2}$$

Now as $R_fC_1 \gg R_1C_1$, we can write

$$f_a < f_b$$

Frequency Response



$f \uparrow$ gain $\uparrow$ till $f = f_b$ at a rate of +20dB decade

After f_b gain decrease at a rate of 20dB/decade, change at $f = f_b$ occurs due to the combination of R_1C_1 and R_fC_f

So for $R_1f_1 \ll T$, the true differentiation results occurs.

Conclusion

$f > f_b$, gain reduces, Hence the problem of instability at high frequency get eliminated.

Note

f_c is unity at gain 0dB so $f < f_b < f_c$

Design of practical differentiator

1) Choose f_a as the highest frequency of the I/p signal
2) Choose C_1 to be less than 1μf and calculate R_f
3) Choose f_b as 10 times of f_a, which ensure that $f_a < f_b$
4) Calculate R_1 and C_f from $R_1C_1 = R_fC_f$
5) $R_{comp} = R_1 \| R_f$ but practically almost $R_{comp} = R_1$

Applications

① wave shaping circuit to ~~decect~~ detect high frequency components in the I/p signal

② As a rate-of-change detector in the FM demodulators.

Design a practical differentiator circuit that will differentiate an input signal with the $f_{max} = 150\,Hz$

(i) $f_a = f_{max} = 150\,Hz$

(ii) choose $C_1 = 1\mu f$ (or Less than 1μf)

$$f_a = \frac{1}{2\pi R_f C_1}$$

$$150 = \frac{1}{2\pi R_f \, 1\times10^{-6}}$$

$$\boxed{R_f = 1.06k\Omega}$$

(iii) $f_b = 10 f_a = 10\times150 = 1500\,Hz$

AND $R_1C_1 = R_fC_f$

$$f_b = \frac{1}{2\pi R_1 C_1}$$

$$1500 = \frac{1}{2\pi R_1 \, 1\times10^{-6}}$$

$$\boxed{R_1 = 106.1\,\Omega}$$

Find C_f

Let $R_1C_1 = R_fC_f$

$$106.1 \times 1\times10^{-6} = 1.06\times10^{3}\, C_f$$

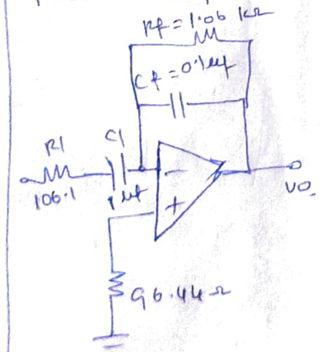
$$\boxed{0.1\mu f = C_f}$$

$$R_{comp} = R_1 \| R_f = \frac{R_1R_f}{R_1+R_f}$$

$$= \frac{106.1 \times 1.06\times10^{3}}{106.1 + 1.06\times10^{3}}$$

$$= 96.44\,\Omega$$

Select $R_{comp} = R_1$ for practical integrator



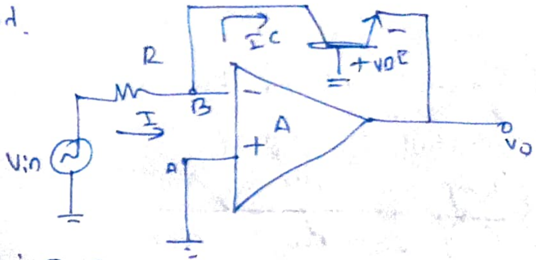
Basic Logarithmic Amplifier

O/p is proportional to the logarithm of the I/p voltage Vin

It is obtained by using a transistor as a diode in the Negative feed back path of an op-amp.

A node B is virtual ground.

hence $V_B = 0$



$$\therefore I = \frac{V_{in} - V_B}{R} = \frac{V_{in}}{R} \quad \text{—①}$$

an opamp input current is zero

$$I = I_C$$

The Voltage $V_{CB} = 0$ as the collector is at virtual ground and base is grounded, Hence we can write the equation I_C as

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \quad I_S = \text{Saturation current} \quad \text{—②}$$

Applying to the o/p side we get

$$V_O + V_{BE} = 0.$$

ie $V_O = -V_{BE}$ and $I_C = I = \frac{V_{in}}{R}$. , sub I_C in equ ②

$$\boxed{-V_O = V_T \ln\left(\frac{V_{in}}{RI_S}\right)}$$

Let $V_{ref} = I_S R$

$$\boxed{V_O = -V_T \ln\left[\frac{V_{in}}{V_{ref}}\right]}$$

O/p is directly proportional to the log of the I/p voltage.

Disadvantages

1. I_0 (Reverse sat current changes with Temp) every 10°C - it is double. $V_T = kT$

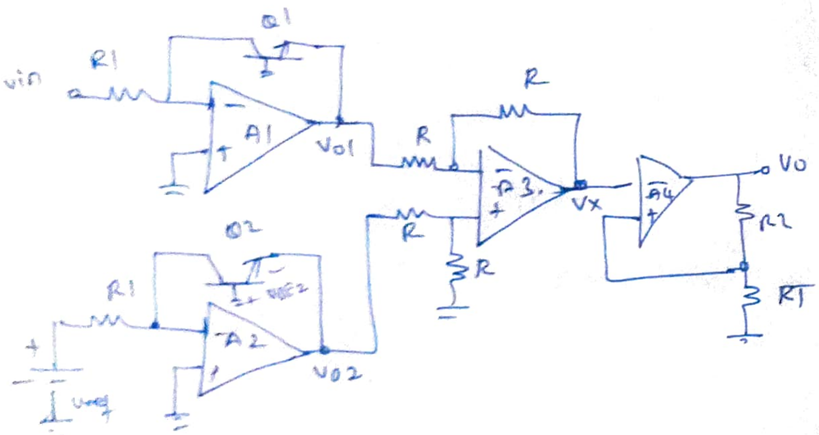
2. very difficulty to set the term V_{ref} for the ckt

3. The term V_T which is kT also changes with Temp.

so Temp affects the perfomce and accury of Basic log amp. so we have to put some sort of compensation circuit.

Temp Compensated log Amplifier

It uses two log Amp one for vin another for Vref



Q1 and Q2 are identical. A1 and A2 work as basic log amp

$I_{s1} = I_{s2} = I_s$.

then $V_{o1} = -V_T \ln\left(\frac{V_{in}}{R_1 I_s}\right)$

$V_{o2} = -V_T \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$.

A_3 act as difference amp with unity gain

so $V_x = V_{o2} - V_{o1}$

$$V_x = -V_T \ln\left[\frac{V_{ref}}{R_1 I_s}\right] - \left[-V_T \ln\left[\frac{V_{in}}{R_1 I_s}\right]\right]$$

$$= -V_T\left[\ln\left(\frac{V_{ref}}{R_1}\right) - \cancel{\ln(I_s)} - \ln\left(\frac{V_{in}}{R_1}\right) + \cancel{\ln(I_s)}\right]$$

$$\boxed{V_x = -V_T \ln\left(\frac{V_{ref}}{V_{in}}\right)}$$

Absorbing -ve sign

$$V_x = V_T \ln\left(\frac{V_{in}}{V_{ref}}\right)$$

NOTE

V_{ref} is decided by external battry and it's not temp depended and Temp dependent compont I_s get cancelled out.

Since V_T is presed in V_x which depend on temperature, this is compensated by Last stage of op-amp A4

$$V_o = V_x\left[1 + \frac{R_2}{R_T}\right]$$

$$V_o = V_T \ln\left(\frac{V_{in}}{V_{ref}}\right) \cdot \left(1 + \frac{R_2}{R_T}\right)$$

$$V_o = \frac{V_T (R_2 + R_T)}{R_T} \ln\left(\frac{V_{in}}{V_{ref}}\right)$$

As Temp changes VT changes but the same time RT also changes, so that ratio $V_T (R_2 + R_T)/R_T$ remains constant

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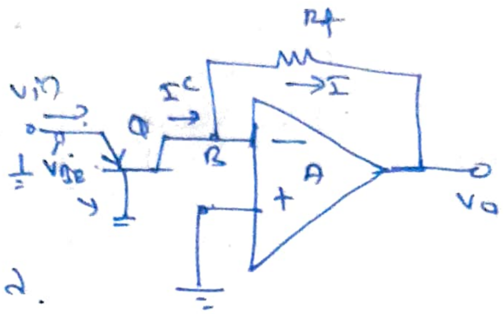
Antilog amp : Antilog of I/P can be obtained by using transistor

obtaining by connecting transistor at I/P terminal of op-amp.



Node B at virtual ground

hence VD = 0

Collector and base of Q are at ground potential and VCB = 0

$$I_C = I_s e^{V_{BE}/V_T} \quad \text{—①}$$

By $V_{BE} = V_{in}$

$$I_C = I_s e^{V_{in}/V_T} \quad \text{—②}$$

Now Ic and I are same as op-amp input current is zero

$$I = I_C = \frac{V_B - V_o}{R_f} = \frac{-V_o}{R_f} \quad \text{—③}$$

$\frac{0 - V_o}{R_f} = \frac{V_o}{R_f}$

Due to virtual gnd $V_B = 0$

equate ② and ③ i.e. IC

$$\frac{-V_o}{R_f} = I_s e^{V_{in}/V_T}$$

$$V_o = -I_s R_f e^{V_{in}/V_T}$$

Assume $I_s R_f = V_{ref}$

$$\boxed{V_o = V_{ref} e^{V_{in}/\eta V_T}}$$

o/p voltage is proportional to the exponential of vin.

i.e. antilog of vin

since Io Is and VT are present in the o/p equation all are function of Temperature. so temp changes, parameters changes and cause serie problems.

Temp Compensated Antilog Amp

The log Amp can be turned around to provide antilog or exponential function called Antilog 'A'

Both are identical Transistor.

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_S}\right) \quad (1)$$

$$V_{BE2} = V_T \ln\left(\frac{I_{C2}}{I_S}\right) \quad (2)$$

As opamp currents are zero

$$I_{C1} = I_1 = \frac{V_O - V_B}{R_1} = \frac{V_O}{R_1} \quad (3)$$

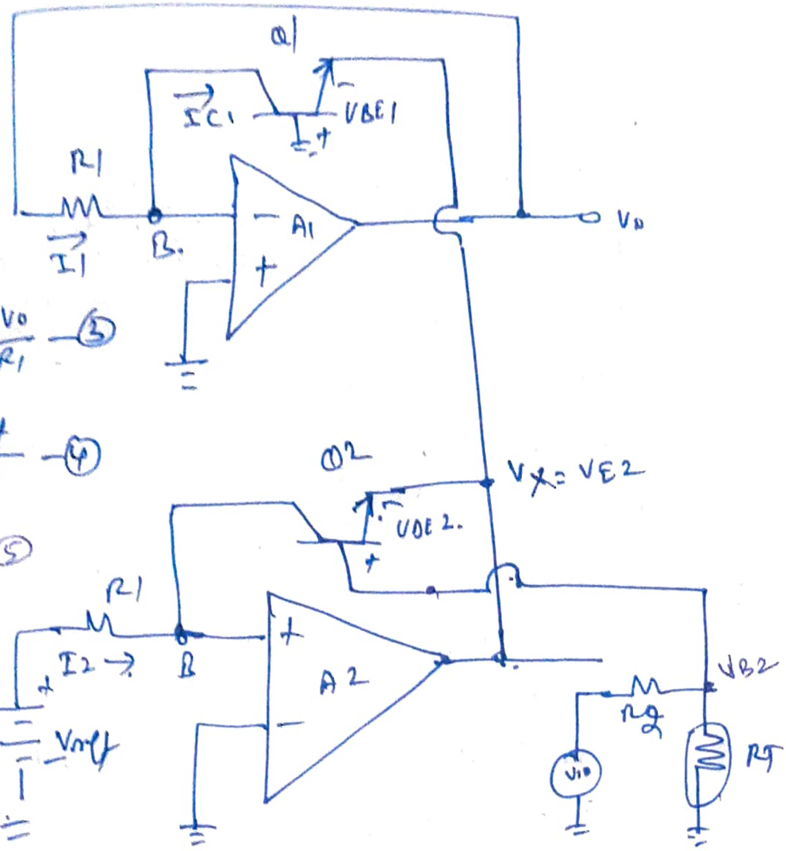
$$I_{C2} = I_2 = \frac{V_{ref} - V_B}{R_1} = \frac{V_{ref}}{R_1} \quad (4)$$

(3) in (1)

$$V_{BE1} = V_T \ln\left(\frac{V_O}{I_S R_1}\right) \quad (5)$$

(4) in (2)

$$V_{BE2} = V_T \ln\left(\frac{V_{ref}}{I_S R_1}\right) \quad (5)$$



Now the voltage V_x is

$$V_x = -V_{BE1} \xrightarrow{\text{Sub } V_{BE} \text{ equation here ie (5)}} = -V_T \ln\left(\frac{V_O}{I_S R_1}\right)$$

$$V_{B2} = V_{in}\left[\frac{R_T}{R_2 + R_T}\right] \quad (6)$$

Now for the transistor Q2, we can write.

$$V_{B2} = V_{E2} + V_{BE2} \quad (7)$$

Sub eq (6) (5) in (7)

$$V_{in}\left[\frac{R_T}{R_2+R_T}\right] = V_x + V_T \ln\left(\frac{V_{ref}}{I_S R_1}\right)$$

$$V_{in}\left[\frac{R_T}{R_2+R_T}\right] = -V_T \ln\left[\frac{V_O}{I_S R_1}\right] + V_T \ln\left[\frac{V_{ref}}{I_S R_1}\right]$$

$$= -V_T\left[\ln\left(\frac{V_O}{R_1}\right) - \cancel{\ln(I_S)} - \ln\left[\frac{V_{ref}}{R_1}\right] + \cancel{\ln(I_S)}\right]$$

$$\therefore V_{in}\left[\frac{R_T}{R_2+R_T}\right] = \boxed{-V_T \ln \frac{V_O}{V_{ref}}}$$

$$\ln\left(\frac{V_O}{V_{ref}}\right) = \frac{-V_{in} R_T}{V_T (R_2+R_T)}, \quad V_O = V_{ref} \ln^{-1}\left[\frac{-V_{in} R_T}{V_T (R_2+R_T)}\right]$$

o/p $\propto$ antilog ($\ln^{-1}$) of i/p, the term $R_T / V_T(R_2+R_T)$ is Constant //

Analog multiplier :

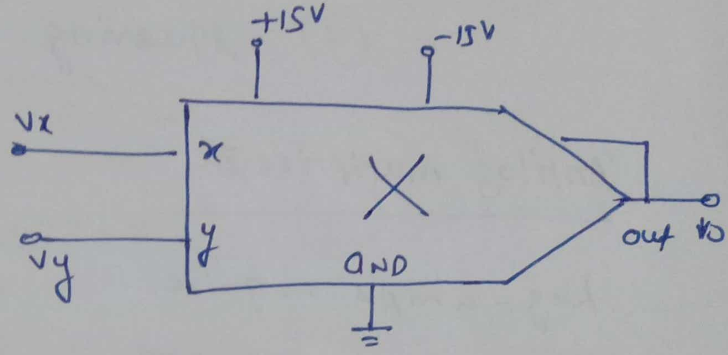
What is analog multiplier?

A circuit which performs multiplication of two analog voltages is called as Analog multiplier. The o/p is the product of the two inputs divided by a reference voltage V_{ref}. The o/p is & called version of x and y inputs.

$$V_o = \frac{V_x V_y}{V_{ref}}$$

Normaly V_{ref} is internally set to 10 volts

$$\text{So } V_o = \frac{V_x V_y}{10}.$$



Schematic symbol, Multiplier

as long as.

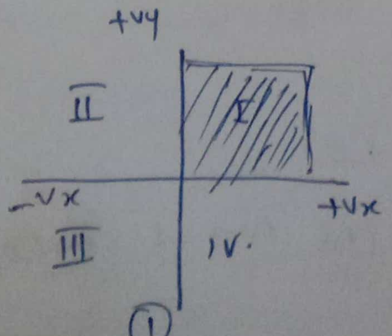
and $V_x < V_{ref}$, $V_y < V_{ref}$ } The o/p of multiplier will not saturate.

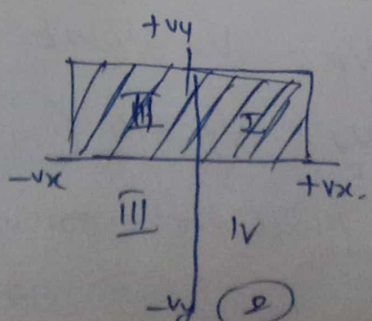
Modes of operation

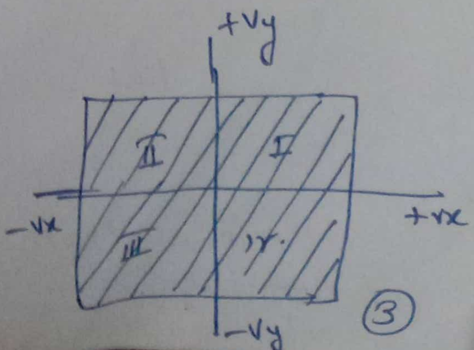
① One quardrant multiplication : Both the I/p are positive

② Two Quardant multiplication : One I/p is held positive and the other is allowed to ~~switch~~ swing Both +ve and Negative

③ Four quardrant multiplier: If both the I/ps may be either +ve or −ve





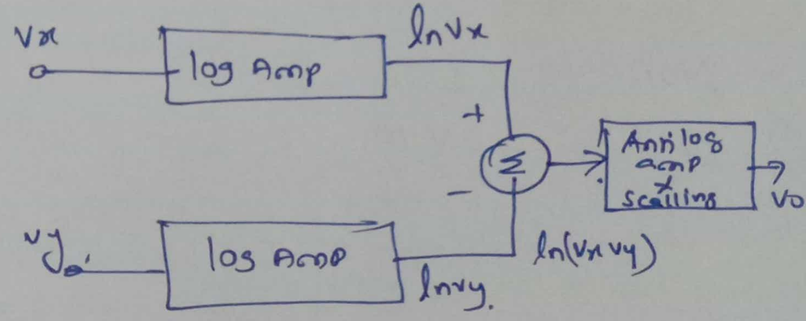


Applications: ① frequency doubling ② Measurement of real power ③ detecting phase-angle difference between two signals of equal frequency.
④ Multiplying two signals
⑤ Dividing one signal by another
⑥ Square root of a signal
⑦ squaring a signal.

Analog multiplier Applications

Antilog multiplier IC

Log-amps require the I/P and reference voltages to be same polarity. This restricts log-antilog multipliers to one quadrant operation



$$\boxed{\ln V_x + \ln V_y = \ln (V_x V_y)}$$

Frequency Doubling:

The multiplication of two sine waves of the same frequency, but of possibly different amplitude and phase allows to double a frequency and to directly measure real power.

Let $V_x = V_x \sin\omega t$

$V_y = V_y \sin(\omega t + \theta)$

where θ is the phase difference the two signals.

~~Applying~~

o/p is $V_o = \dfrac{V_x \sin\omega t \; V_y \sin(\omega t + \theta)}{V_{ref}}$

$$V_o = \frac{V_x V_y}{V_{ref}} \sin\omega t (\sin\omega t \cos\theta + \sin\theta \cos\omega t).$$

$$V_o = \frac{V_x V_y}{V_{ref}} (\sin^2\omega t \cos\theta + \sin\theta \sin\omega t \cos\omega t).$$

But $\sin^2 a = 1 - \cos^2 a$

$\cos 2a = 2\cos^2 a - 1$

$\cos^2 a = \frac{1}{2} + \left(\frac{1}{2}\right)\cos 2a$

$\sin^2 a = 1 - \frac{1}{2} - \left(\frac{1}{2}\right)\cos 2a = \frac{1}{2} - \left(\frac{1}{2}\right)\cos 2a$

$$V_o = \frac{V_x V_y}{V_{ref}} \left[\cos\theta \left[\frac{1}{2} - \left(\frac{1}{2}\right)\cos 2\omega t\right] + \sin\theta \sin\omega t \cos\omega t\right]$$

But $\sin a \cos a = \frac{1}{2} \sin 2a$

Hence $V_o = \dfrac{V_x V_y}{2V_{ref}} (\cos\theta - \cos\theta \cos 2\omega t + \sin\theta \sin 2\omega t)$

(or)

$$V_o = \underbrace{\frac{V_x V_y}{2V_{ref}} \cos\theta}_{DC} + \underbrace{\frac{V_x V_y}{2V_{ref}} (\sin\theta \sin 2\omega t - \cos\theta \cos 2\omega t)}_{\text{2nd Term varies with time.}}$$

The first term is DC is set by the magnitude of the signals and their phase difference.

The second term varies with time, but at twice the frequency of the inputs (2ω)

<u>IDeal Doubler</u>: Both the I/P are same frequency.

$V_x = V_x \sin\omega t$

$V_y = V_y \sin\omega t$

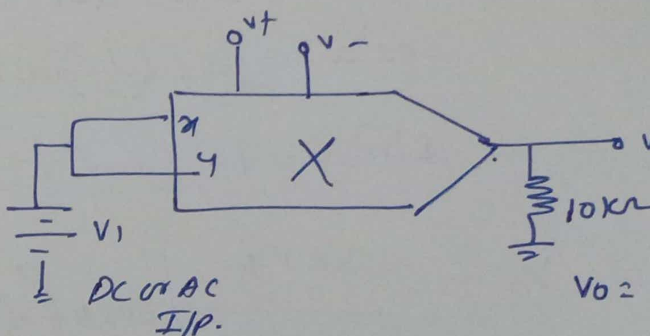
$$\boxed{V_o = \frac{V_x V_y}{V_{ref}} \sin^2\omega t}$$

$$V_o = \frac{V_x V_y}{V_{ref}}\left[1 - \frac{\cos 2\omega t}{2}\right]$$

The o/p contain a DC term and a Negative cosine wave of double frequency. The DC term easily Removed by using coupling capacitor between load and the o/p terminals.

<u>squarer circuit (voltage)</u>

Multiplier can be used to square any +ve ~~and~~ or Negative number provided the number can be represented by a voltage between 0 to V_{ref}



$$V_o = \frac{V_i^2}{V_{ref}}$$

V_i - is the I/P voltage.

I/Ps $V_x = V_y = V_i$

o/p $V_o = K V_x V_y$.

$K V_i^2$

$= \frac{1}{V_{ref}} \cdot V_i^2$

$$\boxed{V_o = \frac{V_i^2}{V_{ref}}}$$

[$K = \frac{1}{V_{ref}}$ the Scaling factor

$V_{in} = V_m \sin \omega t$

$$\boxed{V_o = \frac{V_i^2}{V_{ref}}}$$

For example. $V_i = V_m \sin \omega t$

$V_i = 5 \sin 2\pi \times 10^4 t$ and $V_{ref} = 10V$

$$V_o = \frac{5^2}{10}(\sin 2\pi \times 10^4 t)^2$$

$$= 2.5\left[\frac{1}{2} - \frac{1}{2}\cos 2\pi \times 2\times 10^4 t\right]$$

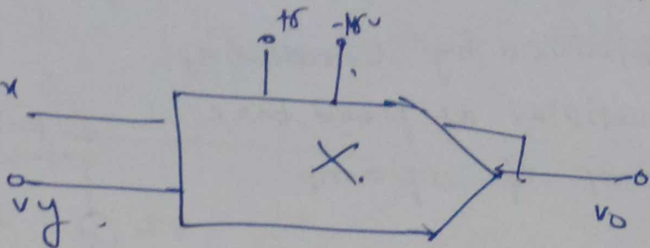
$$= 1.25 - 1.25 \cos 2\pi \times 2 \times 10^4 t$$

The o/p Contains a dc term and frequency is doubled.

Phase Angle Detection: Detect phase angle between two I/Ps.

$V_x = V_{mx} \sin \omega t$

$V_y = V_{my} \sin(\omega t + \theta)$



$V_o = \frac{V_{mx} V_{my}}{V_{ref}} \sin \omega t \sin(\omega t + \theta)$

$= \frac{V_{mx} V_{my}}{V_{ref}} \frac{1}{2} [\cos(\omega t - \omega t + \theta) - \cos(\omega t + \omega t + \theta)]$

$= \frac{V_{mx} V_{my}}{V_{ref}} \times \frac{1}{2} [\cos \theta - \cos(2\omega t + \theta)]$

$\sin A \sin B = \frac{1}{2}(\cos(A-B) - \cos(A+B))$

$= \frac{V_{mx} V_{my}}{V_{ref}} \times \frac{1}{2}$ (dc – ac frequency Term).

The o/p of multiplier is passed to a LPF which provides $\frac{1}{2}$ dc as o/p ie $\frac{1}{2} \cos \theta$.

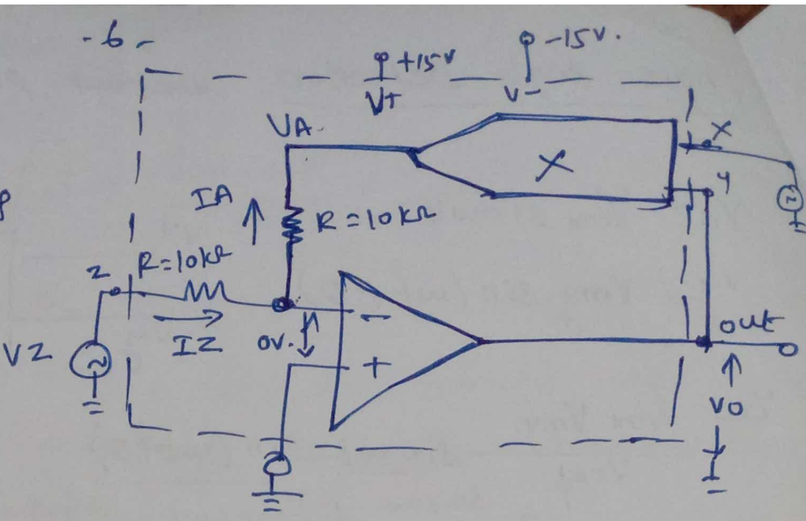
So the phase difference θ between the two input signals can be calculated from the dc component in the o/p voltage Vo ie

$$\boxed{V_{o,dc} = \frac{V_{mx} V_{my}}{2 V_{ref}} \times \cos \theta.}$$

$$\boxed{V_{odc} = \frac{V_{mx} V_{my}}{2 \times 10} \cos \theta}$$

The product of $V_{mx} V_{my}$ is made 20. So the O/P voltage is proportional to θ the phase angle difference between two sinusoidal input voltages applied

Voltage Divider:



obtained by Connecting Multiplier at feed back loop of opamp.

V_Z is divident

V_X is diviser

$$\boxed{V_O = -V_{ref} \cdot \frac{V_Z}{V_X}}$$

Proff: The opamp's inverting terminal is at virtual ground
Therefore

$$I_Z = I_A$$

$$I_Z = \frac{V_Z}{R}$$

The o/p voltage V_A of the multiplier is determined by the multiplicand of V_x and V_y.

$$V_A = \frac{V_x V_y}{V_{ref}} = \frac{V_x V_o}{V_{ref}}$$

Again

$$V_A = -I_A R.$$

$$I_A = -V_A/R$$

sub V_A in I_A

$$I_A = -\frac{V_x V_o}{V_{ref} R}$$

As

$$I_Z = I_A$$

so

$$I_Z = \frac{-V_x V_o}{R \cdot V_{ref}}$$

$$V_Z = I_Z R = \frac{-V_x V_o}{\cancel{R} \cdot V_{ref}} \cdot \cancel{R}$$

$$V_Z = \frac{-V_x V_o}{V_{ref}}$$

$$V_{ref} V_Z = -V_x V_o$$

$$\boxed{-V_{ref} \frac{V_Z}{V_X} = V_o}$$

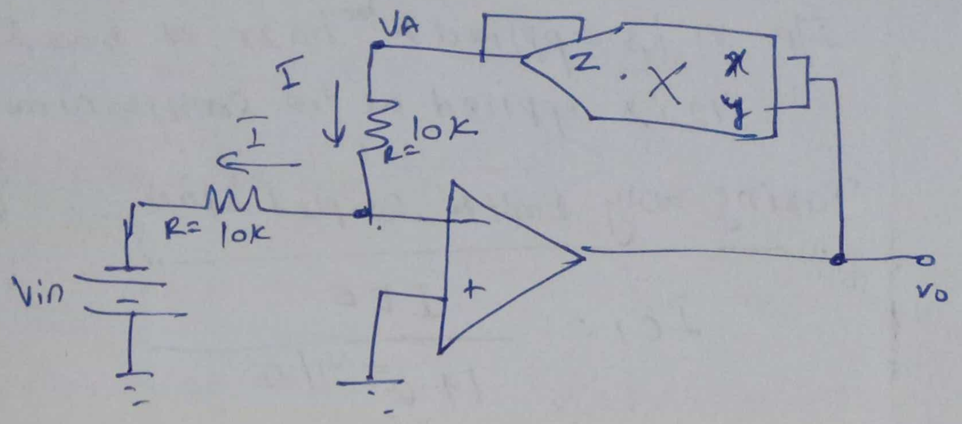
Square R
Let Vo
Here V

Square Root:

Let $V_o = \frac{V_x V_y}{V_{ref}}$

Here $V_A = \frac{V_o V_o}{V_{ref}}$

$$V_A = \frac{V_o^2}{V_{ref}}$$



And $V_A = -V_{in}$.

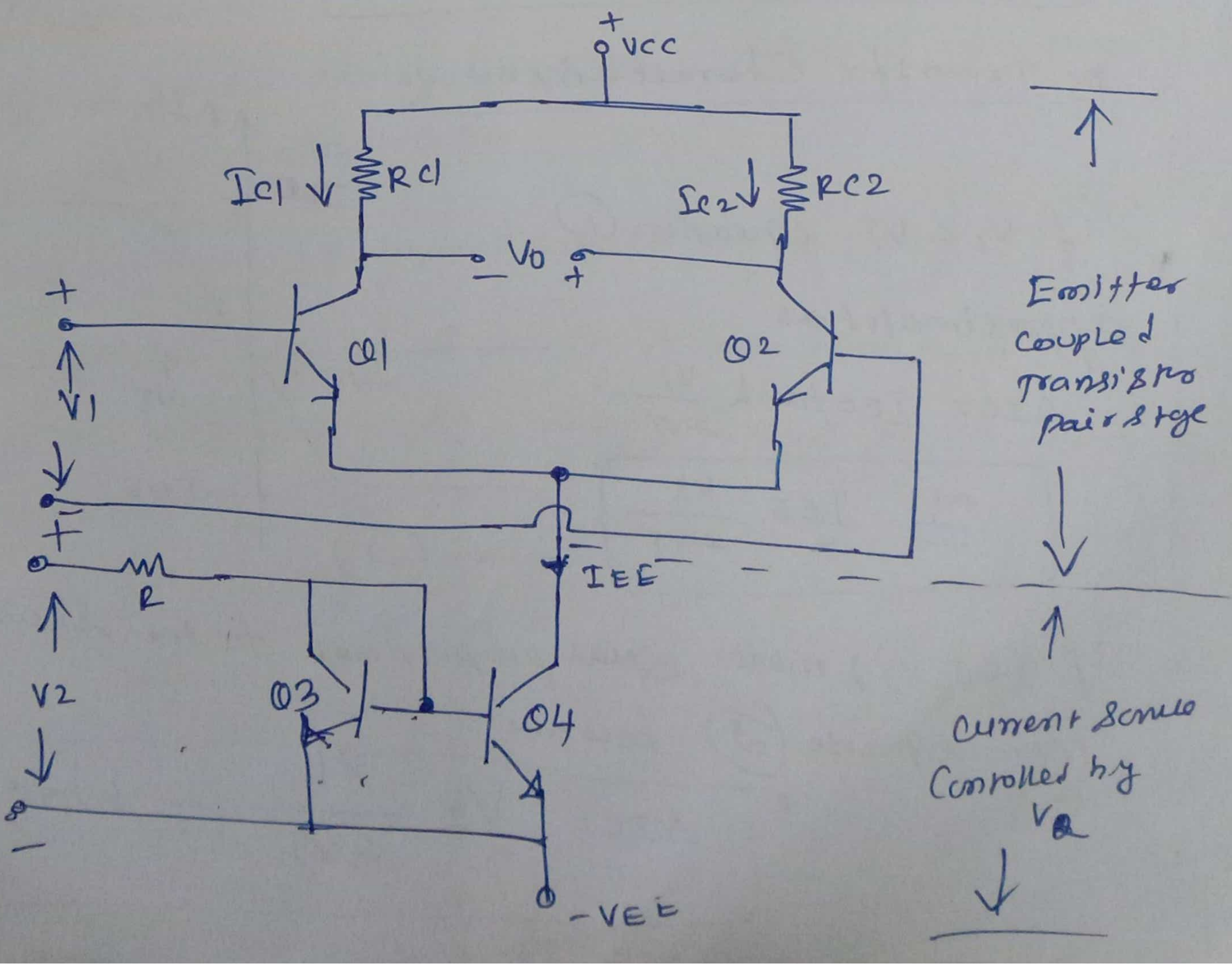
So $V_o^2 = -V_{in} V_{ref}$

or $\boxed{V_o = \sqrt{V_{ref} |V_{in}|}}$ taking magnitude only.

Thus, o/p Vo is proportional to square root of magnitude of Vin. Vin must be Negative or else op amp will saturate.

Vin Range lies between -1 and -10V.

Analog multiplier Using Emitter Coupled Transistor pair



I/P V_1 is applied to the base of transistor Q_1 and Q_2
V_2 is applied as the emitter current to both transistor

Taking only Emitter Coupled stage

$$I_{C1} = \frac{I_{EE}}{1+e^{-V_1/V_T}}$$

$$I_{C2} = \frac{I_{EE}}{1+e^{V_1/V_T}}$$

I_{EE} = emitter Bias current

V_T = Temp Equivalent voltage.

polarity of exponential depends on the I/p voltage V_1

$$\Delta I_C = I_{C1} - I_{C2}.$$

$$\Delta I_C = \frac{I_{EE}}{1+e^{-V_1/V_T}} - \frac{I_{EE}}{1+e^{V_1/V_T}}$$

$$= I_{EE}\left[\frac{1}{1+e^{-V_1/V_T}} - \frac{1}{1+e^{V_1/V_T}}\right]$$

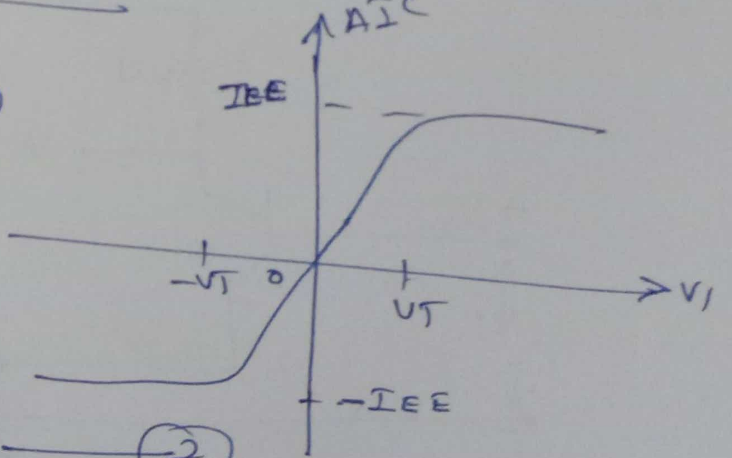
$$\boxed{\Delta I_C = I_{EE} \tanh \frac{V_1}{2V_T}} \quad \text{——— (1)}$$

DC Transfer Characteristics

if $V_1 < V_T$ equation (1) approximated as

$$\Delta I_C = I_{EE} \tanh \frac{V_1}{2V_T}$$

$$\boxed{\simeq I_{EE} \frac{V_1}{2V_T}} \quad \text{——— (2)}$$



if I_{EE} is made ~~equal~~ proportional to the second I/P V_2. then equation (2) becomes

$$\boxed{\Delta I_C = V_2 \frac{V_1}{2V_T}} \quad \text{where } V_2 \propto I_{EE}$$

IBE by considering Base to Emitter voltage,

$$I_{EE} \simeq K_0 (V_2 - V_{BE(ON)}) \quad \text{——— (3)}$$

sub (3) in (2).

$$\boxed{\Delta I_C = \frac{K_0 (V_2 - V_{BE(ON)}) \cdot V_1}{2 V_T}}$$

K_0 is scalling factor

For proper Multiplication

(1) $V_1 < 50mV$.

(2) V_2 must be greater than $V_{BE(ON)}$.

Draw Backs:

(1) The input voltage V_2 is offset by $V_{BE(ON)}$. so desired input V_2 cannot be multiplied with other I/P V_1. Thus the preciseness in getting the product O/P is affected

(2) V_2 must be always positive resulting in two quadrant multiplication.

(3) $\tanh\left(\frac{V_1}{2V_T}\right)$ is approximated as $\left(\frac{V_1}{2V_T}\right)$ with assumption $V_1 \ll V_T$. In Room Temp, $V_T = 26mV$. Therefore, V_1 must be very small to satisfy the approximation

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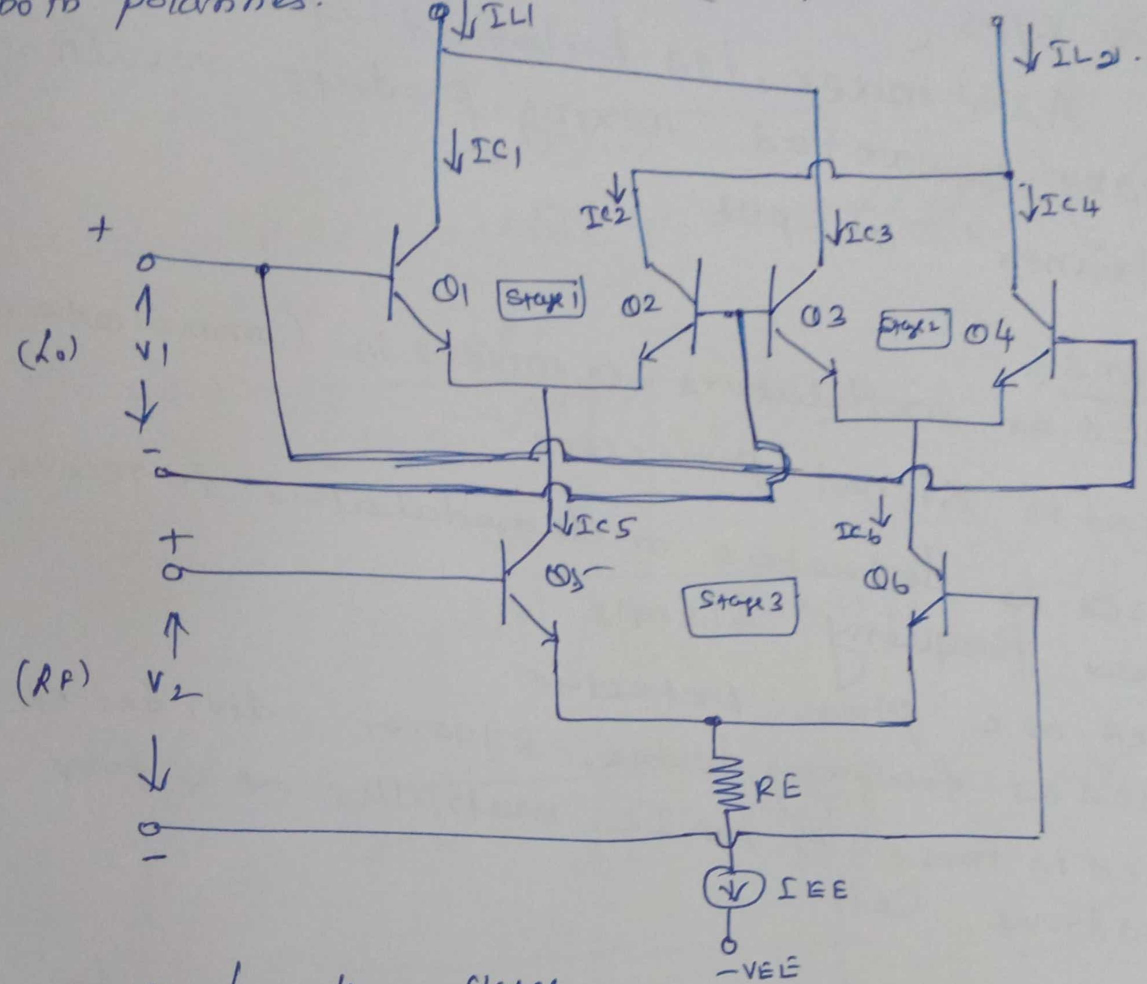
-10-

Explain the working of a Gilbert multiplier cell.

The Gilbert Multiplier also called four quadrant multiplier cell. It allows the two input voltage to swing in both polarities.



circuit has three stages.

stage 1 and 2, & 3

What is Gilbert Multiplier cell?

The Gilbert multiplier cell is a modification of the emitter coupled cell and this allows four quadrant Multiplication. Therefore, it forms the basics of most of the IC balanced multipliers.

Two cross coupled emitter-coupled pairs in series connection with an emitter coupled pair form the structure of the Gilbert multiplier cell.

It is a type of mixer. It produces o/p signals that are proportional to the product of two I/p signals. It widely used for frequency conversion in radio systems.

Advantage: O/P current is an accurate multiplication of the (differential) base currents of both I/PS.

As a mixer, its balanced operation cancels out many unwanted mixing products, resulting in a "cleaner" output.

Applications:

1) Used as modulators or mixers in communication systems
2) used in signal processors.
3) Used as detectors or demodulators to recover low frequency signals.
4) Used as a Phase Detectors
5) used as frequency doubler, squarer, divider etc.
6) Used in most of the IC multipliers as a four quadrant Cell.

DC Analysis:

collector currents of Q_1 and Q_2 are given by.

$$I_{C1} = \frac{I_{C5}}{1+e^{-V_1/V_T}} \quad \text{——} (1)$$

$$I_{C2} = \frac{I_{C5}}{1+e^{V_1/V_T}} \quad \text{——} (2)$$

[∴ I_{C5} is emitter current of pair Q_1 and Q_2

(ii) collector current of Q_3 and Q_4 are given as

$$I_{C3} = \frac{I_{C6}}{1+e^{V_1/V_T}} \quad \text{——} (3)$$

$$I_{C4} = \frac{I_{C6}}{1+e^{-V_1/V_T}} \quad \text{——} (4).$$

[∴ I_{C6} is emitter current of pair Q_3 and Q_4

And collector current of Q5 and Q6 can be given as

$$I_{C5} = \frac{I_{EE}}{1+e^{-V2/VT}} \quad \text{—— (5)}$$

$$I_{C6} = \frac{I_{EE}}{1+e^{V2/VT}} \quad \text{—— (6)}$$

Sub values of IC5 and IC6 in equations (1), (2), (3) & (4)
we get

$$I_{C1} = \frac{I_{EE}}{[1+e^{-V1/VT}][1+e^{-V2/VT}]} \quad \text{—— (7)}$$

$$I_{C2} = \frac{I_{EE}}{[1+e^{V1/VT}][1+e^{-V2/VT}]} \quad \text{—— (8)}$$

$$I_{C3} = \frac{I_{EE}}{[1+e^{V1/VT}][1+e^{V2/VT}]} \longrightarrow (9)$$

$$I_{C4} = \frac{I_{EE}}{[1+e^{-V1/VT}][1+e^{V2/VT}]} \quad \text{—— (10)}$$

The differential o/p current ΔI is given as

$$\Delta I = I_{L1} - I_{L2}$$

Where $I_{L1} = I_{C1} + I_{C3}$ and $I_{L2} = I_{C2} + I_{C4}$
from the figure.

$$\therefore \Delta I = (I_{C1} + I_{C3}) - (I_{C2} + I_{C4})$$

or

$$\Delta I = (I_{C1} - I_{C4}) - (I_{C2} - I_{C3}) \quad \text{—— (11)}$$

sub equations 7 to 10 in equations (11) and taking exponential terms as hyperbolic tangent functions, we get

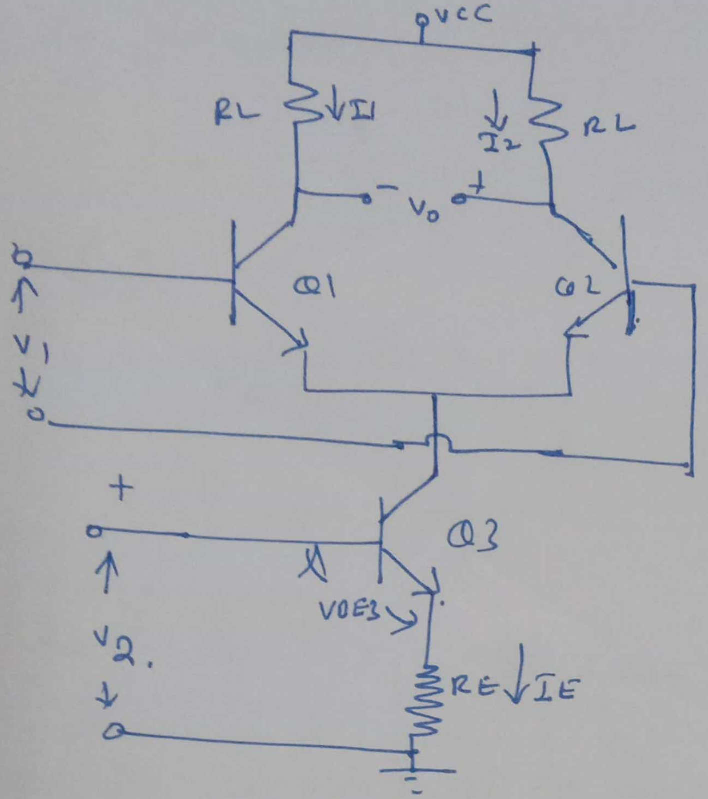
$$\Delta I = I_{EE}\left[\tanh\left(\frac{V1}{2V_T}\right)\tanh\left(\frac{V2}{2V_T}\right)\right]$$

Thus the differential current ΔI is the product of the hyperbolic tangent of two I/Ps of voltages V_1 and V_2. The O/P V_o can be obtained from ΔI by using two equal value Resistor R connected to Vcc and sending current $I_{L1} = (I_{C1} + I_{C3})$ through one resistor and $I_{L2} = (I_{C2} + I_{C4})$ through other Resistor.

What are the advantages of emitter coupled transistor pair?

1. High current gain
2. more stability
3. compact and easily implemented in IC form.

Variabe Transconductance Technique.



2mark

What is the function of Variabe Transcondutue amplifier?

Multiply two I/p voltages by using the principle of dependency of transistor transconductance on the emitter current bias applied. The emitter current bias controlled by the V_2.

Q1 and Q2 forms differential Amp

Differential Stage is used for transconductance Technique Emitter current bias is Controlled by the Second Input Voltage V_2. Q1 and Q2 forms differential amplifier

for very small differential voltage ie $V_1 \ll V_T$, under this condition the o/p voltage is given as

$$\boxed{V_0 = g_m R_L V_1}$$

where $\boxed{g_m = \frac{I_E}{V_T}}$ is the transconductance — (1)

V_0 depends on g_m and g_m depends on I_E, By changing V_2, I_E changes thereby g_m changes. ie g_m controlled by V_2 internaly.

From abue Figure

$$V_2 = I_E R_E + V_{BE3}$$

$$\text{if } I_E R_E > V_{BE3}$$

$V_2 = I_E R_E$ and $\boxed{I_E = \frac{V_2}{R_E}}$ —— (2)

Sub I_E in g_m equation.
(2) in (1)

$$g_m = \frac{\frac{V_2}{R_E}}{V_T} = \frac{V_2}{R_E V_T} \quad —— (3)$$

Let $V_o = g_m R_L V_1$

then $V_o = \frac{V_2}{R_E V_T} R_L V_1$ —— (4)

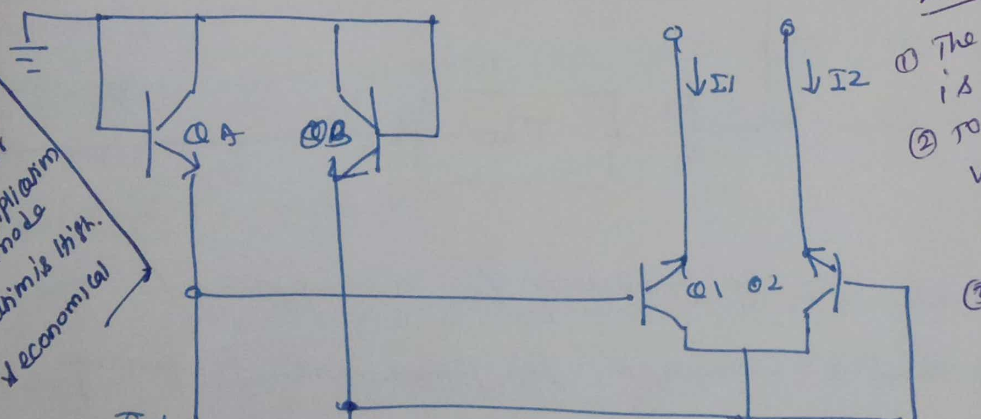
$$= V_1 V_2 \frac{R_L}{R_E V_T}$$

$$K = \frac{R_L}{R_E V_T}$$

$$\boxed{V_o = K V_1 V_2}$$

K is the scalling facter.

O/P is proportional to the product of two input voltages.
To improve the linearity of the multiplier, exponential current voltage characteristics can be converted into linear characteristics.



Advantages:
1) Accurate O/P
2) It can provide four quadrant multiplication mode
3) speed of operation is high.
4) Low cost & economical

Limitations:
(1) The scale factor K is temp dependent
(2) Total current I_E varies as a function of V_2.
(3) The large common mode voltage swing in the circuit which is highly objectionable, if a single ended O/P

The limitation can be eliminated by Gilbert cell

Transistors QA and QB is diode connected and are driven by I_A and I_B, I_1 and I_2 are related as

$$\boxed{\frac{I_1}{I_2} = e^{(V_1/V_2)}}, \quad \boxed{V_1 = V_T \ln\left(\frac{I_B}{I_A}\right)}$$

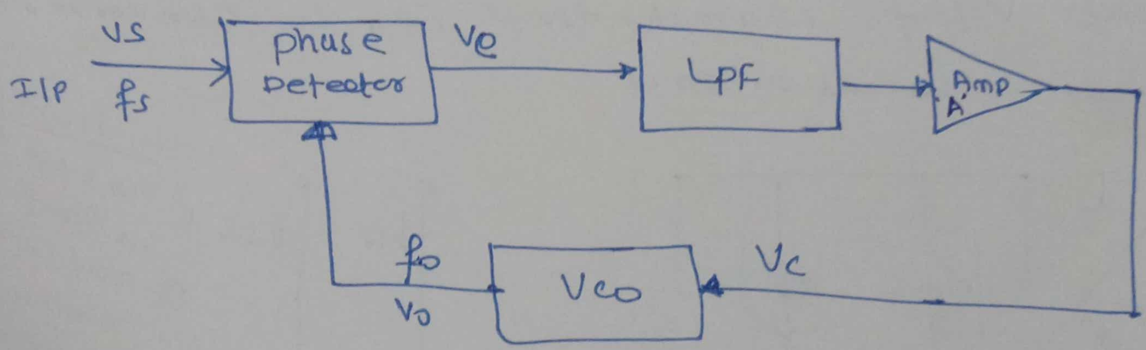
and substituting V_1 in $\frac{I_1}{I_2}$ we get $\frac{I_1}{I_2} = \frac{I_B}{I_A}$, Assuming that V_T is very small

What is PLL and List the Basic Building Blocks of PLL?

PLL: phase Locked Loop: PLL is a circuit which detects the phases of two signals and reduce the difference in the presence of a phase difference. The internally generated frequency and externally frequency are compared to detect and track the change in their phase difference.

Basic Building Blocks of PLL [closed loop system].

1) phase Detector / Comparator
2) A Low pass Filter
3) An error Amplifier
4) A voltage Controlled Oscilator (VCO)



I/P signal V_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of incoming signal.

If the two signals differ in frequency and/or phase, an error voltage V_e is generated.

phase Detector is basically multiplier and produce

sum $(f_s + f_o)$ and

difference $(f_s - f_o)$ components at its o/p.

LPF: The High frequency component $(f_s + f_o)$ is removed by LPF and the difference frequency components is amplified and then applied as control voltage V_c to VCO.

Capacture Range (or) state

The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. once this action ~~takes~~ starts, we say that the signal is in Capacture Range. (The Range of frequencies over which the PLL can acquire lock with the I/P signal)

Phase Lock state:

The frequency of VCO can be set by an external capacitor and Resistor. The o/p frequency f_o of VCO is compared with the incoming signal f_s.

when $\boxed{f_o = f_s}$, the PLL is said to be locked

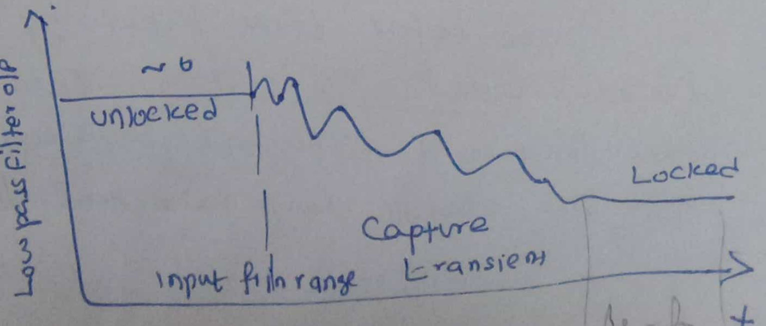
Tracking State:

once the PLL is Locked, PLL tracks the changes in frequency of I/P signal and the VCO o/p frequency changes and try to match the I/P signal. This action is repetitive in nature.

NOTE: once PLL Locked, the phase difference ϕ generates a corrective control voltage V_c to shift the VCO frequency from f_o to f_s and there by maintain a lock.

Capture transient

Range of frequency PLL can lock with f_s. called Lock in Range



From above figure, As capture starts, a small sine wave appears due to frequency difference between VCO frequency and I/P frequency $(f_o - f_s)$. The DC component of the signal drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move towards closer to the I/P signal frequency.

The difference in frequency becomes smaller and a large DC component passed by the filter, shifting the VCO frequency further. These process continues until the VCO locks onto the signal and the difference frequency is DC.

Capature starts → sine wave → f_o moves towards f_s
$f_o = f_s$ = locked
Difference frequency only DC

Important Definitions Relat to PLL

2mrk **Lock in Range:**

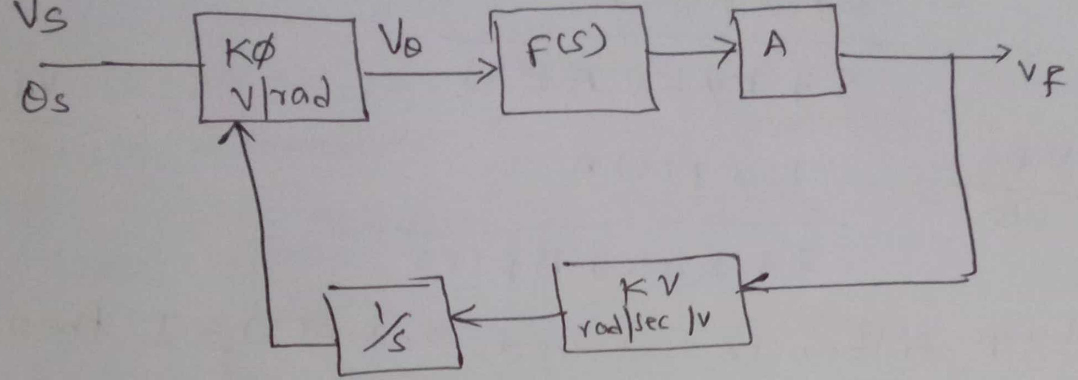
Once the PLL locked, it can track frequency changes in the incoming signals. The range of frequency over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range usually expressed as a percentage of f_o, the VCO frequency.

2mrk **Capture Range**: The Range of frequencies over which the PLL can acquire lock with an I/P signal is called the capture range, expressed as percentage of 'f_o'

2mrk **pull in time**:

The total time taken by the PLL to establish lock is called pull in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

Closed Loop Analysis of PLL



Block diagram of PLL system.

K_ϕ : Conversion gain of phase detector in volt/rad

F(s): Loop Transfer function.

A : Gain of the Amplifier

K_v: voltage to frequency transfer coefficient of Vco

The phase of the vco output is actually equal to the time integral of the vco output frequency.

Since $W_o(t) = \dfrac{d\,\theta_o(t)}{dt}$

$$\theta_o(t) = \theta_o\Big|_{t=0} + \int_0^t w_o(t)\,dt$$

Integration is represented by $1/s$

When $V_f = 0$, the Vco frequency is called free running frequency, W_c. The relation between the Vco output frequency W_o and V_f is given by.

$$W_o(t) = \omega_c + K_o V_f(t)$$

The closed loop transfer function for a PLL system. given by.

18-2

$$\frac{V_f}{\theta_s} = \frac{K_\phi F(s) A}{1 + K_\phi F(s) A \frac{K_V}{s}}$$

$$= \frac{s K_\phi F(s) A}{s + K_\phi K_V A F(s)}$$

$$\therefore \frac{V_f}{\omega_s} = \frac{1}{s} \frac{V_f}{\theta_s}$$

$$\frac{V_f}{\omega_s} = \frac{K_\phi F(s) A}{s + K_\phi K_V A F(s)}$$

if Loop filter is not used, and $F(s) = 1$ then

$$\frac{V_f}{\omega_s} = \frac{K_\phi A}{s + K_\phi K_V A}$$

$$= \left(\frac{K_L}{s + K_L}\right) \frac{1}{K_V}.$$

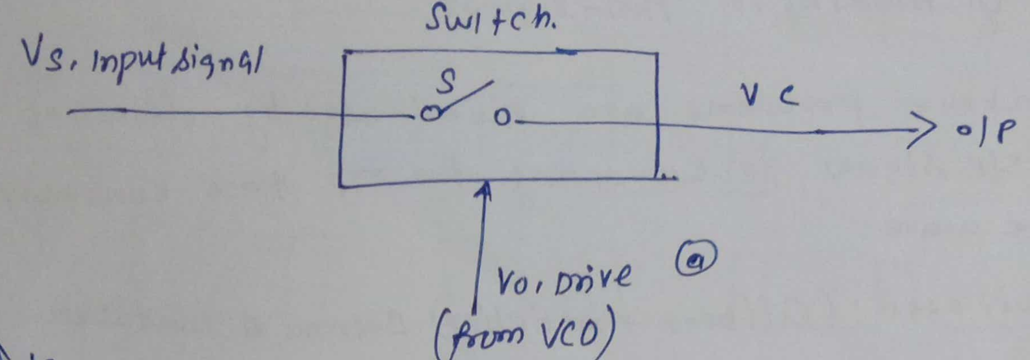
where $K_L = K_\phi K_V A$ and it known as Loop Bandwidth,

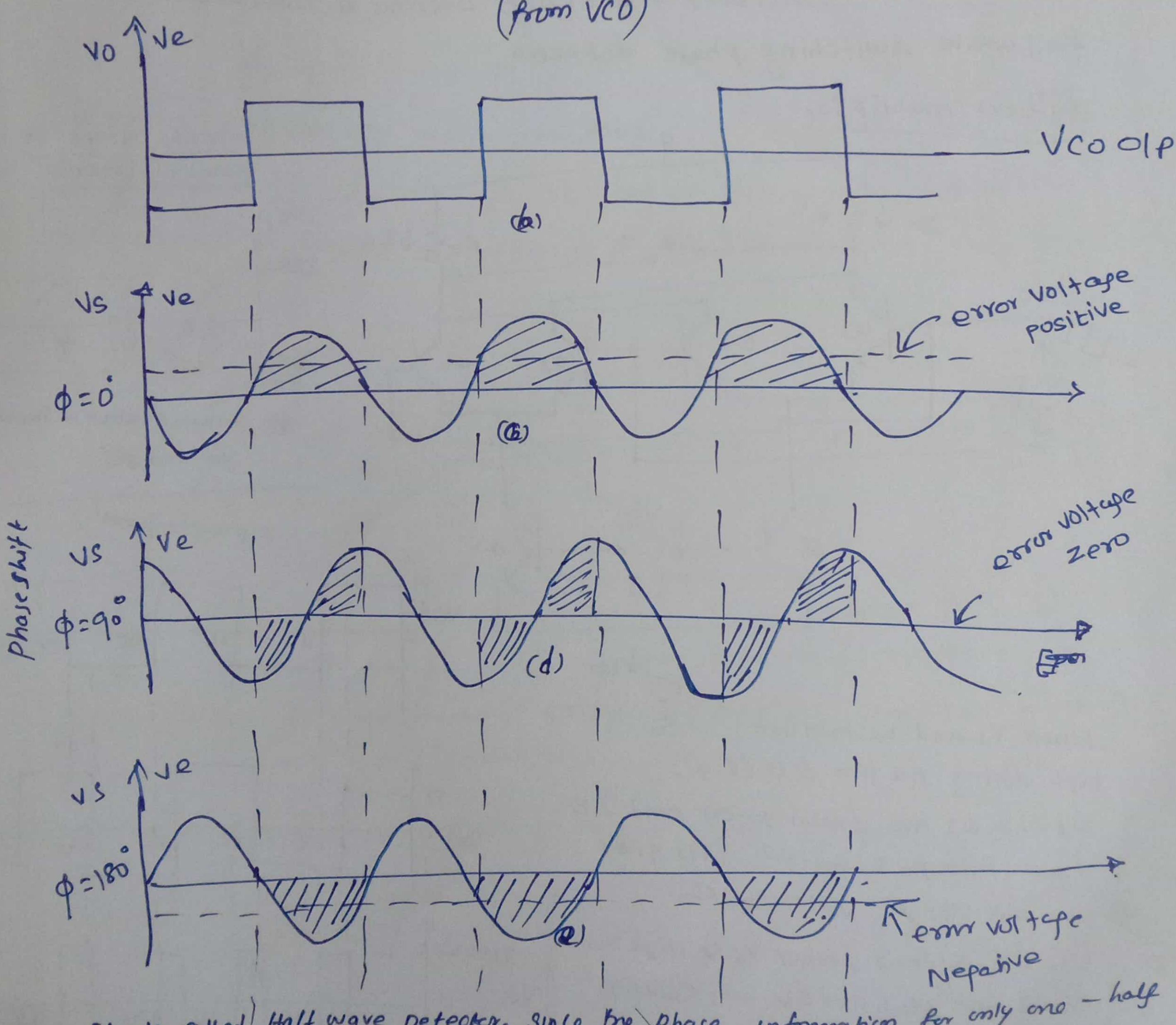
K_L = product of the phase detector gain K_ϕ . x VCO transfer coefficient.

—x—

Analog phase Detector:

It is a switch type phase Detector. A Gilbert cell can be used as along phase detector. An electronic switch is ~~is used~~ is opened and closed by signal coming from VCO. The input signal is, therefore, chopped at a repetition rate determined by VCO frequency.





It also called Half wave Detector, since the phase information for only one - half of the I/P waveform is detected and averaged. The o/p of the phase comparator when filtered through a LPF gives an error signal which is the average value of the o/p waveform shown in above

Problems associated with the Switch type phase Detector

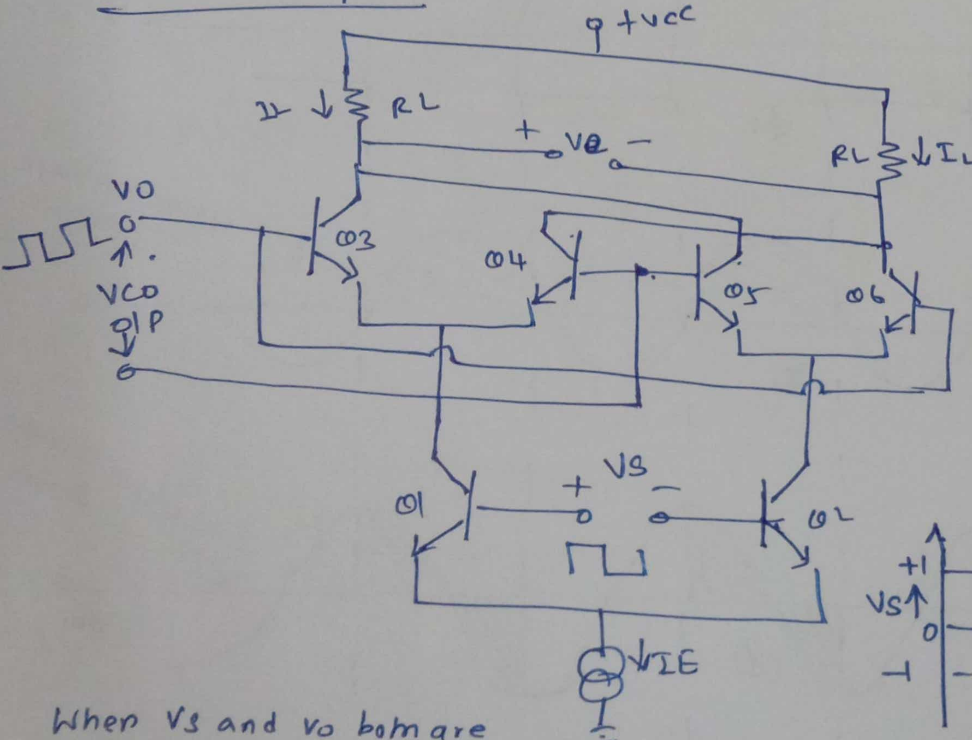
1) The o/p voltage 'V_o' is proportional to the I/P signal amplitude 'V_s'. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude.

2) The o/p is proportional to $\cos\phi$ and not proportional to ϕ making it non-linear.

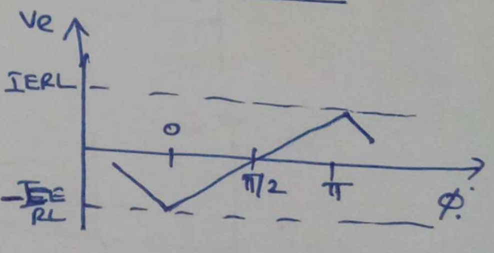
The above problems are eliminated by limiting the amplitude of the I/P signal ie converting the I/P to a constant amplitude square wave.

Circuit used: (Gilbert multiplier) Balanced modulator used as full wave switching phase detector.

Gilbert multiplier

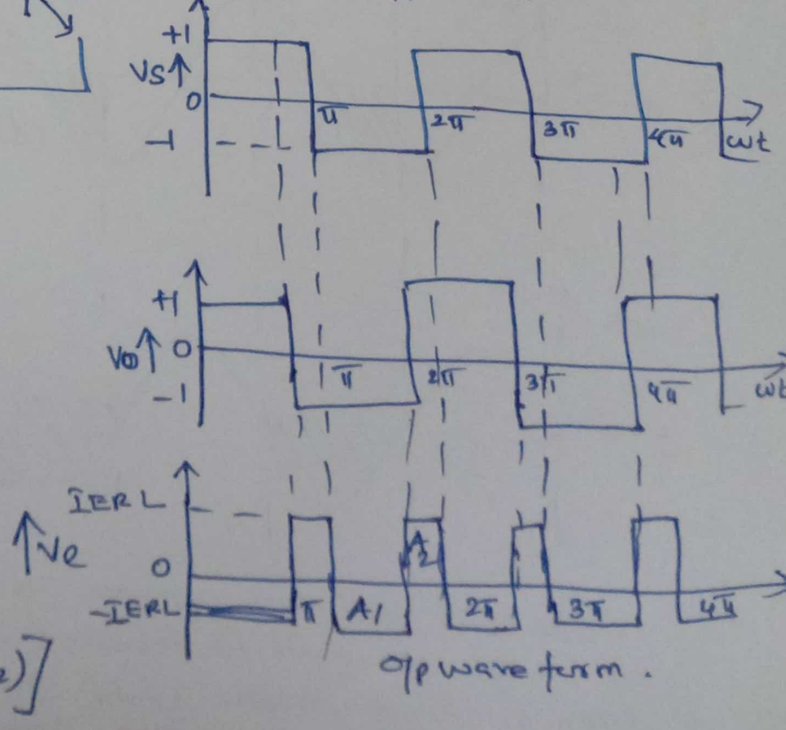


o/p DC voltage Vs phase difference



* Linear relation between Ve and φ

I/p waveform



o/p waveform.

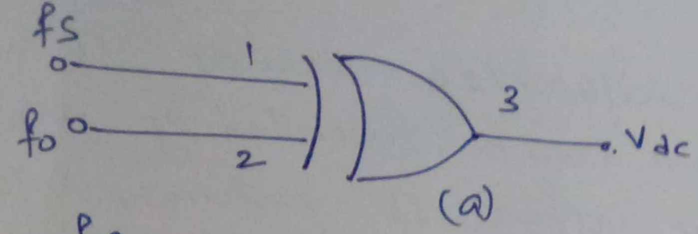
When Vs and Vo both are high during the time 0 to $(\pi - \phi)$, Q_1 and Q_3 are driven to on and I_E flows through Q_1 and Q_3. This gives an o/p voltage $V_e = -I_E R_L$.

For $(\pi - \theta)$ for π, when Vs is High and Vo is Low, Q1 and Q6 on, Resulting $V_e = I_E R_L$

then $(V_e)_{avg} = \frac{1}{\pi}\left[\text{area } A_1 + \text{Area}(A_2)\right]$

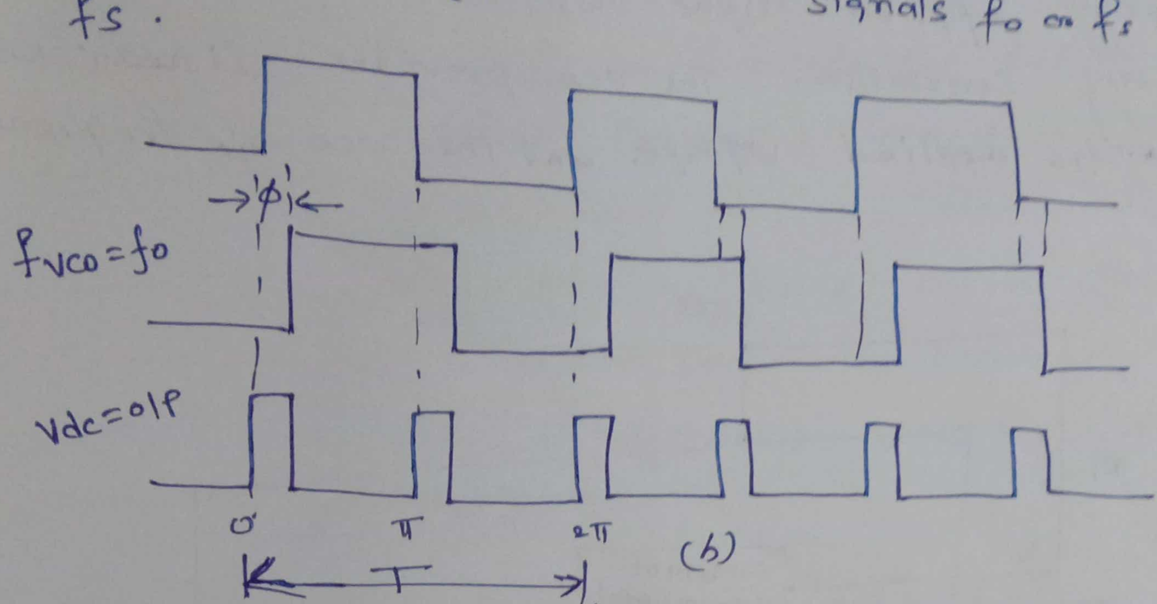
$= K\phi(\phi - \pi/2)$

Digital phase Detector : using EX-OR gate



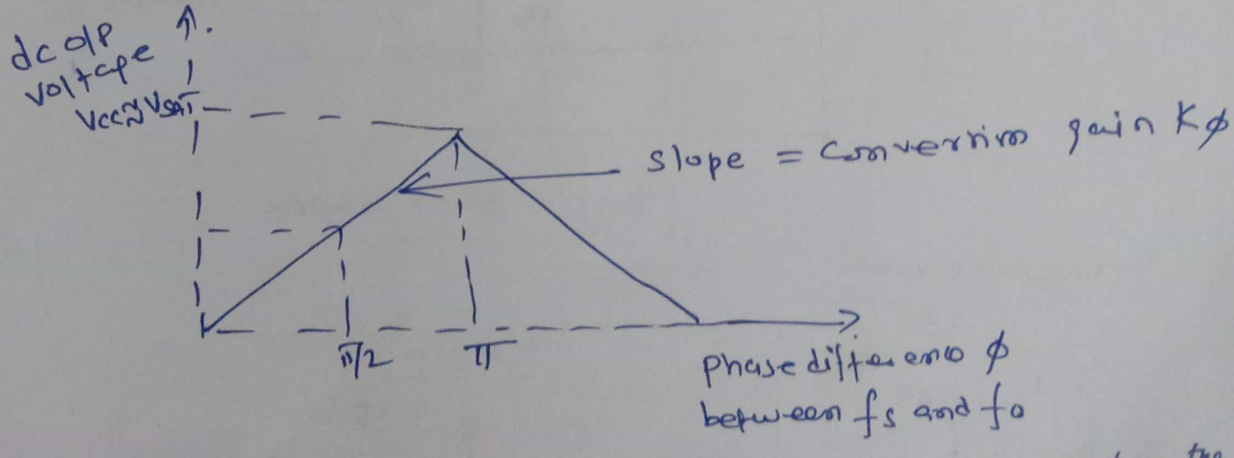
(a)

o/p of X-OR is High when only one of two I/P signals fo or fs is High.



(b)

I/P and o/p waveforms for $f_s = f_o$ in (b). Here f_s is leading f_o by ϕ degrees. The variation of dc o/p voltage with phase difference ϕ is shown below.



From above Fig, maximum error voltage is produced when the phase difference is π radians.

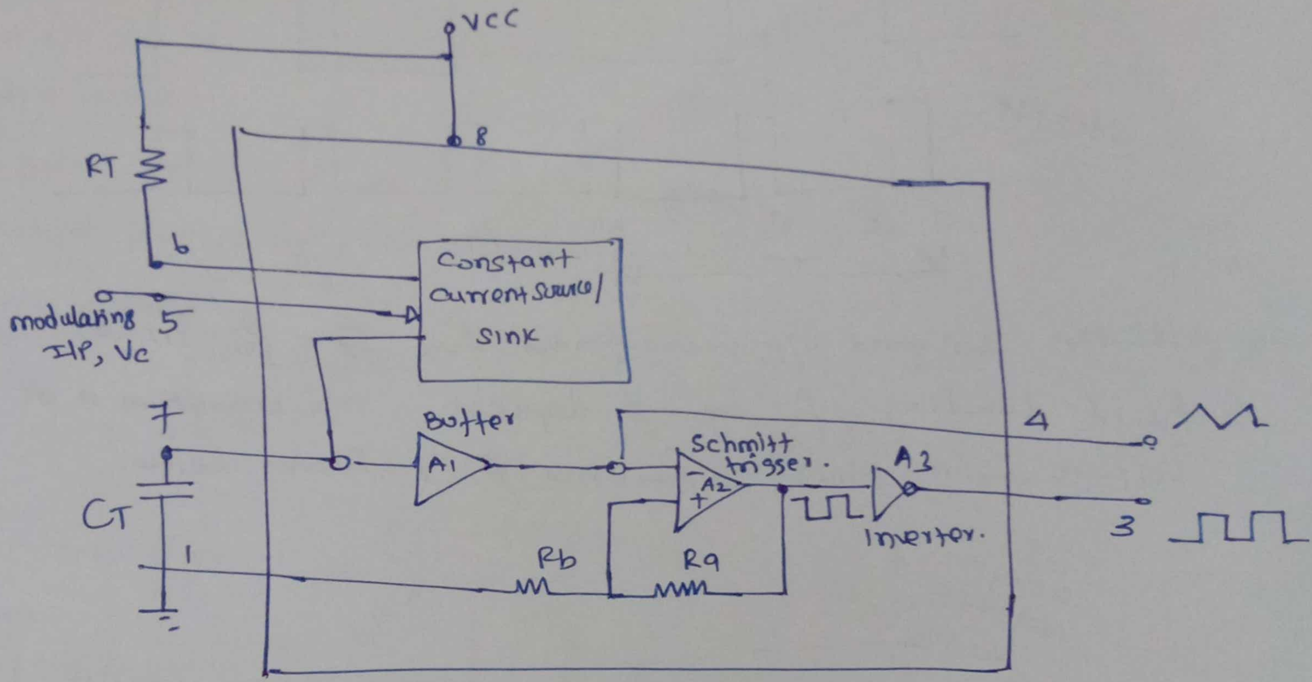
The conversion gain $K_\phi = \frac{V_{CC}}{\pi}$ if $V_{CC} = 5V$

$$\boxed{K_\phi = \frac{5V}{\pi} = 1.59\,V/\text{radian.}}$$

VCO :

What is VCO?

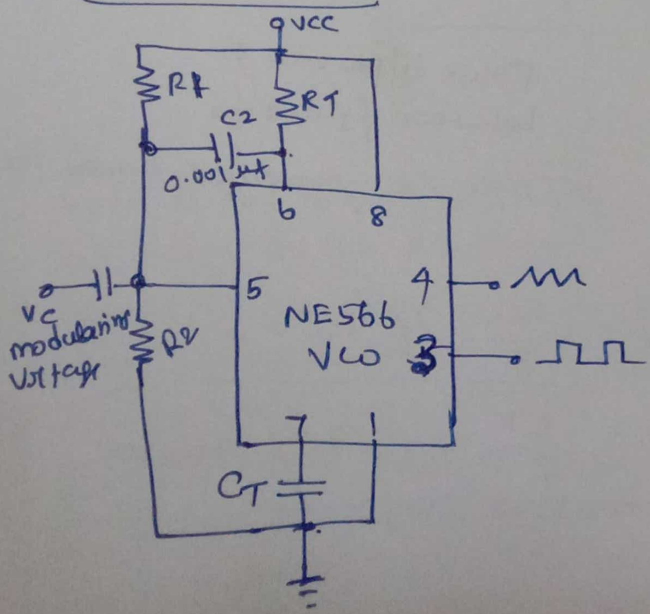
A voltage controlled oscilator is a circuit in which the frequency of oscilation can be controlled by an externaly applied input voltage. It performs voltage to frequency conversion. The VCO provides linear Relationships between the applied voltage and the VCO o/p frequency.

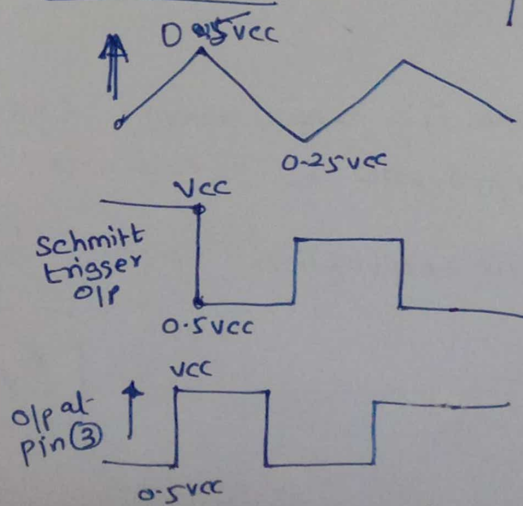


Basic Block diagram

A3 => current Amplifier to Drive the Load

Connection Diagram





o/p wave forms.

* A small capacitor 0.001µf connected between 5 and 6 to eliminate possible oscilations.
* VCO used to low frequency signals into audio frequency Range.
* modulating voltage applied at pin no 5
* Capacitor C_1 is charging and discharges due to the reference set at the non inverting terminal of op-amp A_2 from 0.5VCC to 0.25VCC by potential divider Ra and Rb.
* If the o/p of Buffer tries to exceed 0.5VCC the schmitt trigger goes low and the capacitor discharges until 0.25VCC and again schmitt trigger goes high state and this process repeats.

The o/p frequency of VCO can be calulated as

The total voltage on the capacitor changes from 0.25VCC to 0.5VCC. Thus $\Delta V = 0.25\,VCC$. The Capacitor

The Rate of change of voltage across capacitor is given as $\Big\}$ $\dfrac{\Delta v}{\Delta t} = \dfrac{i}{CT}$.

(or) $\dfrac{0.255\,Vcc}{\Delta t} = \dfrac{i}{CT}$

$$\boxed{\Delta t = \frac{0.25\,Vcc\;CT}{i}} \quad \text{——} (1)$$

The time period of triangular wave form is $\cancel{2\Delta t}$ $2\Delta t$ (T)

The frequency of oscilator fo is

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5\,Vcc\;CT} \quad \text{——} (2)$$

But $i = \dfrac{Vcc - V_c}{R_T}$

sub i in eq (2)

Where, V_c is the voltage at pin 5. There fore

With no modulating I/p voltage $V_c = (7/8)(+V)$

$$\boxed{f_o = \frac{2(V_{CC} - V_c)}{C_T R_T V_{CC}}} = \boxed{\frac{2(V_{CC} - (7/8)V_{CC})}{C_T R_T V_{CC}}} \quad (3)$$

original frequency

$$= \frac{1}{4 R_T C_T} = \frac{0.25}{R_T C_T}$$

The o/p frequency of VCO can be changed either by (i) R_T (ii) C_T or (iii) the voltage at V_c at pin No 5. The voltage can be varied by connecting a $R_1 R_2$ circuit

Voltage to frequency conversion factor

Voltage to frequency conversion factor K_v is defined as

2 mark

$$\boxed{K_v = \frac{\Delta f_o}{\Delta V_c}} \quad (4)$$

Here ΔV_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is 'f_1' then,

$$\Delta f_o = f_1 - f_o = \frac{2(V_{CC} - V_c + \Delta V_c)}{C_T R_T V_{CC}} - \frac{2(V_{CC} - V_c)}{C_T R_T V_{CC}}$$

from o/p f_o we have to generate f_1

$$\frac{1}{C_T R_T V_{CC}}\left[\cancel{2V_{CC}} - \cancel{2V_c} + 2\Delta V_c - \cancel{2V_{CC}} + \cancel{2V_c}\right]$$

$$\Delta f_o = \frac{2\Delta V_c}{C_T R_T V_{CC}} . = \Delta f_o C_T R_T V_{CC} = 2\Delta V_C \quad (5)$$

$$\text{or } \Delta V_c = \frac{\Delta f_o C_T R_T V_{CC}}{2}$$

Sub. the value of R_T and C_T in f_o ~~below~~ from equation (3), we get

$$\boxed{f_o = \frac{0.25}{R_T C_T}} = \frac{0.25}{\frac{2\Delta V_C}{\Delta f_o \cdot V_{CC}}}$$

$$\Delta V_C = \Delta f_o V_{CC} / 8 f_o \qquad \Delta V_C = \frac{\Delta f_o V_{CC}}{8 f_o}$$

$R_T C_T = \frac{2\Delta V_C}{\Delta f_o V_{CC}}$

$f_o = 0.25$

$$\text{or} \quad \boxed{K_v = \frac{\Delta f_o}{\Delta V_c} = \frac{8 f_o}{V_{CC}}}$$

$$= \frac{f_o}{0.125 V_{CC}}$$

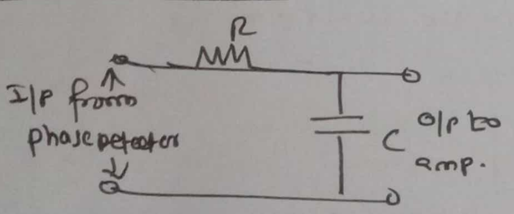
Vco is called as V-f converter Why?

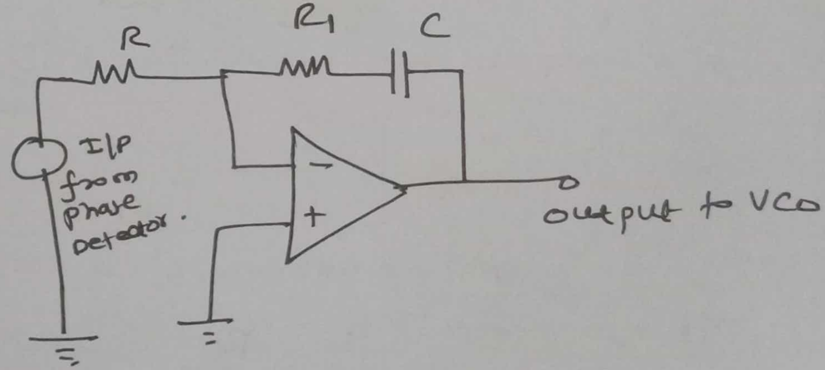
Vco is called as voltage to frequency converter because, when the control voltage I/P V_c is changed to a new voltage ΔV_c, o/p frequency of VCO is also changed to new frequency Δf_o to f_o, the free running frequency or centre frequency VCO

$$V_c \text{ to } \Delta V_c \propto f_o \text{ to } \Delta f_o$$

ΔV_c is voltage deviation and Δf_o is the frequency deviation. Therefore, the out of VCO is directly proportional to input voltage V_c.

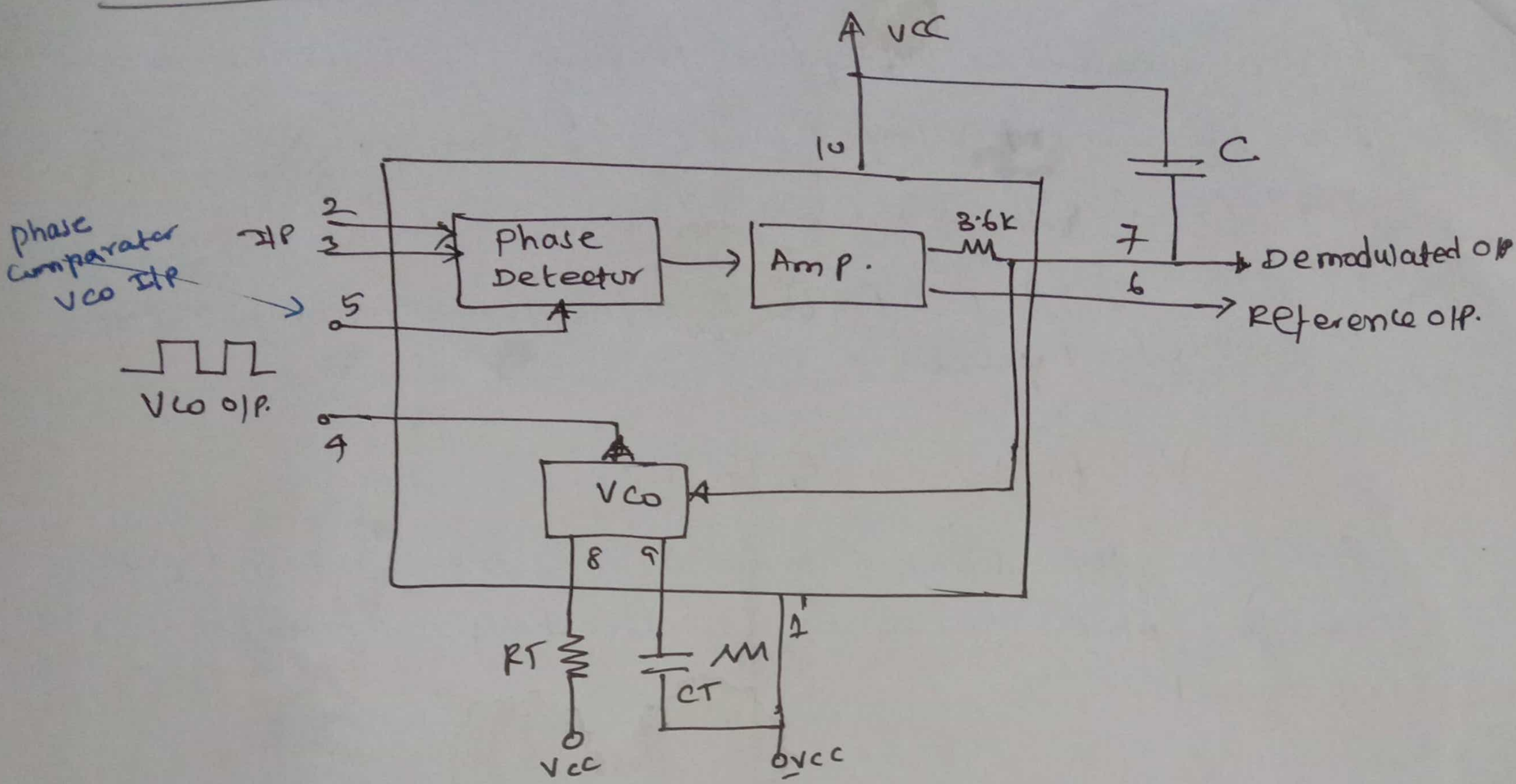
Low pass Filter:





Low pass Filter Remove the high frequency components and also controls the dynamic characteristics of PLL

MonoLiTHIC PLL (IC 565)



The output frequency of VCO can be written as

$$\boxed{f_o = \frac{0.25}{R_T C_T} \text{ Hz}}$$

→ C_T, R_T ⇒ external capacitor and resistor connected to pin no 8 and 9. R_T = 2kΩ to 20kΩ

→ The free running frequency of VCO is adjusted with R_T and C_T.

→ The capacitor C and 3.6k resistor make a low pass filter.

→ phase comparator compares f_o with input signal f_s

→ conversion ratio of phase detector of 565 PLL as

$$\boxed{K_\phi = \frac{0.7-(-0.7)}{\pi} = \frac{1.4}{\pi}}$$

→ Demodulated output taken at pin no-7.

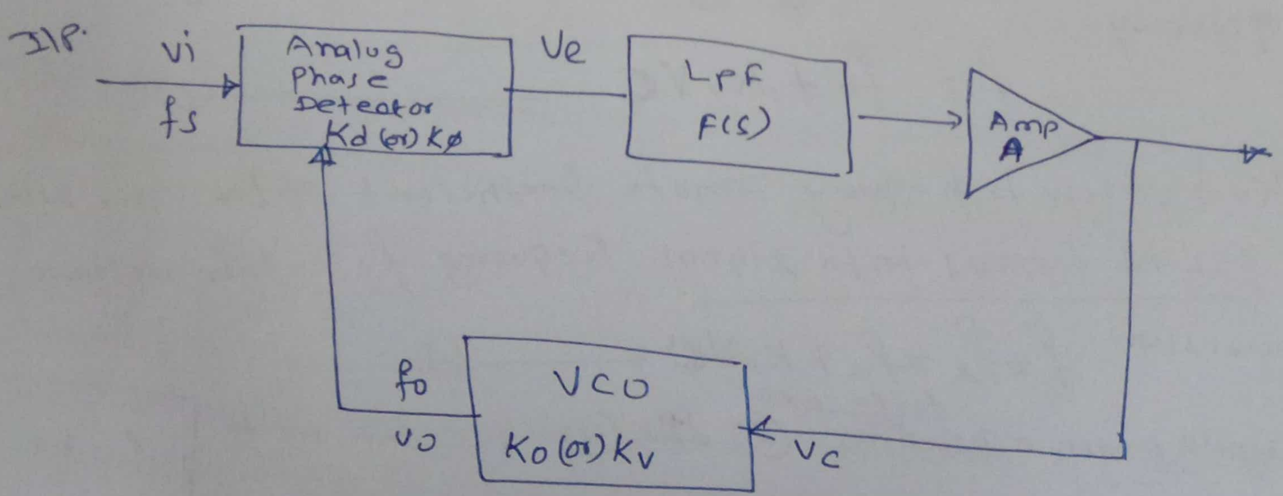
Electrical characteristics - 27 -

1) operating frequency: 0.001 HZ to 500KHZ
2) operating voltage range: ±6V to ±12V.
3) I/P tracking Level required: 10mV rms minimum to 3V PP maximum
4) I/P resistance: 10kΩ
5) o/p sink current: 1mA
6) o/p source current: 10mA
7) Bandwidth adjustment range: ±1% to ±60%.
9) square wave amplitude 5.4 Vpp at ±6V supply voltage.
10) Traiangle wave amplitude 2.4 Vpp at ±6v supply voltage

Derivation of Lock in Range and Capture Range

Lock in Range:

To understand we take Basic Block of PLL with transfer function of each block as given by



Derivation of Lock in Range in PLL

If ϕ radians is the phase difference between the signal voltage V_i and the VCO voltage V_o, then the o/p voltage of analog phase Detector V_e is given by

$$V_e = K\phi(\phi - \pi/2) \quad \text{---------} \quad (1)$$

where $K\phi$ is the phase angle-to-voltage transfer coefficient of the phase Detector (or) conversion gain given in volt/radians. and $\frac{\pi}{2}$ is the initial phase shift

O/P of Amp ie control voltage V_c which is given to VCO and it is given by

$$V_c = A \cdot V_e$$

$$V_c = A K\phi(\phi - \pi/2) \quad \text{---------} \quad (2)$$

$A \Rightarrow$ voltage gain of the Amp.

This V_c shifts (ie change) Vco o/p frequency from its free running frequency f_o to a new frequency 'f' is given by

$$f = f_o + K_v V_C \quad \text{---------} \quad (3)$$

$K_v \Rightarrow$ voltage to frequency transfer Coefficient of the VCO. When PLL is Locked into signal frequency f_s, then we have

(Locked state) $f = f_s = f_o + K_v V_C$ ---------- (4).

$\frac{f_s - f_o}{K_v} = C_V$

From equations (2) and (4) we can write

$$V_c = \frac{f_s - f_o}{K_v} = A K\phi\left[\phi - \frac{\pi}{2}\right]$$

$$\phi = \frac{\pi}{2} + \frac{f_s - f_o}{K_v K\phi A}.$$

$f = f_o + K_v \cdot A K\phi (\phi - \pi/2)$

From (4)

$f_s - f_o = K_v \cdot V_C$

V_C

$\frac{f_s - f_o}{K_v} =$

The ma
d
$V_{s(m}$

From phase detector.

The maximum control voltage and deviation occurs when $\phi = 0$ radian or $\phi = \pi$ radian, substituting these values in V_c

$V_{c(max)} = \pm K\phi \pi/2$

$V_{c(max)} = AK\phi\left[\phi - \frac{\pi}{2}\right]$ we get

$V_c = K\phi(\phi - \pi/2)$

$V_{c(max)} = \pm K\phi \pi/2$

$\pm$ is omitted since peak swing is considered

$$\boxed{V_{c\,max} = \pm \pi/2\, K\phi\, A} \quad \text{—— (5)}$$

Sub (5) in (4)

The maximum VCO frequency swing that can be obtained by is given by

$$(f - f_o)_{max} = K_v V_{c\,max} = K_v K\phi A\, \pi/2 \quad \text{—— (6).}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be.

Sub (5) in (4)

$$f = f_s = f_o \pm \underbrace{\cancel{(f - f_o)_{max}}}_{K_v \cdot V_c} = f_o \pm K_v K\phi (\pi/2) A = f_o \pm \Delta f_L \quad \text{—— (7)}$$

Where $2\Delta f_L$ will be the lock-in frequency range and is given by

Lock in Range $= 2\Delta f_L = K_v K\phi A \pi$ from exp (7)

(or) $\boxed{\Delta f_L = \pm K_v K\phi A\, \pi/2}$ —— (8)

The lock in range is symmetrically located with respect to VCO free running frequency f_o, for IC 565 PLL.

$$K_v = \frac{8 f_o}{V}$$

Where $V = +V_{cc} - (-V_{cc})$

and the o/p voltage of phase detector is limited by to a max of $\pm 0.7V$ and so $K\phi$ is given as

$$K\phi = \frac{0.7 - (-0.7)V}{\pi} = \frac{1.4}{\pi} \text{ and } A = 1.4$$

Sub $K\phi$, K_v and A value in exp (8)

$$\cancel{K\phi} = \Delta f_L = \frac{1.4}{\pi} \times \frac{8 f_o}{V} \times 1.4 \times \pi/2$$

$$\boxed{\Delta f_L = \pm 7.84 \frac{f_o}{V}}$$

Derivation in Capture Range

Initially, when PLL is not locked to the signal, the frequency of the Vco will be free running frequency f_o. The phase angle difference between the signal and the Vco o/p voltage will be

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o)t + \Delta\theta \quad \text{— (1)}$$

The phase angle difference ~~is~~ does not remain constant but will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o \quad \text{— (2)}$$

The phase detector o/p voltage will therefor not have dc component but it produce ac o/p with triangular waveform of peak amplitude $K\phi(\pi/2)$

fundamental frequency $(f_s - f_o) = \Delta f$

LPF is a RC Network with transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)}, \quad f_1 = \frac{1}{2\pi RC} \text{ is the 3dB point of LPF.}$$

For the condition that ~~Slope of LPF~~ where $(f/f_1)^2 >> 1$ then transfer function can be expressed approximately as.

$$T(f) = \frac{f_1}{jf} \quad \text{— (3)}$$

The fundamental frequency term $(f_s - f_o) = \Delta f$ is given to LPF. If $\boxed{\Delta f > 3 f_1}$, the transfer function of LPF will be approximately as

$$T(\Delta f) \simeq f/\Delta f = \frac{f}{f_s - f_o} \quad \text{— (4)}$$

The voltage Vc to drive the Vco is

$$V_c = V_e \times T(f) \times A \quad \text{— (5)}$$

or $V_c(max) = V_e(max) \times T(f) \times A$

$$= \pm K_\phi (\pi/2) A \,(f_1/\Delta f). \quad \text{—— (6)}$$

For the acquisition of signal frequency, put $f = f_s$. So the maximum signal frequency range that can be acquired by PLL is

$$(f - f_0) = (f_s - f_0)_{max} = \pm K_v K_\phi (\pi/2) A \cdot (f_1/\Delta f) \quad \text{—— (7)}$$

$$\pm K_v (V_{c\,max})$$

Now $\underline{\Delta f_c} = (f_s - f_0)_{max}$.

$$\Delta f_c = \pm K_\phi K_v (\pi/2) \cdot A \cdot \left(\frac{f_1}{\Delta f_c}\right)$$

$$(\Delta f_c)^2 = \pm K_\phi K_v (\pi/2) \cdot A \cdot f_1. \quad \text{—— (8)}$$

Since $\Delta f_L = \pm K_v K_\phi (\pi/2) A$ —— (9)

$\cancel{\Delta f_L = (\Delta f_L)^2 \cdot f_1}$.

Sub (9) in (8)

$$(\Delta f_c)^2 = \Delta f_L \cdot f_1$$

$$\boxed{\Delta f_c \simeq \pm\sqrt{\Delta f_L \cdot f_1}.} \quad \text{—— (10)}$$

Therefor total capture range is

$$2\Delta f_c = 2\sqrt{f_1 \Delta f_L}$$

Where the lock in-range $= 2\Delta f_L = K_v K_\phi A \cdot \pi$

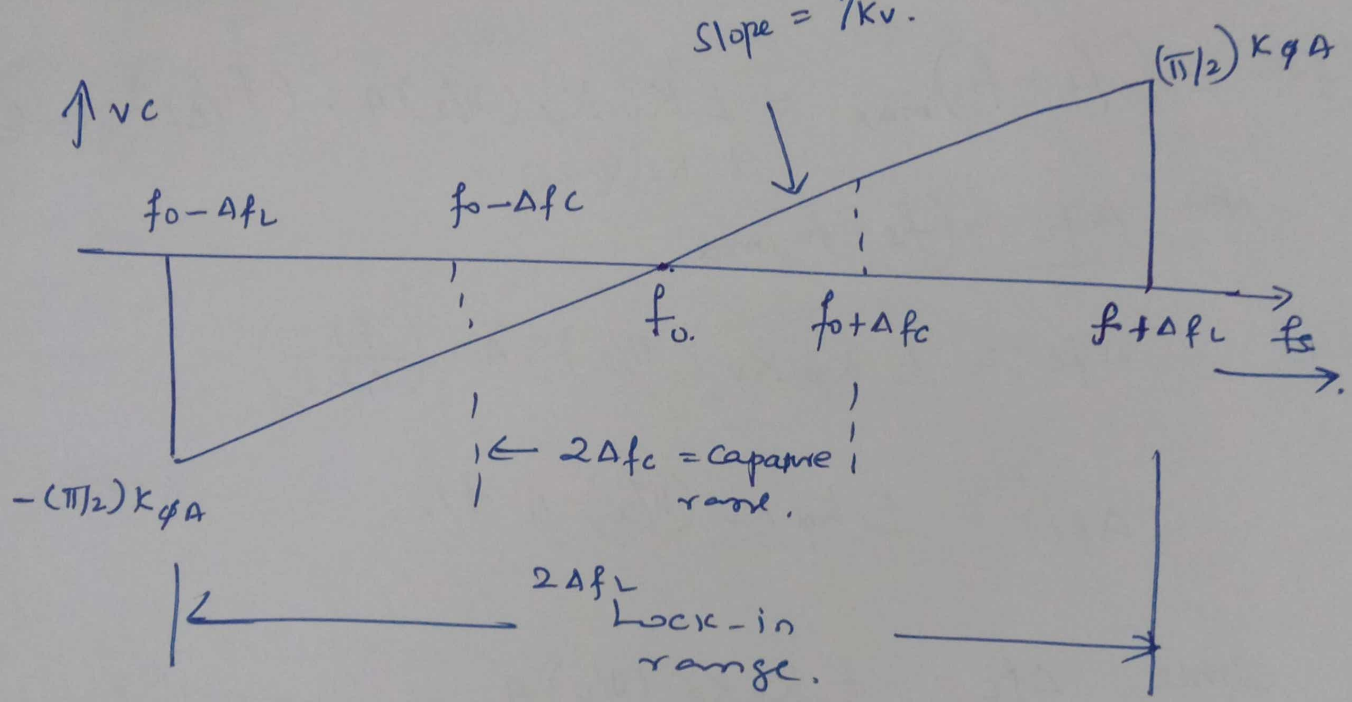
for PLL 565 $R = 3.6\,k\Omega$, so the capture range is

$$\Delta f_c \pm \left[\frac{\Delta f_L}{2\pi (3.6 \times 10^3) C}\right]^{1/2}$$

NOTE: Large capature Range will make a PLL more susceptible to Noise and undesirable signal.

→ So capacture Range Always less than lock in Range.

→ LPF BW initialy set for a larger value, for signal acquisition once the signal captured, the BW of LPF is redued, to minimise the interference.



PLL Loock Range – and – Capatre Range.

Problem: For a PLL circuit with following parameters determine free-running frequency of VCO f_o, the Lock range f_L and capture Range f_c of PLL and illustrate the relationship between f_o, f_L and f_C.

the parameters are

(i) supply voltages $+V = 10V$, $-V = -10V$

(ii) $R_1 = 12k\Omega$, $C_1 = 0.01\mu f$

(iii) RC N/W, $R = 3.6k\Omega$, $C = 10\mu f$

Determine the free-running frequency

$$f_o = \frac{1.2}{4R_1C_1}$$

$$= \frac{1.2}{4 \times (12\times10^3)\times(0.01\times10^{-6})} = 2500Hz = 2.5kHz$$

Lock Range can be determined by exp.

$$\boxed{f_L = \pm 7.84\frac{f_o}{V}} = 7.84\ \frac{2500}{20}$$

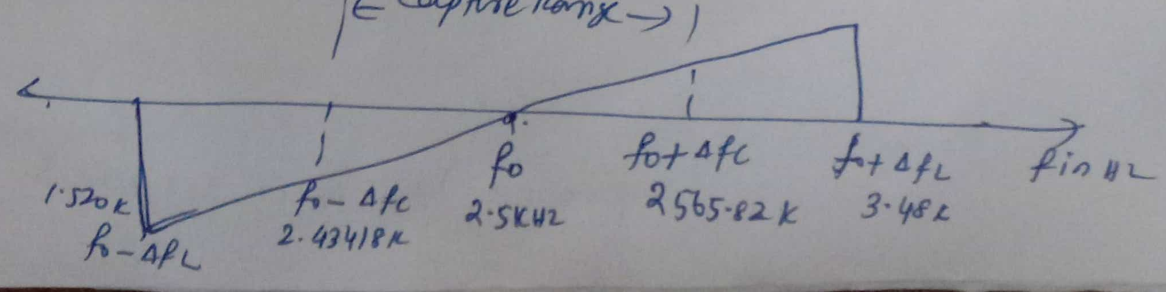
$$\Delta f_L = \pm 980Hz$$

$V = (V_{CC} - (-V_{CC}) = 10 - (-10) = 20V$.

Capature Range

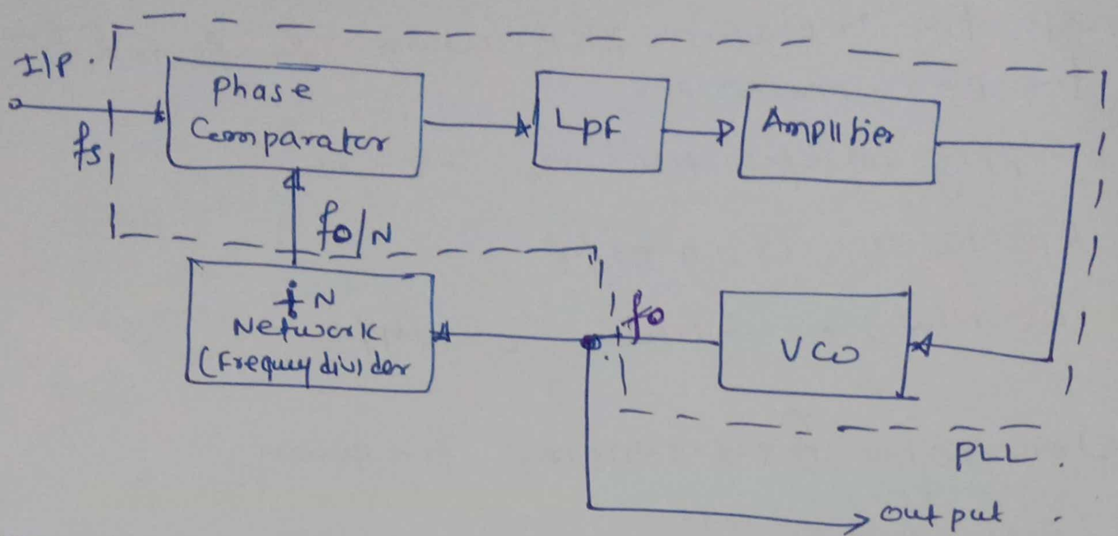
$$\Delta f_c = \pm\left[\frac{\Delta f_L}{2\pi(3.6k\Omega)\cdot C}\right]^{1/2}$$

$$= \pm\frac{980Hz}{2\pi\times3.6\times10^3\times10\times10^{-6}} = 65.82Hz$$



PLL APPLICATIONS

Frequency multiplication / Division



$f_o = N f_s$

From fig, $\div$N Network inserted between VCO output and phase comparator input.

In Locked state, the VCO o/p frequency f_o is given by (PLL)

$$\boxed{f_o = N f_s}$$

~~Multiplication factor is obtained~~ By selecting a proper scaling factor N of the counter (ie $\div$ by N Network), we can obtain desired multiplication.

Division: Since the VCO output (a square wave) is rich in Harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s.

The output f_o of VCO is now given by

$$\boxed{f_o = \frac{f_s}{m}}$$

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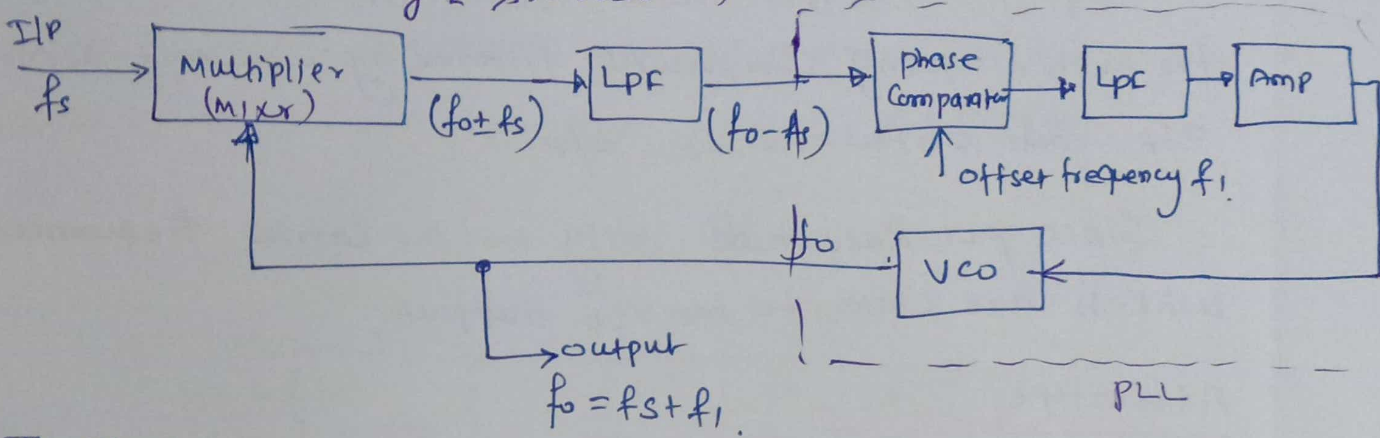
exm: $f_o = 6 f_s$.

N = 6 we should select N = 6

Frequency Translation:

Shifting the frequency of an osilator by a small factor.



The I/P to the phase Detector is

(i) offset frequency f_1 and $(f_o - f_s)$

During Locked State, o/p frequency is adjusted to make two input frequencies of phase Detector equal.

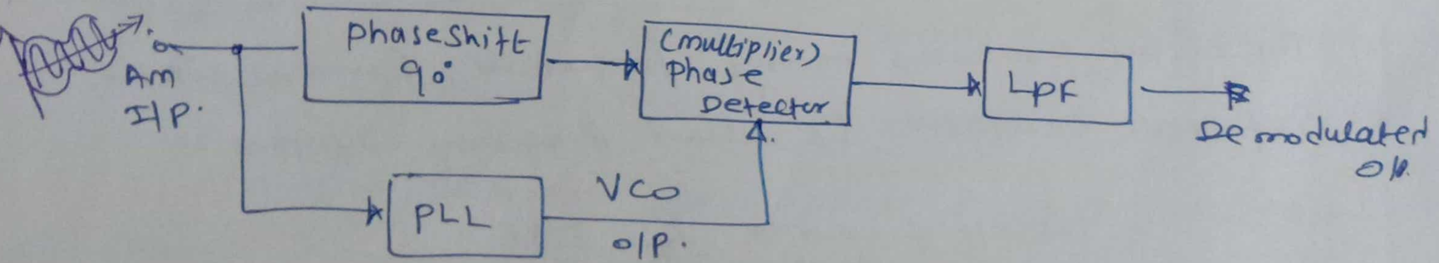
This gives,

$$f_o - f_s = f_1$$

$$\therefore \boxed{f_o = f_s + f_1}$$

ie, the o/p frequency is the sum of input frequency and offset frequency. By adjusting the offset frequency f_1 we can shift the frequency of the osilator to the desired value.

AM Detection



PLL is used to demodulate the Am Signals.

PLL is locked to the carrier frequency of I/P Signals once Locked, The output of VCO has the Same frequency of Carrier, but it Unmodulated signal fed into the detector.

Since VCO output always 90° out of phase with the incoming signals under the Locked Condition, the Am Signal also shifted by 90° before being fed into detector.

this makes both the signals applied to the mult in same phase.

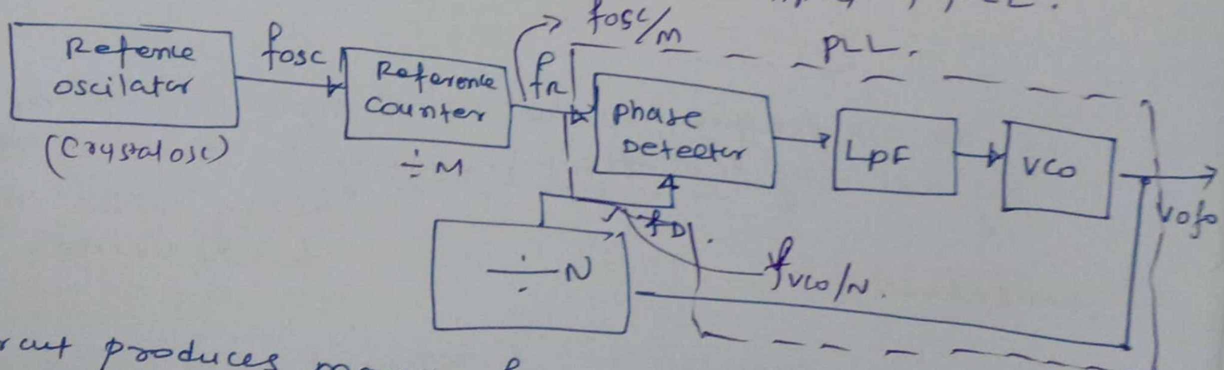
O/P of multiplier contain sum and difference frequency the high frequency component filtered by LPF and demodulated o/p at obtained at o/p.

Since PLL Responds only to the carrier frequencies which are close to the VCO output.

Advantage

① High degree of selectivity
② Noise immunity is more. compare to peak detector.

Frequency synthesizer: Same as frequency multiplier except the divide by M network is added at the input of PLL.



The circuit produces many frequencies from a single reference oscilator is called frequency synthesizer.

The o/p of counter $(\div M)$ $f_R = \frac{f_{osc}}{M}$

under Locked state $f_R = f_D = \frac{f_{vco}}{N}$ $\therefore \boxed{f_o = N f_R}$

$\hookrightarrow f_{osc}/M = f_{vco}/N$.

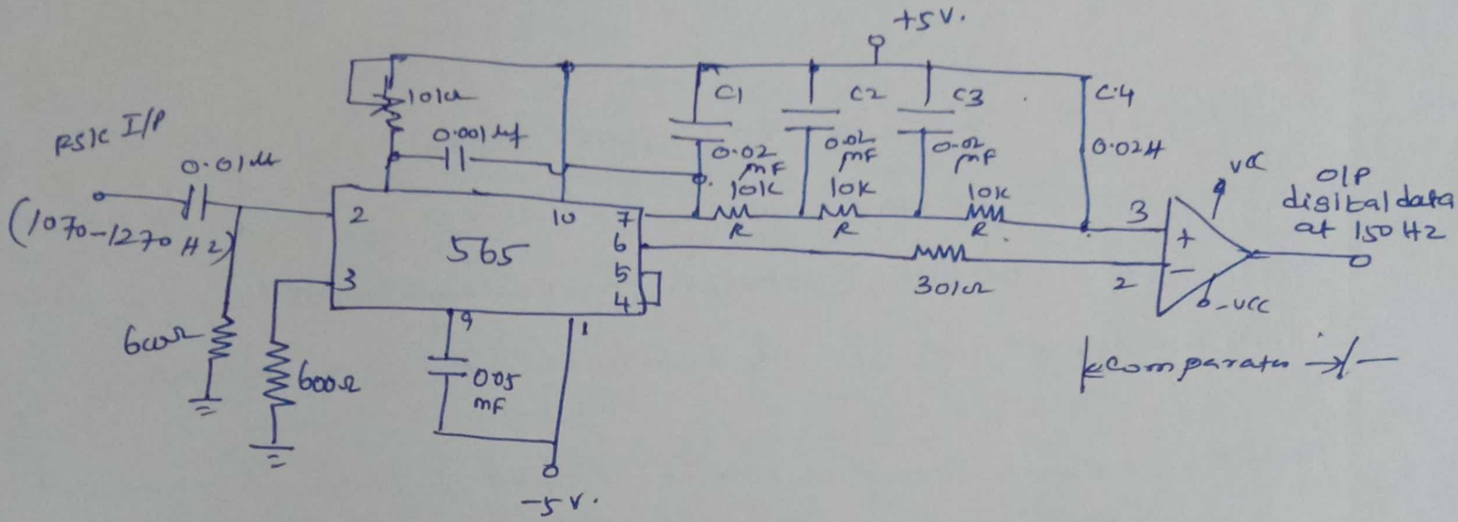
so that $f_{vco} = (N/M)\, f_{osc}$.

By adjusting divider counts to desired value large no of frequencies can be produced, all drived form the crystal oscilator

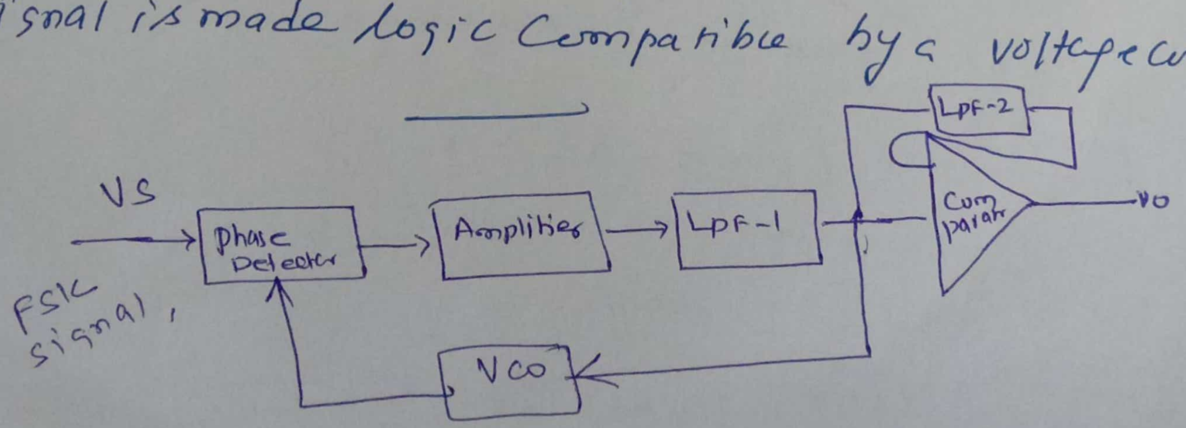
FSK Demodulator:

Frequency shift keying.

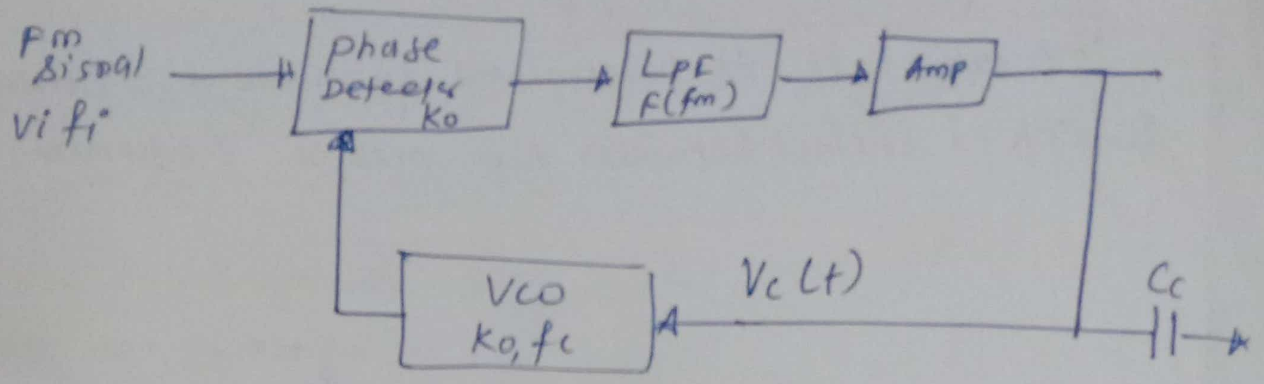
Binary data is transmitted by means of a carrier frequency which is shifted between two present frequencies.



FSK demodulator for tele-typewriter signals of 1070Hz and 1270Hz. As the signal appears at the I/P, the loop locks to the Input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A Three stage RC Filter remove the carrier component and the output signal is made logic compatible by a voltage comparator



Fm Demodulator



if PLL is Locked to a Fm signal, VCO tracks the instantaneous frequency of the I/P signal. The filtered error voltage which controls the vco and maintains a lock with the I/P signal is the demodulated Fm output.

problem: A PLL with a free running frequency of 1KHz is connected to a variable frequency oscilator. The frequency of oscilator gradually increased and when its frequency was 850 Hz, the PLL got locked. The frequency of oscilator was decreased and it went to out of lock for the oscilator frequency of 800 Hz. Calculate the lock range and capture range of PLL.

Capture Range

$$\Delta f_c = |f_i - f_o| = |f - f_o|$$

$$= |850\,Hz - 1KHz|$$

$$\Delta f_c = 150\,Hz$$

$2\Delta f_c = 300\,Hz$ is the Capture Range

Lock Range

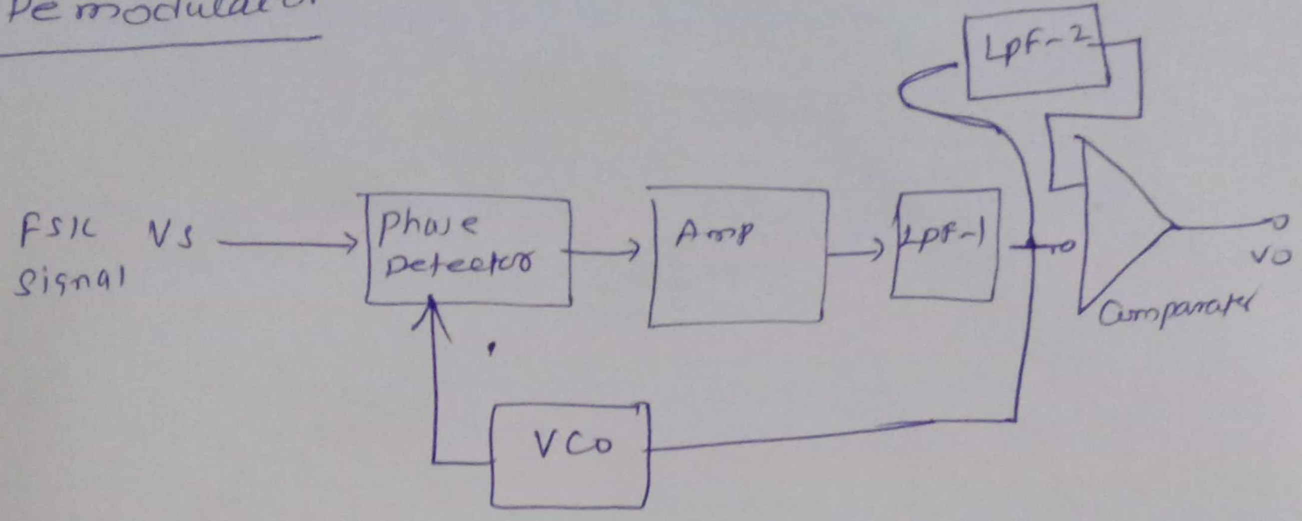
$$\Delta f_L = |f_i - f_o| = |f - f_o|$$

$$= |800\,Hz - 1KHz|$$

$$\Delta f_L = 200\,Hz$$

$2\Delta f_L = 400\,Hz$ is the lock Range.

FSK Demodulator



In Digital data transmission, binary data is transmitted by means of a carrier frequency. It uses two different carrier frequency for logic 1 and logic 0 states of binary data signal. This type of transmission called FSK.

On the receiving end, two carrier frequencies are converted into 1 and 0 to get the original binary data. This process is called FSK Demodulation.

Comparator: produce a reconstructed digital o/p signal

Let consider two frequencies.

f_1 — represented as '0'

f_2 — " '1'.

If PLL remain locked into the FSK signal at both f_1 and f_2, the VCO voltage which is also ~~supplied~~ supplied to the comparator will be given as

$$V_{C1} = (f_1 - f_0) / K_V$$

$$V_{C2} = (f_2 - f_0) / K_V.$$

The difference between two control level is $\Delta V_C = (f_2 - f_1) / K_V$.

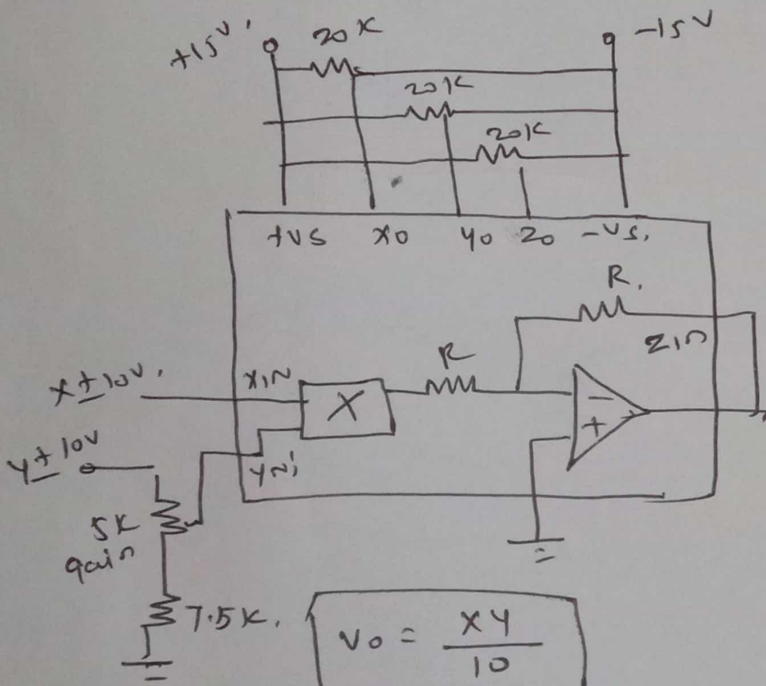
The reference voltage for the comparator is derived from LPF-2 and it is adjusted midway between V_{C1} and V_{C2}. Therefore, for V_{C1} and V_{C2}, comparator ~~op~~ gives o/p '1' and

Analog multiplier IC AD 532 :

Featrus:

1. only four external adjusmet are neccery.
2. maximum four quadrant error is below 0.5%.
3. Temp drift is as Low as 0.01 % / °C
4. Simple operetions.

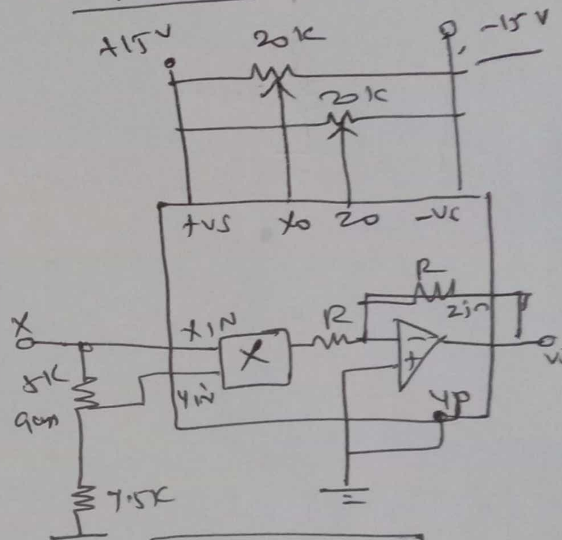
Applications: 1. multiplier



$$\boxed{V_o = \frac{XY}{10}}$$

X_0 and Y_0 is null pot used for balancing operation.
Z_0 pot compansate the o/p opamp offset voltage.
Gain pot sets the fullscale o/p level.

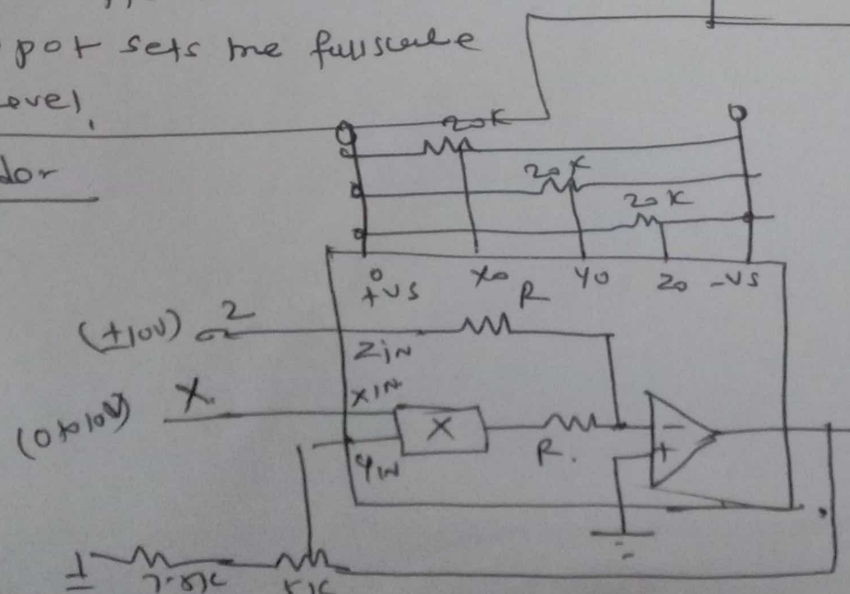
2. squarer



$$\boxed{V_o = \frac{X^2}{10}} = \frac{XY}{10}$$

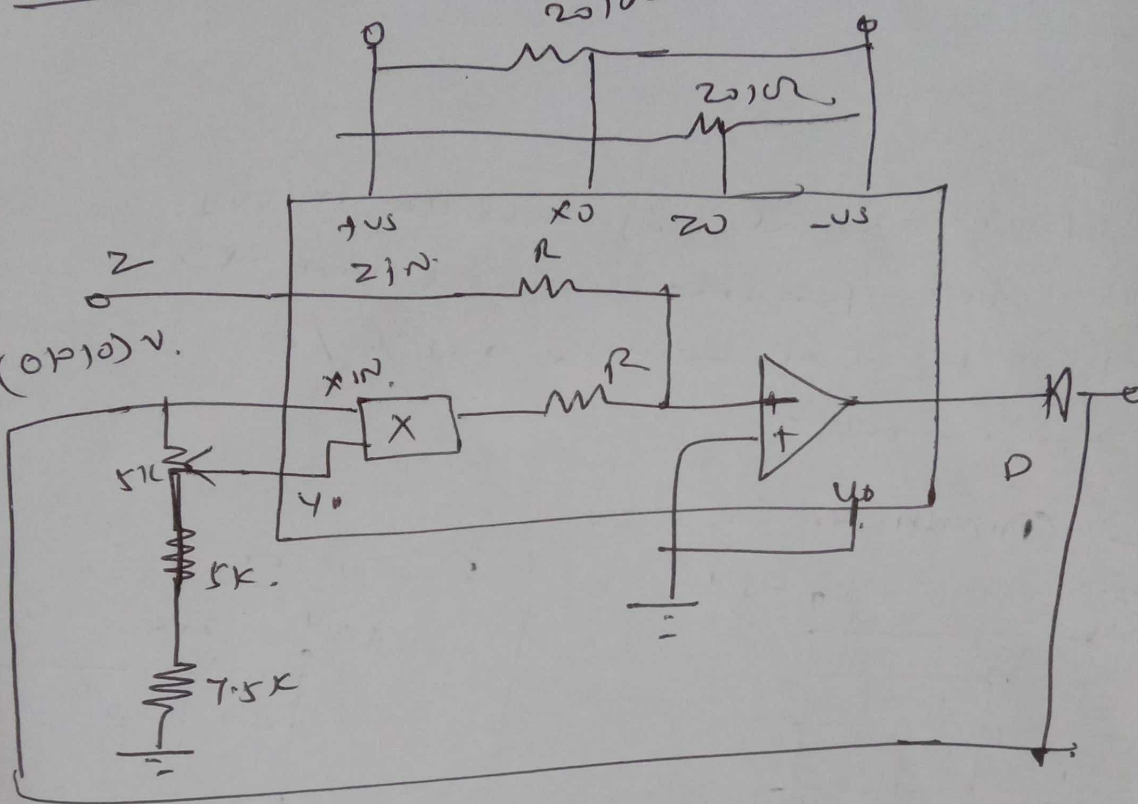
It provides two quadrant operation, X and Y connected togather. o/p always +ve

Divider



$$\boxed{V_o = \frac{10Z}{X}}$$

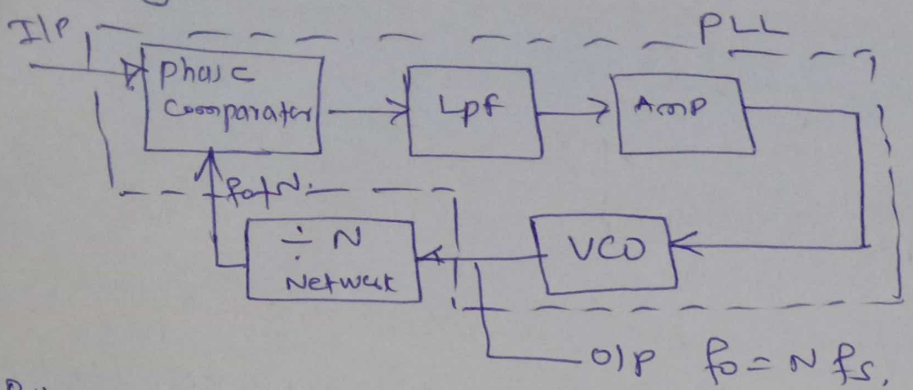
Square root:



$V_0 = \frac{\sqrt{10Z}}{X}$

PLL Application

① Frequency Multiplication / Division.

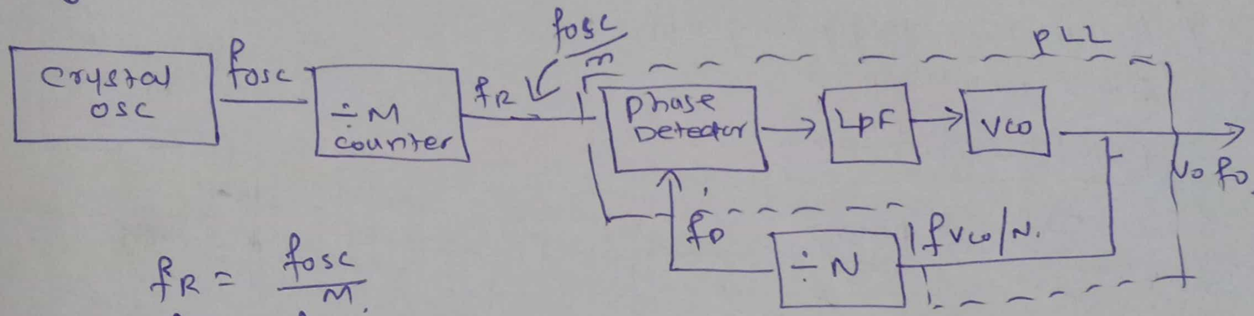


Divider

$f_o = f_s / m$

By proper selection of scaling factor, we can obtain Desired multiplication

② Frequency synthesizer



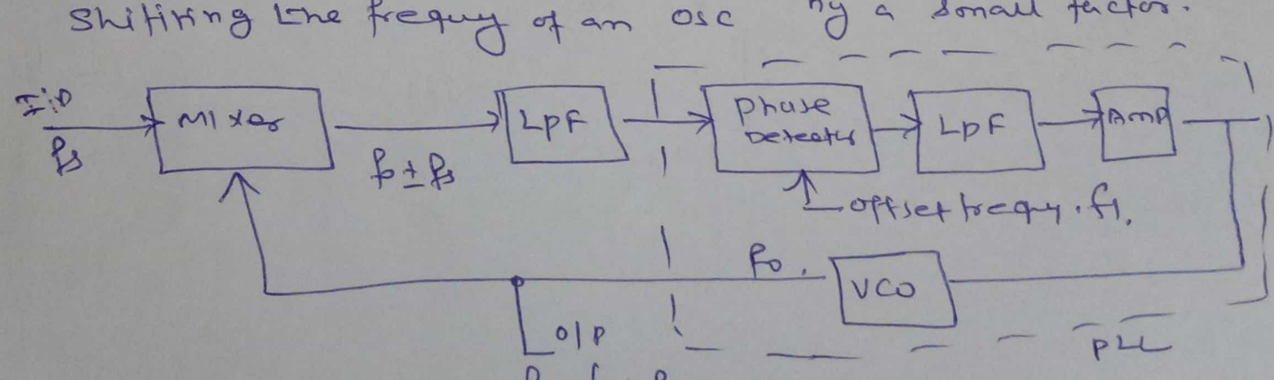
$f_R = \frac{f_{osc}}{M}$

$f_D = \frac{f_{vco}}{N}$

Under Locked condition, $f_{osc}/M = f_{vco}/N$, so $f_{vco} = (N/M) f_{osc}$.
By adjusting divider counter to desired value large no of frequencies can be produced.

③ Frequency Translation

Shifting the frequency of an osc by a small factor.



$f_o = f_s + f_1$

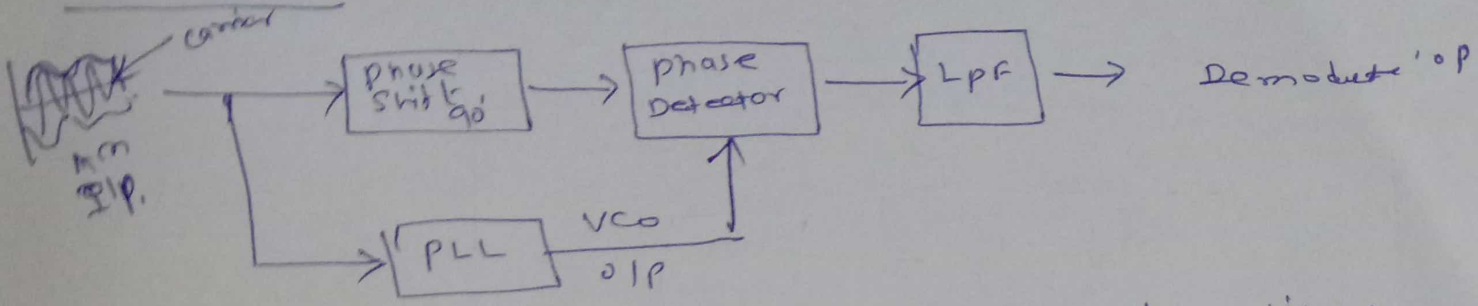
During Locking state

$f_o - f_s = f_1$

$f_o = f_s + f_1$

O/P. ~~frequency~~. By adjusting the offset frequency f_1, we can shift the frequency of the oscillator to the desired value.

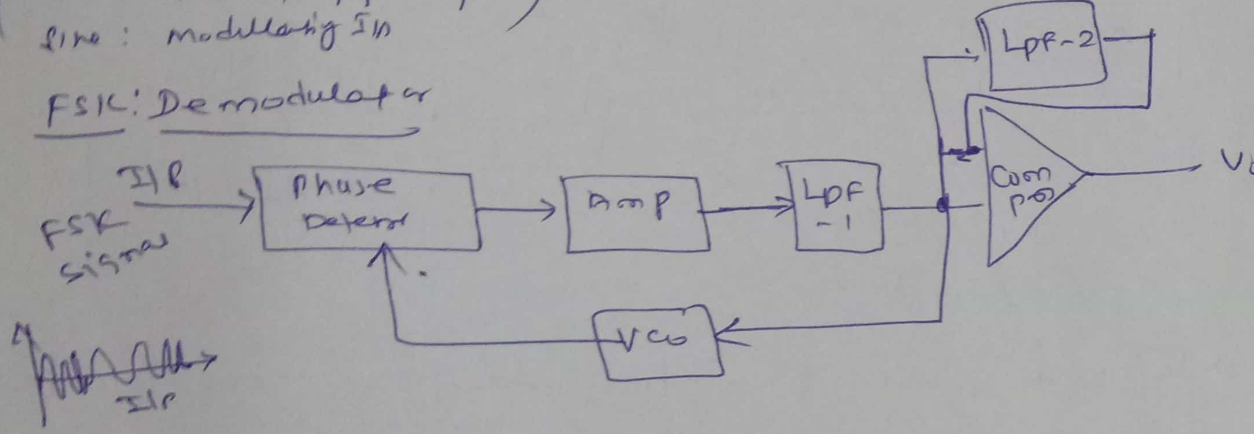
Am Detection



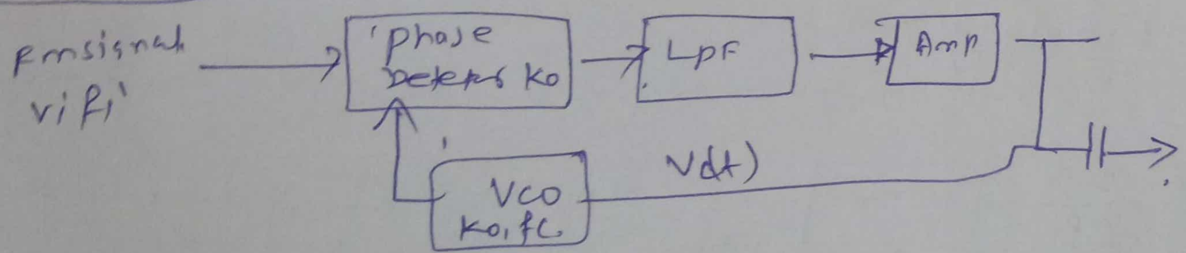
Vco o/p always 90° out of phase with incoming signal under locking condition, and Am signal also shifted to 90° Both fed into detector with same phase. Then low frequency components filtered by LPF and demodulated o/p obtained at o/p

(Carrier - High frequency component
Sine : modulating Sin)

FSK: Demodulator



Fm Demodulator



Capture Range:

initialy, PLL is not locked, Vco frequency will be the free running frequency f_o - Let phase angle (ϕ) difference between the signal and the VCO O/P voltage will be.

$$\phi = \underbrace{(W_s t + \theta_s)}_{I/P} - \underbrace{(W_o t + \theta_o)}_{VCO\,O/P} = (W_s - W_o)t + \Delta\theta \quad — ①$$

ϕ - not constant so

$$\frac{d\phi}{dt} = W_s - W_o \quad — ②$$

→ Fundamental frequency $(f_s - f_o) = \Delta f$

→ LPF is a RC N/W, with TF $= T(jf) = \dfrac{1}{1 + j(f/f_1)}$ $\quad f_1 = \dfrac{1}{2\pi RC}$ is the 3dB point of LPF

For this condition that $\left(f/f_1\right)^2 >> 1$, then T.F can be expressed approximately as.

$$\boxed{T(f) = \frac{f_1}{jf}} \quad — ③$$

Δf is applied to LPF

if $\Delta f > 3f_1$, then TF of LPF is approximated as

$$\boxed{T(\Delta f) \approx \frac{f}{\Delta f} = \frac{f}{f_s - f_o}} \quad — ④$$

Let $V_c = V_e \times T(f) \times A$ — ⑤

$$V_{c(max)} = V_{e(max)} \times T(f) \times A$$
$$= \pm K\phi(\pi/2).A \times f_1/\Delta f \quad — ⑥$$

For acquisition of signal frequency, put $f = f_s$, so max signal frequency Range that can be acquired by PLL is.

~~$(f - f_o) = (f_s - f_o)_{max} \pm K_v . V_{c(max)}$~~

$$(f - f_o) = \underline{(f_s - f_o)}_{max} = \pm K_v . V_{cmax}$$
$$= \pm K_v . K\phi(\pi/2) A . \times f_1/\Delta f_{cap}. \quad — ⑦$$

Now

$\Delta f_c = (f_s - f_o)_{max}$, so

$$\Delta f_c = \pm K\phi K_v (\pi/2) . A \left(f_1/\Delta f_{cap}\right)$$

$$(\Delta f_c)^2 = \pm K\phi K_v (\pi/2) . A . f_1 \quad — ⑧$$

Since $\Delta f_L = \pm K_v K\phi(\pi/2) A$ — ⑨

9 in 8 $\quad (\Delta f_c)^2 = \Delta f_L . f_1$

$$(\Delta f_c) \approx \pm\sqrt{\Delta f_L . f_1} \quad — ⑩$$

Therefore total capture Range

$$2\Delta f_c = 2\sqrt{\Delta f_L . f_1}$$

where the lock Range $2\Delta f_L$

$$= \underline{2\Delta f_L} = K_v K\phi A . \pi$$

For PLL, $R = 3.6 k\Omega$ the capture Range

$$\Delta f_c \pm \left[\frac{\Delta f_L}{2\pi(3.6 \times 10^3)C}\right]^{1/2}$$

Total capture Range $2\Delta f_{cap}$

Lock in Range

ϕ – radians – phase diff between V_i and VCO o/p V_o.

$\rightarrow$ phase angle to voltage tran coff.

$V_e = K\phi\,(\phi - \pi/2)$

$\rightarrow$ initial phase shift

$V_c = A \cdot V_e$

$= A \cdot K\phi\,(\phi - \pi/2)$ — (2)

V_c shifts $\underline{f_o \rightarrow f'}$

$f = f_o + K_V \cdot V_c$

$f_o + K_V \cdot A \cdot K\phi\,(\phi - \pi/2)$

Locked state

$f = f_s = f_o + K_V V_c$ — (3)

$f_s - f_o = K_V V_C$

$\boxed{\frac{f_s - f_o}{K_V} = V_C}$ — (4)

From eq (2) and (4)

$V_C = \frac{f_s - f_o}{K_V} = A \cdot K\phi\,(\phi - \pi/2)$ — (5)

$\boxed{\phi = \pi/2 + \frac{f_s - f_o}{K_V K\phi A}}$

~~$\Delta f_L = A \cdot K\phi\,[\phi - \pi/2]$~~

Max corr voltage occurs from PD when $\phi = 0$ and $\phi = \pi$

$V_e = K\phi\,(\phi - \pi/2)$

$V_e(max) = \pm K\phi\,\pi/2$

$|||^{ly}$ $V_{c\,max} = A K\phi\,[\phi - \pi/2]$

$\boxed{V_{c\,max} = \pm A K\phi\,\pi/2}$ — (5)

sub (5) in (3)

Let $f = f_s = f_o \pm K_V \cdot V_e$

$= f_o \pm K_V \cdot A \cdot K\phi\,[\phi - \pi/2]$

$= f_o \pm \Delta f_L$.

When $2\Delta f_L$ will be the lock in range are given by.

$2\Delta f_L = K_V K\phi A \cdot \pi$ $\therefore$ $\boxed{\Delta f_L = \pm K_V K\phi A\,\pi/2}$

$\phi = 0$

$K_V = \frac{8 f_o}{V}$

$K\phi = \frac{1.4}{\pi}$, $A = 1.4$

$\Delta f_L = \frac{1.4}{\pi} \times \frac{8 f_o}{V} \times 1.4 \times \pi/2$

$\Delta f_L = \pm 7.84 \frac{f_o}{V}$

EC8453 Linear Integrated Circuits

Unit 4

ADC Types

Successive Approximation (SAR) ADC.
Flash ADC
Single slope ADC
Dual Slope ADC.
Delta ADC
Delta-sigma (ΔΣ) ADC.
Pipelined ADC.

FLASH TYPE ADC

Flash type ADC produces an equivalent digital output for a corresponding analog input in no time. Hence, flash type ADC is the fastest.To convert the analog input voltage into a digital signal of n-bit output, $(2^n – 1)$ comparators are required

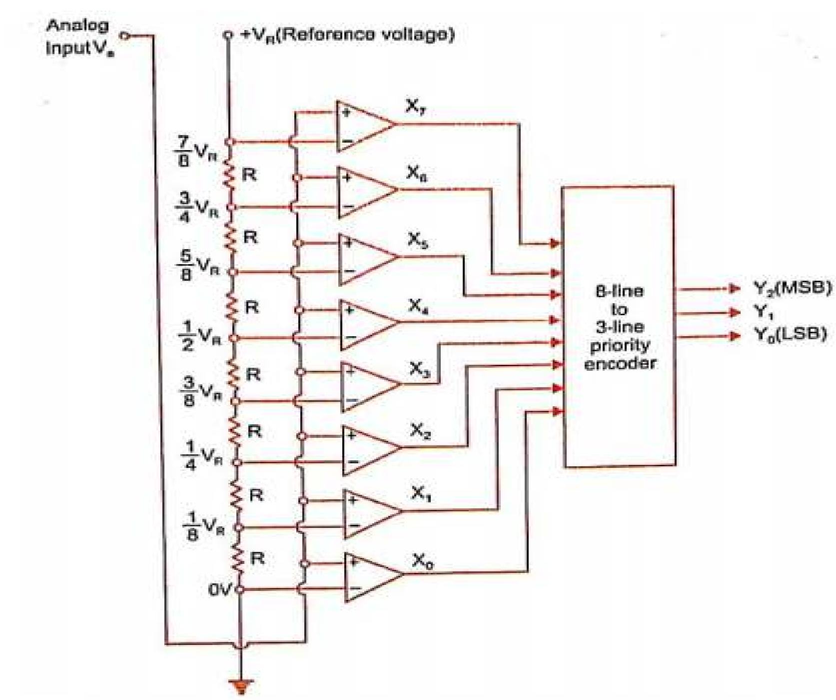


Figure . .Basic circuit for flash type A/D converter

Note: In this design Vref is 8V is used

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

The 3-bit flash type ADC consists of a voltage divider network, 7 comparators and a priority encoder.

The voltage divider network contains 8 equal resistors. A reference voltage VR is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom to top with respect to ground will be the integer multiples (from 1 to 8) of VR8

The external input voltage Vi is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top.

At a time, all the comparators compare the external input voltage with the voltage drops present at the respective other input terminal. That means, the comparison operations take place by each comparator parallelly.

- The output of the comparator will be '1' as long as Va is greater than the voltage drop present at the respective other input terminal.
- Similarly, the output of comparator will be '0', when, Va is less than or equal to the voltage drop present at the respective other input terminal.

All the outputs of comparators are connected as the inputs of priority encoder. This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has '1'.

Therefore, the output of priority encoder is nothing but the binary equivalent (digital tput) of external analog input voltage, Va

Flash ADC Advantages

- It is the fastest ADC and is utilized in high bandwidth applications.

Flash ADC Disadvantages

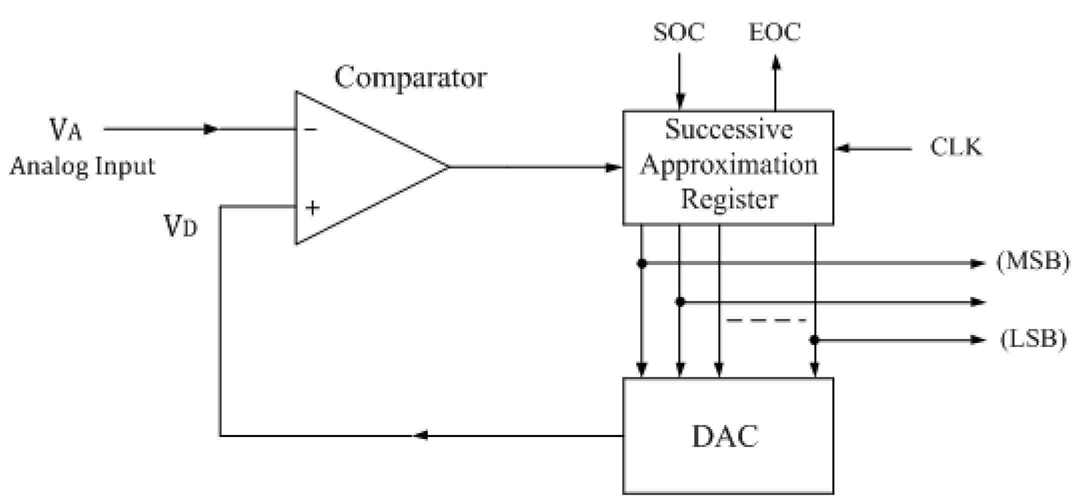
- These ADC are more power-consuming as compared to ADCs implemented with different techniques.
- It is a limited resolution of up to 8-bits.
- Increase bits lead to a large die area. With an 8-bit resolution, it needs a die area big enough to accommodate 255 comparators (2^N-1).
- The resistors and comparators should be matched to provide an accurate reference voltage to the comparators by the voltage divider network

Flash ADC Applications

- Satellite communication
- Radar processing
- Oscilloscopes

Successive Approximation ADC(https://www.electronics-tutorial.net)

Successive Approximation type ADC is the most widely used and popular ADC method. The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digitaloutput, unlike the counter and continuous type A/D converters. The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB



The functional block diagram of successive approximation type of ADC

It consists of a successive approximation register (SAR), DAC and comparator. The output of SAR is given to n-bit DAC. The equivalent analog output voltage of DAC, VD is applied to the non-inverting input of the comparator. The second input to the comparator is the unknown analog input voltage VA. The output of the comparator is used to activate the successive approximation logic of SAR.
When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000

The principle of successive approximation process for a 4-bit conversion is explained here. This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.

Step (1): The MSB is initially set to 1 with the remaining three bits set as 000. The digital equivalent voltage is compared with the unknown analog input voltage.

1000 MSB is 1 remaining three bits set as 000

Step (2): If the analog input voltage is higher than the digital equivalent voltage (VA >VD), the MSB is retained as 1 and the second MSB is set to 1.

1100 MSB 1 and second bit set to 1

Otherwise, the MSB is set to 0 and the second MSB is set to 1.

Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

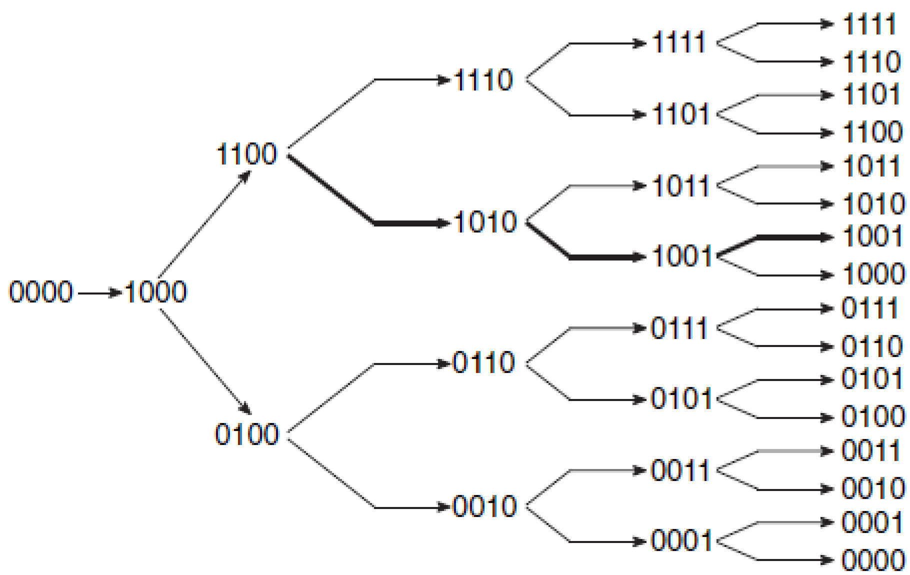
Let VA= 11V and Vref = 16V, in DAC output we get half of reference voltage ie 8V

The above steps are more accurately illustrated with the help of an example. Let us assume that the 4-bit ADC is used and the analog input voltage is VA = 11 V. when the conversion starts, the MSB bit is set to 1.
Now VA = 11V > VD = 8V = [1000]2

Since the unknown analog input voltage VA is higher than the equivalent digital voltage VD, as discussed in step (2), the MSB is retained as 1 and the next MSB bit is set to 1 as follows VD = 12V = [1100]2

Now VA = 11V < VD = 12V = [1100]2
Here now, the unknown analog input voltage VA is lower than the equivalent digital voltage VD. As discussed in step (2), the second MSB is set to 0 and next MSB set to 1 as VD = 10V = [1010]2

Now again VA = 11V > VD = 10V = [1010]2
Again as discussed in step (2) VA>VD, hence the third MSB is retained to 1 and the last bit is set to 1. The new code word is
VD = 11V = [1011]2
Now finally VA = VD , and the conversion stops.

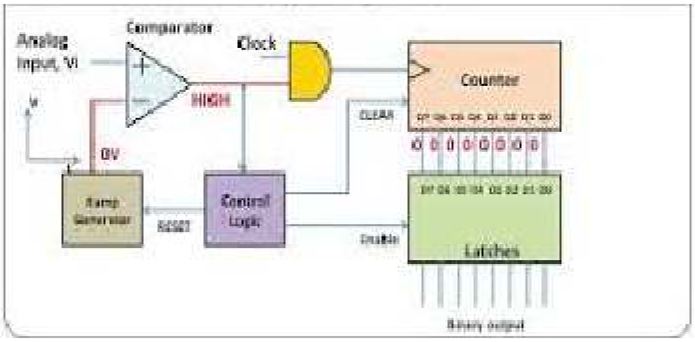


Conversion process in a successive approximation type A/D converter.

Advantages:
1 Conversion time is very small.
2 Conversion time is constant and independent of the amplitude of the analog input signal VA.

Disadvantages:
1 Circuit is complex.
2 The conversion time is more compared to flash type ADC.

Single Slope ADC



The above is the block diagram of single slope ADC. These converter techniques are based on comparing the unknown analog i/p voltage with a reference voltage that begins at 0v & increases linearly with time.The time required for the reference voltage to reach the value of unknown analog i/p voltage is proportional to the amplitude of unknown analog i/p voltage.

The time period can be measured using a digital counter. The main circuit of this converter is a ramp generator which on receiving a RESET from the control circuit increases linearly with time from 0v to a max volt Vm Assume a +ive analog i/p voltage Vi is applied at the non-inverting i/p of the comparator. **When a RESET signal is applied to the control logic, the 4-digit decade counter resets to 0 & the ramp begins to increase. Vi is +ive the comparator o/p is in HIGH state. This allows the clk pulse to pass to the i/p of the 4-digit counter through the AND gate & the counter is incremented. This process continues until the analog i/p voltage is greater than the ramp generator voltage.**

When the ramp generator voltage is equal to the analog i/p voltage, the comparator o/p becomes negatively saturated or logic 0.The clk is prevented from passing through the gate causing the counter operation. Then the control circuit generates a signal, which latches the counter values in the 4-digit latch, which is displayed on 7-segmant displays. The displayed value is then equivalent to the amplitude of analog input voltage.

Dual Slope Adc

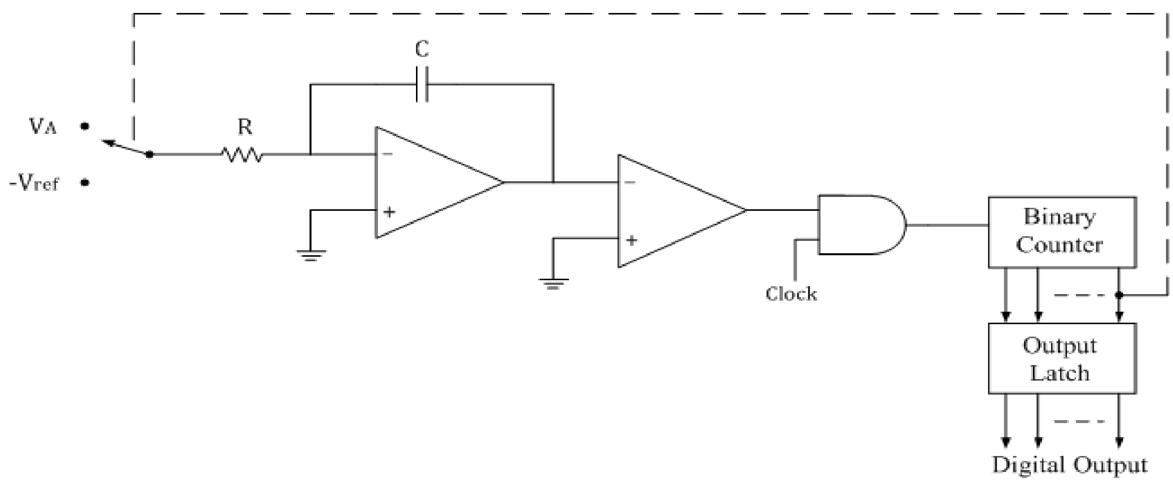
In dual slope type ADC, the integrator generates two different ramps, one with the known analog input voltage VA and another with a known reference voltage –Vref. Hence it is called a s dual slope A to D converter. The logic diagram for the same is shown below

Operation:

The binary counter is initially reset to 0000; the output of integrator reset to 0V and the input to the ramp generator or integrator is switched to the unknown analog input voltage VA. The analog input voltage VA is integrated by the inverting integrator and generates a negative ramp output. The output of comparator is positive and the clock is passed through the AND gate.

This results in counting up of the binary counter.
The negative ramp continues for a fixed time period t1, which is determined by a count detector for the time period t1. At the end of the fixed time period t1, the ramp output of integrator is given by

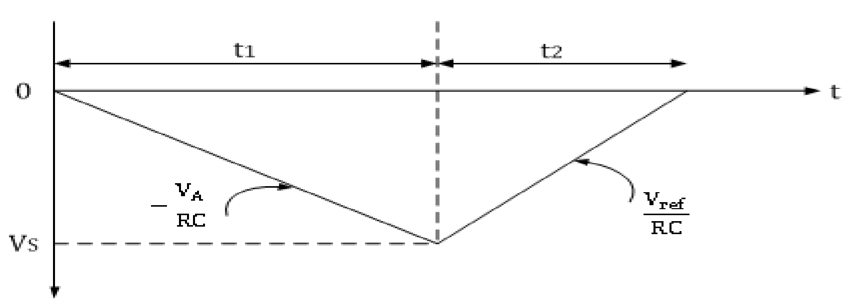
∴VS=-VA/RC×t1



When the counter reaches the fixed count at time period t1, the binary counter resets to 0000 and switches the integrator input to a negative reference voltage –Vref.
Now the ramp generator starts with the initial value –Vs and increases in positive direction until it reaches 0V and the counter gets advanced. When Vs reaches 0V, comparator output becomes negative (i.e. logic 0) and the AND gate is deactivated. Hence no further clock is applied through AND gate. Now, the conversion cycle is said to be completed and the positive ramp voltage is given by

∴VS=Vref/RC×t2

Where Vref & RC are constants and time period t2 is variable.
The dual ramp output waveform is shown below



Since ramp generator voltage starts at 0V, decreasing down to –Vs and then increasing up to 0V, the amplitude of negative and positive ramp voltages can be equated as follows.

$\therefore V_{ref}/RC \times t2 = -VA/RC \times t1$
$\therefore t2 = -t1 \times VA/V_{ref}$
$\therefore VA = -V_{ref} \times t1/t2$

Thus the unknown analog input voltage VA is proportional to the time period t2, because Vref is a known reference voltage and t1 is the predetermined time period.

The actual conversion of analog voltage VA into a digital count occurs during time t2. The binary counter gives corresponding digital value for time period t2. The clock is connected to the counter at the beginning of t2 and is disconnected at the end of t2. Thus the counter counts digital output as

Digital output=(counts/sec) t2
∴Digital output=(counts/sec)[t1×VA/Vref]

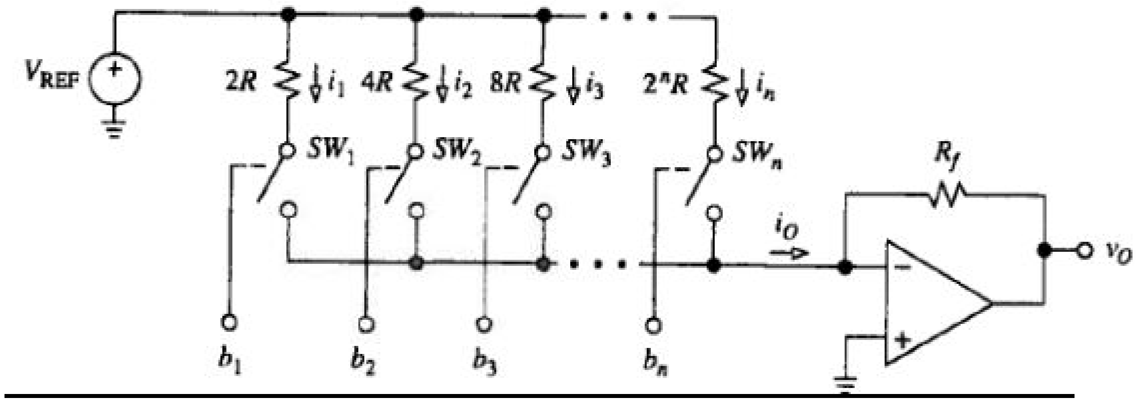
DAC

A **Digital to Analog Converter (DAC)** converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1

Types of DACs

There are **two types** of DACs

- Weighted Resistor DAC
- R-2R Ladder DAC



Advantages/Disadvantages of weighted resistor method

1. The Resistors that are being used in the network have a wide variety of values present that ensures the stability and the absolute accuracy across all the resistors

When the n given by the user is large, the corresponding resistance provided to LBS is considered to be a large value. If it is compared with the provided input resistance of the Amplifier. This all leads to accurate results

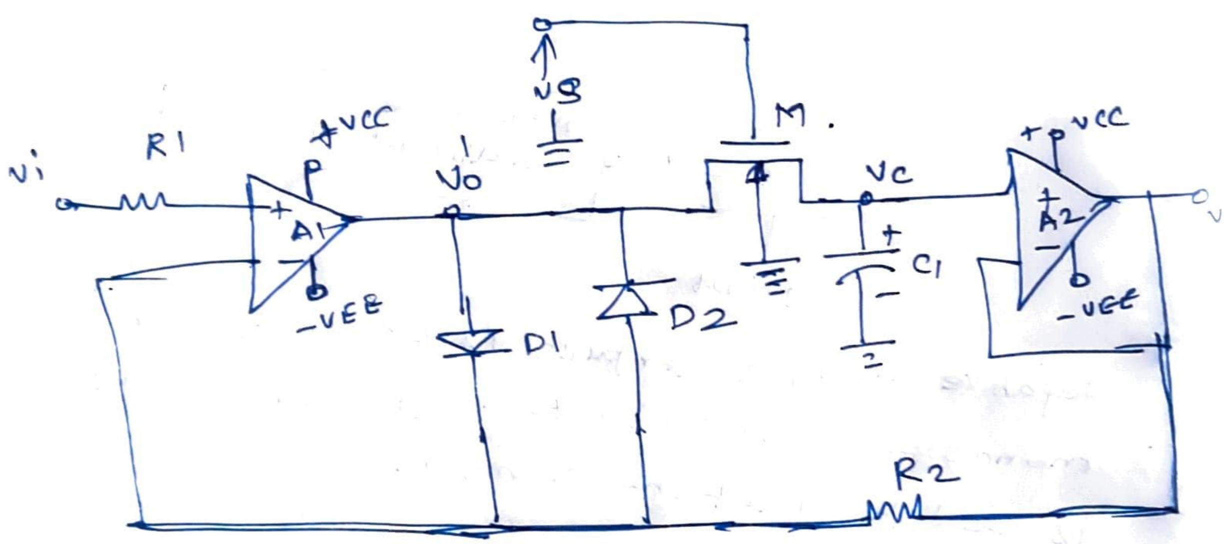
1. N number of switches that represents a bit applied to the input provided.
2. A ladder network supported by a weighted resistor. The resistor is inversely proportional to the corresponding binary digital signal.
3. A reference voltage V ref provided
4. A summing Amplifier

High speed Sample and HOLD circuits

The circuit takes a samples from the analog I/P signal and holds it for a particular period of time is known as high speed Sample and hold circuits.

Sampling Time: The circuit switch allows samples of I/P for short duration time.

Holding Time: The value is holded by a capacitor for holding time

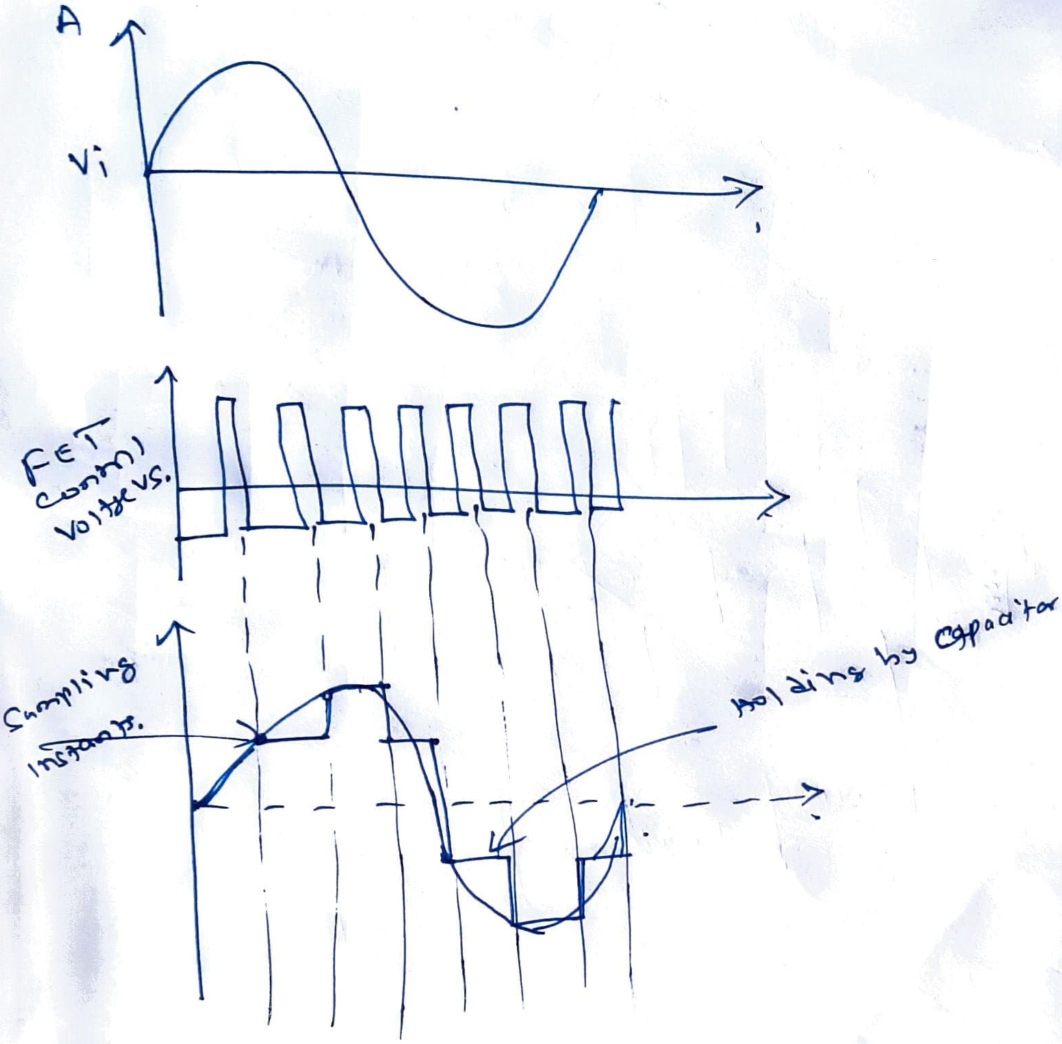


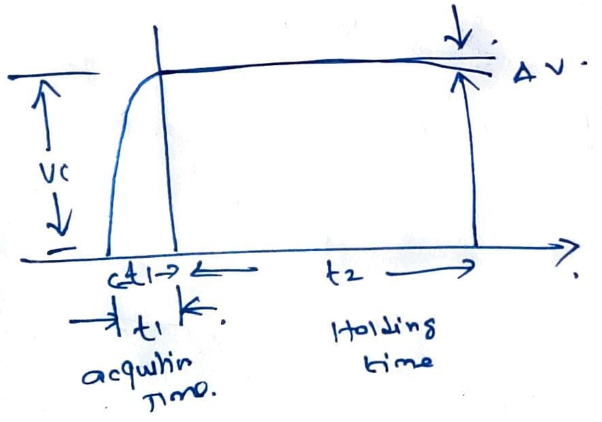
The sample and HOLD circuit uses a basic compar~~amar~~ switch, OPAMP and MOSFET, Diodes,

When Vs is given, M-switch is ON, A1 and A2 act as voltage follower, switch ON, capacitor is charging to maximum value ~~and discharge~~.

When Vs is OFF period, the MOSFET M switches OFF and capacitor Hold the value and retains it until next sample comes in.

T1 = acquisition time
T2 = is Holding time.



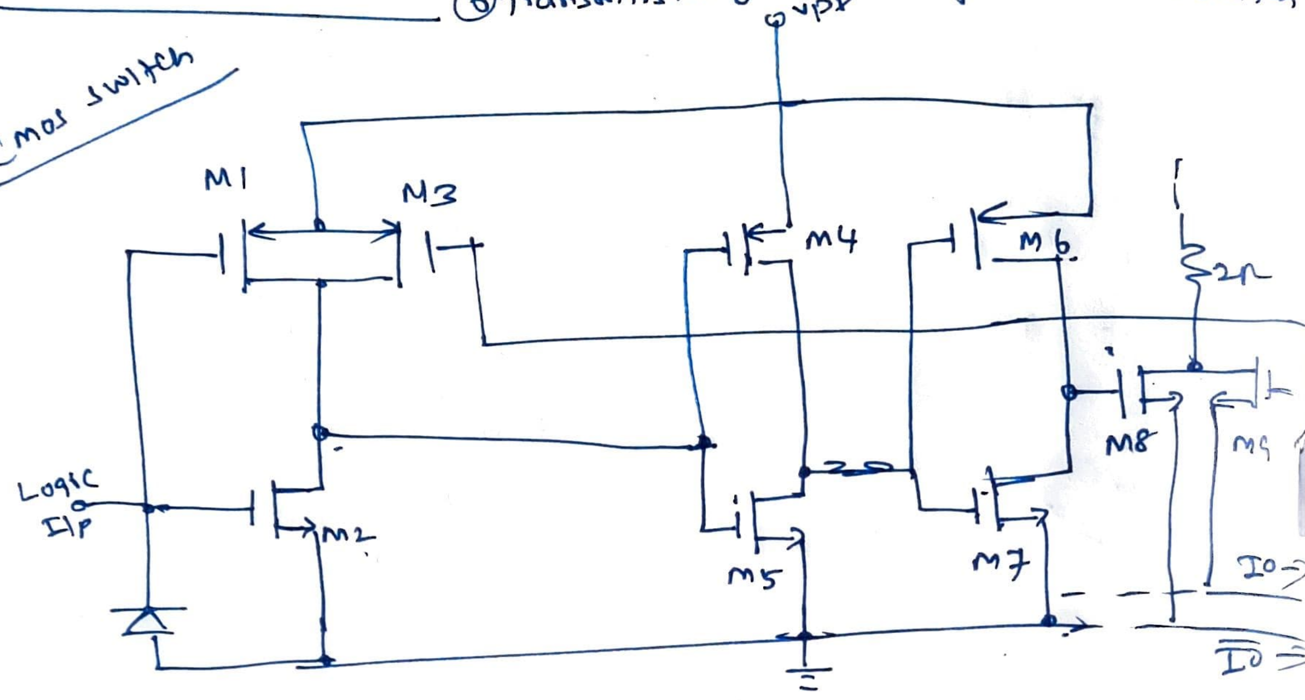


During Holding time, the capacitor slowly discharges to produce the change in amplitude (ΔV). This is known as droop. To avoid this, capacitors are selected with less Leakage during holding time.

① cmos switch ② BJT switch ③ Totem pole switch
④ cmos inverter switch, ⑤ multiplying DAC switch
⑥ Transmission gate switch

Switches for DAC

Cmos switch



Cmos switch. Switch consist of pair of Nmos Transistor. M8 - M9. The transistor M1 - M7 capable of accepting TTL and cmos compatible Logic I/P

When the I/P is Logic High, M8 - OFF, M9 - ON and 2R connected to IO

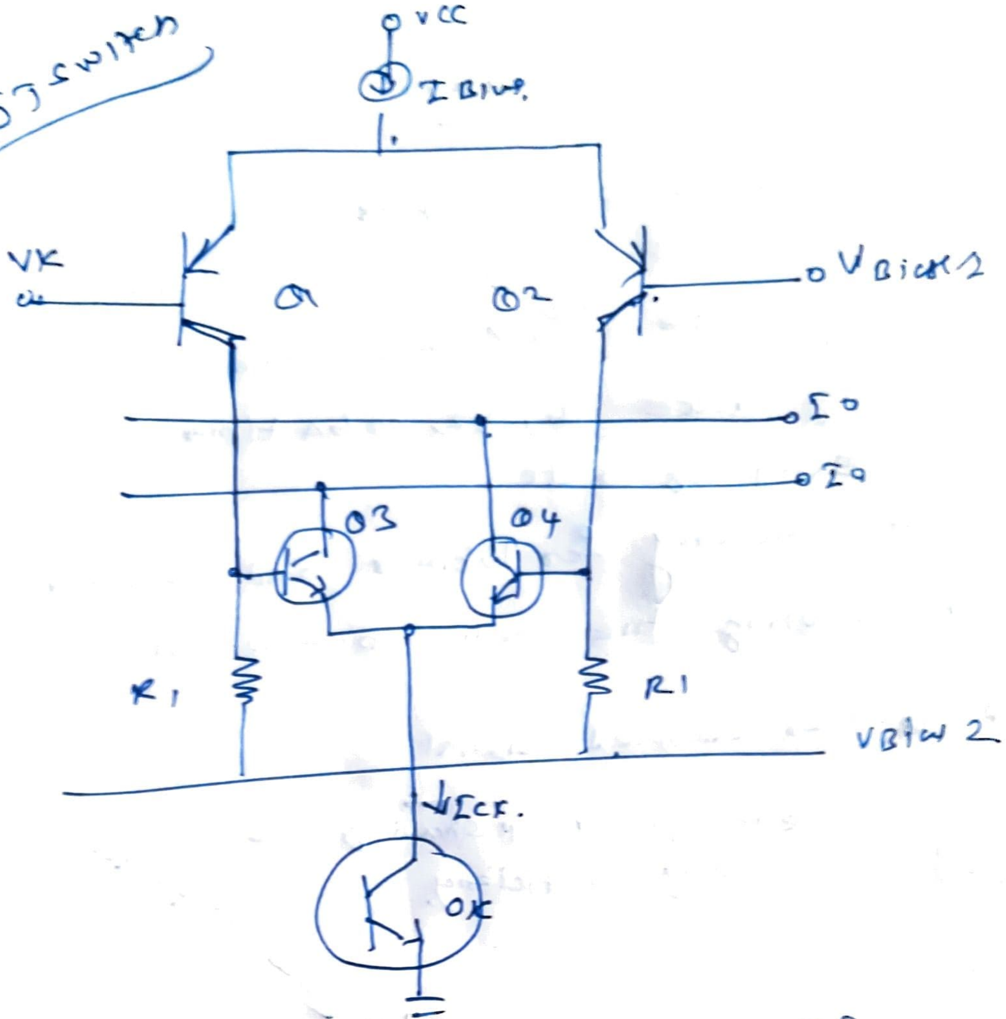
Vin = Low, M8 - ON, M9 = OFF, 2R connected to $\overline{IO}$

BJT switch

BJTs are used to provide fast current switching and true o/p current source or sink capability in DACs

When $V_K > V_{Bias}$ 1, Q1 off, Q2 - ON and at Q3 - OFF, Q4 - ON. thus steering Q_K's collector current I_{CK} to the IO bus.

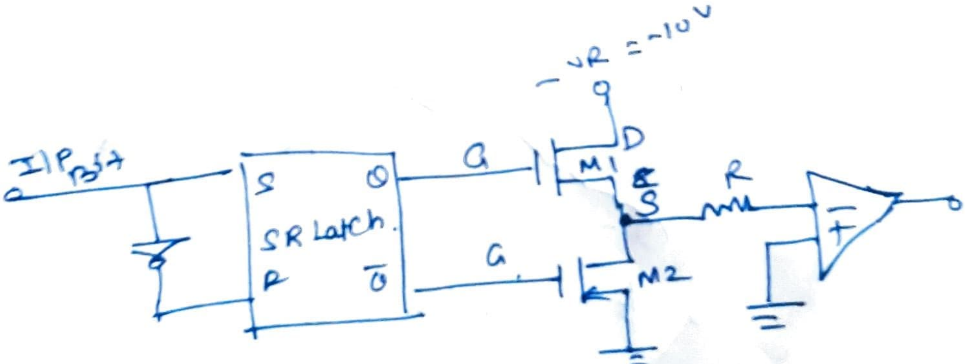
BJT switch



When $V_K < V_{BIAS}$, Q1 ON, Q2 = OFF
Q3 = ON, Q4 = OFF

Ick driven to $\bar{I_0}$ Q vs. The switching threshold is set by Vbias 1, which is typically near 1.4 V to ensure compatibility with both cmos and TTL

Totem pole switch



M1 M2 - N channel enhancement MOSFET

① S=1, R=0, Q=1 $\bar{Q}$=0
Q=1, M1 → ON - allowing -10V to appear at nodes.

② S=0, R=1, Q=0, and $\bar{Q}$=1
$\bar{Q}$=1, — M2 → ON allowing nodes to connect ground.

EC8453 Linear Integrated Circuits

UNIT V WAVEFORM GENERATORS AND SPECIAL FUNCTION ICS

Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave Generator,ICL8038 function generator, Timer IC 555, IC Voltage regulators – Three terminal fixed and adjustable voltage regulators – IC 723 general purpose regulator – Monolithic switching regulator, Low Drop – Out(LDO) Regulators – Switched capacitor filter IC MF10, Frequency to Voltage and Voltage to Frequency converters, Audio Power amplifier, Video Amplifier, Isolation Amplifier, Optocouplers and fibre optic IC.

Explain the square wave generator, triangular wave generator and Saw tooth wave generator with neat diagram (A/M 2020, N/D 2018,A/M 2019,A/M 2016.2014)

Square Wave Generator or Astable Multivibrator

A **square wave generator** is an electronic circuit which generates square wave. The **circuit diagram** of a op-amp based square wave generator is shown in the following figure

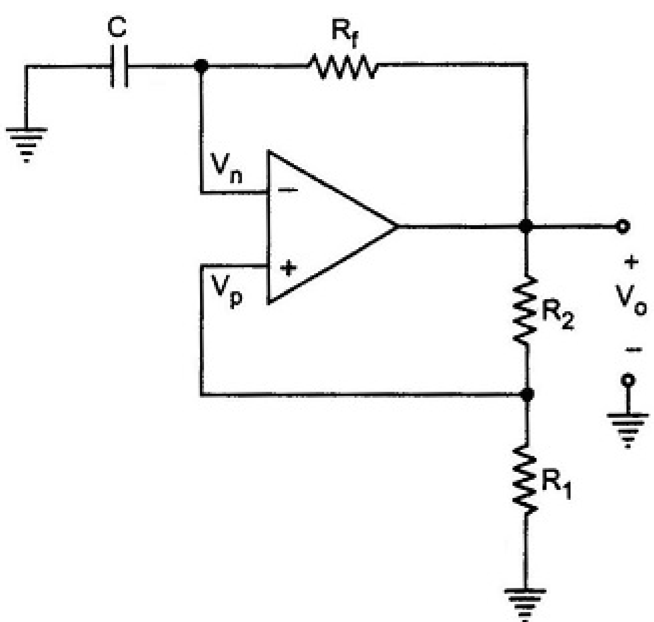


Fig. 2.83 Square wave generator

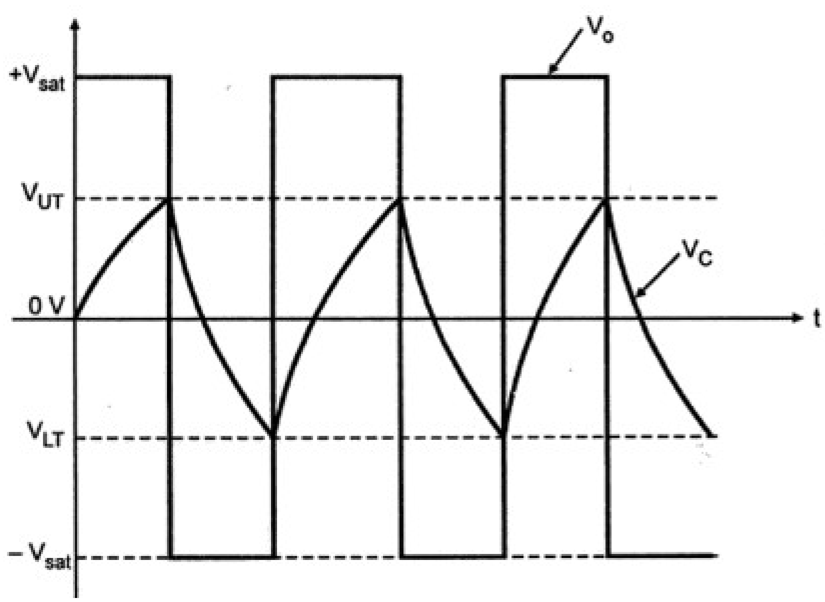
Observe that in the circuit diagram shown above, the resistor $R1$ is connected between the inverting input terminal of the op-amp and its output of op-amp. So, the resistor $R1$ is used in the **negative feedback**. Similarly, the resistor $R2$ is connected between the non inverting input terminal of the op-amp and its output. So, the resistor $R2$ is used in the **positive feedback** path.

A capacitor C is connected between the inverting input terminal of the op-amp and ground. So, the **voltage across capacitor C** will be the input voltage at this inverting terminal of op-amp. Similarly, a resistor $R3$ is connected between the non-inverting input terminal of the op-amp and ground. So, the **voltage across resistor $R3$** will be the input voltage at this non-inverting terminal of the op-amp.

The **operation** of a square wave generator is explained below –

Assume, there is **no charge** stored in the capacitor initially. Then, the voltage present at the inverting terminal of the op-amp is zero volts. But, there is some offset voltage at non-inverting terminal of op-amp. Due to this, the value present at the output of above circuit will be $+V_{sat}$

- Now, the capacitor C starts **charging** through a resistor $R1$. The value present at the output will change to $-V_{sat}$, when the voltage across the capacitor C reaches just greater than the voltage (positive value) across resistor $R3$
- The capacitor C starts **discharging** through a resistor $R1$, when the output of above circuit is $-V_{sat}$. The value present at the output of above circuit will change to $+V_{sat}$, when the voltage across capacitor C reaches just less than (more negative) the voltage (negative value) across resistor $R3$



Square wave generator: Output and Capacitor voltage waveform

Comparator and positive feedback resistors R_1 and R_2 form an inverting schmitt trigger.

When V_o is at $+V_{sat}$, the feedback voltage is called the upper threshold voltage V_{UT} and is given as

$$V_{UT} = \frac{R_1 \quad +V_{sat}}{R_1 + R_2} \qquad \dots (1)$$

When V_o is at $-V_{sat}$, the feedback voltage is called the lower-threshold voltage V_{LT} and is given as

$$V_{LT} = \frac{R_1 \quad -V_{sat}}{R_1 + R_2} \qquad \dots (2)$$

Frequency of Oscillation:

The frequency of oscillation of Square Wave Generator Using Op amp is determined by the time it takes the capacitor to charge from V_{UT} to V_{LT} and vice versa. The voltage across the capacitor as a function of time is given as

$$V_C(t) = V_{max} + (V_{initial} - V_{max})e^{(-t/T)} \qquad \dots (3)$$

where

- $V_C(t)$ is the instantaneous voltage across the capacitor.
- $V_{initial}$ is the initial voltage
- V_{max} is the voltage toward which the capacitor is charging.

Let us consider the charging of capacitor from V_{LT} to V_{UT}, where V_{LT} is the initial voltage, V_{UT} is the instantaneous voltage and $+V_{sat}$ is the maximum voltage. At $t = T_1$, voltage across capacitor reaches V_{UT} and therefore equation (3) becomes

$$V_{UT} = +V_{sat} + (V_{LT} - +V_{sat})e^{(-T_1/R_f C)} \qquad \dots (4)$$

$$\therefore - (V_{LT} - +V_{sat})e^{(-T_1/R_f C)} = +V_{sat} - V_{UT}$$

$$\therefore \quad e^{(-T_1/R_f C)} = \frac{(+V_{sat} - V_{UT})}{(+V_{sat} - V_{LT})}$$

$$\therefore \quad \frac{-T_1}{R_f C} = ln\left(\frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}\right)$$

$$\therefore \quad T_1 = -R_f C\, ln\left(\frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}\right)$$

$$= R_f C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right) \qquad \dots (5)$$

The time taken by capacitor to charge from V_{UT} to V_{LT} is same as time required for charging capacitor from V_{LT} to V_{UT}. Therefore, total time required for one oscillation is given as

$$T = 2T_1 \qquad \ldots (6)$$

$$= 2R_f\, C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right) \qquad \ldots (7)$$

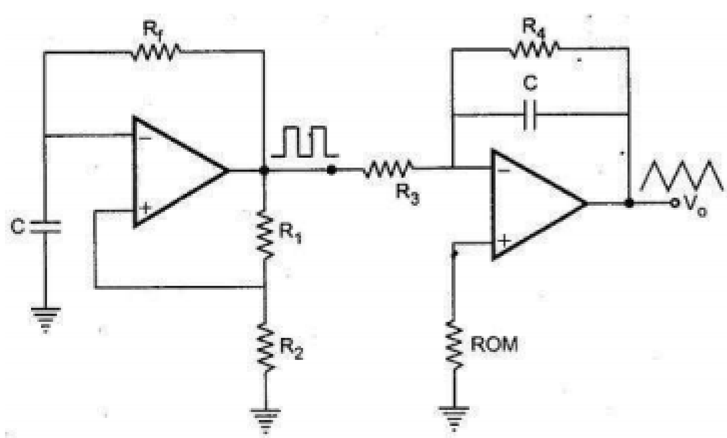
The frequency of oscillation can be determined as $f_o = 1/T$, where T represents the time required for one oscillation.

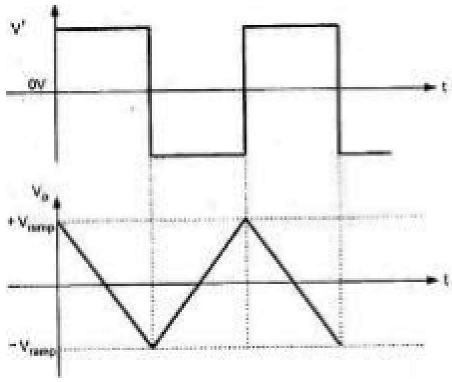
Substituting the value of T we get,

$$f_o = \frac{1}{2\,R_f\, C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)} \qquad \ldots (8)$$

Triangular Wave Generator

Triangular wave is generated by alternatively charging and discharging a capacitor with a constant current. This is achieved by connecting integrator circuit at the output of square wave generator





Input-output waveforms

Assume that V' is high at +Vsat. This forces a constant current (+Vsat/R3) through C (left to right) to drive Vo negative linearly. When V' is low at —Vsat, it forces a constant current (— Vsat /R3) through C (right to left) to drive Vo positive, linearly. The frequency of the triangular wave is same as that of square wave

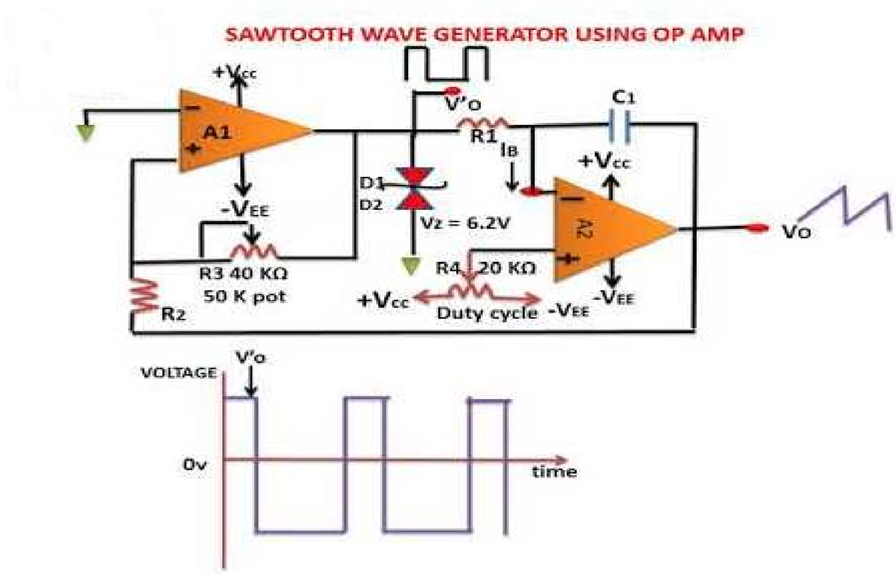
Although the amplitude of the square wave is constant (± Vsat), the amplitude of the triangular wave decreases with an increase in its frequency, and vice versa. This is because the reactance of capacitor decreases at high frequencies and increases at low frequencies. In practical circuits, resistance R4 is connected across C to avoid the saturation problem at low frequencies as in the case of practical integrator

To obtain stable triangular wave at the output, it is necessary to have 5R3 C2 > T/2, where T is the period of the square wave input.

The time period of the output of the square wave generator is T = 2 x 2.303 Rf C x log((2R2+R1)/R1) which is the same for triangular wave generator. Frequency of the output f = 1/T

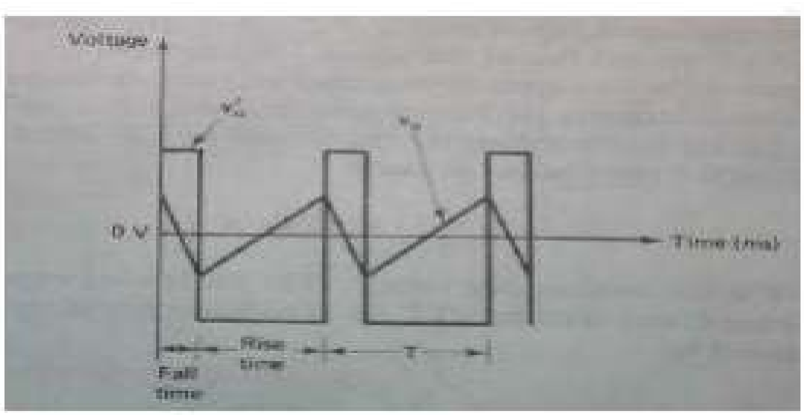
Saw tooth Wave form Generator

Sawtooth wave generator is given in above figure. Schematic of Sawtooth wave generator Sawtooth waveform can be also generated by an asymmetrical astable multivibrator followed by an integrator as shown in figure .The sawtooth wave generators have wide application in time-base generators and pulse width modulation circuits. The difference between the triangular wave and sawtooth waveform is that the rise time of triangular wave is always equal to its fall of time while in saw tooth generator, rise time may be much higher than its fall of time , vice versa



The triangular wave generator can be converted in to a sawtooth wave generator by injecting a variable dc voltage into the non-inverting terminal of the integrator. In this circuit a potentiometer is used. Now the output of integrator is a triangular wave riding on some dc level that is a function of R4 setting.

The duty cycle of square wave will be determined by the polarity and amplitude of dc level. A duty cycle less than 50% will cause output of integrator be a sawtooth. With the wiper at the centre of R4 , the output of integrator is square wave. Use of the potentiometer is when the wiper moves towards −VEE,the rise time of the sawtooth become longer than the fall time (see fig. If the wiper moves towards +VCC , the fall time becomes more than the rise time.



Output waveform of sawtooth wave generator

Features of LM380:

1. Internally fixed gain of 50 (34dB)
2. Output is automatically self centering to one half of the supply voltage.
3. Output is short circuit proof with internal thermal limiting.
4. Input stage allows the input to be ground referenced or ac
5. Wide supply voltage range (5 to 22V).
6. High peak current capability.
7. High impedance.

Explain the working principle of 1. Audio power amplifier 2. Videoamplifier 3. Isolation Amplifier

Applications:

Explain switched capacitor filter , audio power amplifier, opto coupler? (April May 2017)

Briefy write the working principle and functionalities of LM 380 audio amplifier. (8)

[APR/MAY 2016][NOV/DEC 2017][APR/MAY 2019

(i) Audio Power Amplifier:

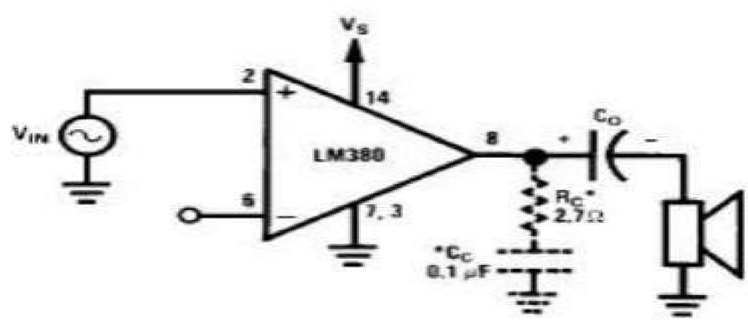


Figure shown above is the connection of Audio power Amplifier. Amplifier requires very few external components because of the internal biasing, compensation & fixed gain.

• When the power amplifier is used in the non inverting configuration, the inverting terminal may be either shorted to ground, connected to ground through resistors & capacitors.

• Similarly when the power amplifier is used in the inverting mode, the non inverting terminal may be either shorted to ground or returned to ground through resistor or capacitor.

• Usually a capacitor is connected between the inverting terminal & ground if the input has a high internal impedance.

• As a precautionary measure, an RC combination should be used at the output terminal (pin 8) to eliminate 5-to-10 MHz oscillation.

• C1 is coupling capacitor which couples the output of the amplifier to the 8 ohms loud speaker which acts as a load. The amplifier will amplify the Vin applied at the non- inverting terminal

Video Amplifier

8.25.1 IC MC 1550 as a Video Amplifier

The Fig. 8.25.1 shows MC 1550 used as a video amplifier. As it uses a cascode amplifier pair, the video amplifier is called cascode video amplifier. The transistor Q_1 is a common emitter amplifier and transistor Q_3 is a common base amplifier and they together from a cascode amplifier.

To properly terminate the co-axial cable carrying the video signal, a 50 Ω resistance is connected between the pins 1 and 4 of MC 1550. Such a small resistance has very negligible effect on the biasing of the transistor Q_1. The load resistance R_L is directly inserted in the collector of the transistor Q_3.

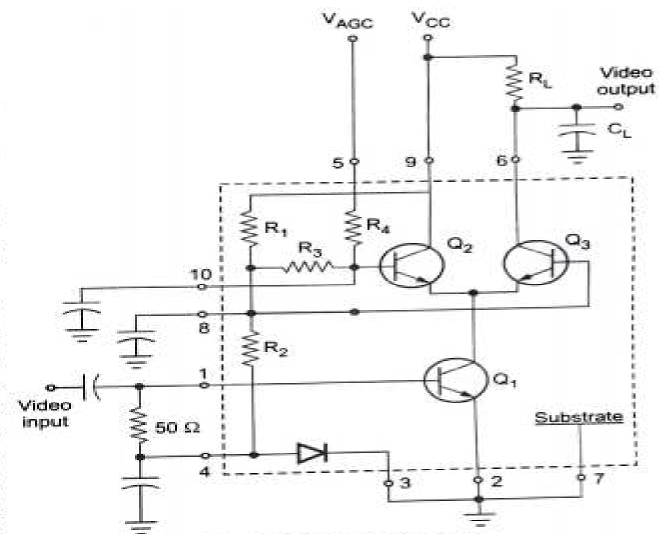


Fig. 8.25.1 Video amplifier

The Fig. 8.25.1 (a) shows the small signal approximate equivalent circuit for video amplifier. Both Q_2 and Q_3 are operating in their active region, therefore the collector of Q_1 sees the very small input resistance (r_{e2} || r_{e3}) of two common-base stages in parallel. By representing Q_1 in its hybrid-π model, and due to very low load on Q_1, we can neglect the effect of C_C. Q_3 can be represented as a current source, α_3 I_3, where I_3 is the emitter signal current of Q_3 and $\alpha_3 = 1$ and is independent of frequency over the band of frequencies under consideration. C_S represents the capacitance from the collector of Q_1 and Q_3 to the substrate.

Isolation Amplifier (Nov/ Dec 2016) [NOV/DEC2013][MAY/JUN 2012]

8.26 Isolation Amplifier

AU : May-05, 12

An isolation amplifier is an amplifier that offers an ohmic or electrical isolation between its input and output terminals. Isolation amplifiers are often used when there is a very large common-mode voltage difference between the input and output sides of the device. They can provide voltage difference of several thousands of volts between input and output. The isolation in the isolation amplifier is achieved by use of transformer or by use of optically coupled devices discussed earlier.

The Fig. 8.26.1 shows some of the symbols used for isolation amplifiers.

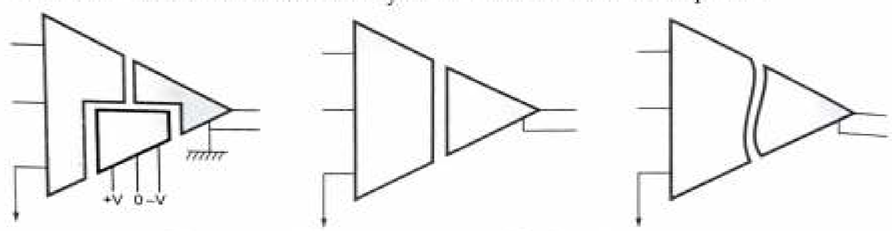


Fig. 8.26.1 Different symbols used for isolation amplifiers

An important characteristics of an isolation amplifier is the linearity of the input to output transfer characteristics. But the non linear input current to light output characteristics is a problem in this regard. There are various methods of obtaining a high degree of linearity in optically coupled isolation amplifiers. Such two examples of isolation amplifiers are discussed in the following section. Fig. 8.26.2 shows an isolation amplifier in which a LED-photo transistor couplers are used as an optoisolators. As shown in Fig. 8.26.2, first LED-phototransistor coupler is used in the feedback loop of amplifier A_1 and the second LED-phototransistor coupler is used at the input of amplifier A_2. Both LED-phototransistor couplers are used with matched characteristics, are driven by the same amplifier, amplifier A_1. Due to the matched characteristics of the two LED-photo transistor pairs, the non-linear characteristics and temperature dependence get compensated.

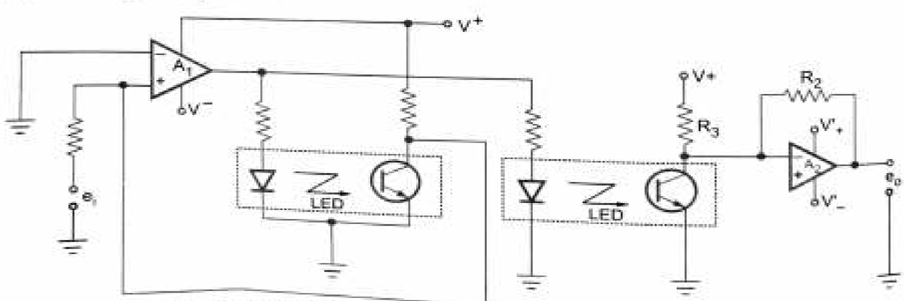


Fig. 8.26.2 LED-Phototransistor linearized isolation amplifier

IC 723 – GENERAL PURPOSE REGULATOR

Disadvantages of fixed voltage regulator:

1. Do not have the shot circuit

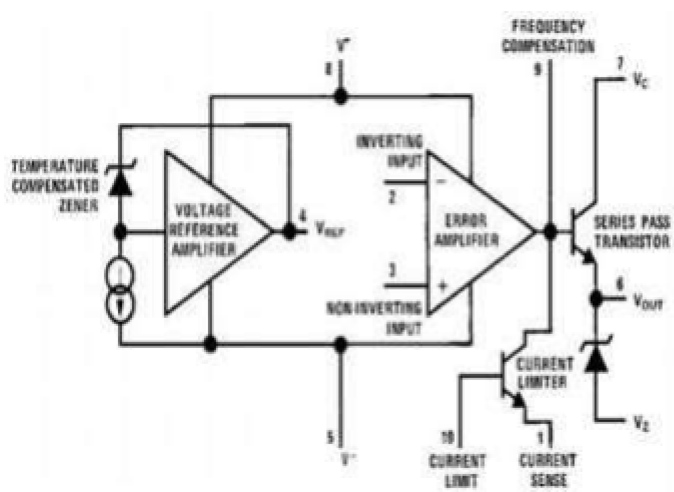
2. Output voltage is not adjustable

These limitations can be overcomes in IC723.

Features of IC723:

1. Unregulated dc supply voltage at the input between 9.5V & 40V
2. Adjustable regulated output voltage between 2 to 3V.
3. Maximum load current of 150 mA (ILmax = 150mA).
4. With the additional transistor used, ILmax upto 10A is obtainable.
5. Positive or Negative supply operation
6. Internal Power dissipation of 800mW.
7. Built in short circuit protection.
8. Very low temperature drift.
9. High ripple rejection

Explain the functional block diagram of voltage regulator and basic low voltage and high voltage regulator.



Functional block diagram of IC723

Functional block diagram of IC723 is shown in figure 5.6.1.The simplified functional block diagram can be divided in to 4 blocks.

1. Reference Generating block:

The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block. The Zener diode is used to generate a fixed reference voltage internally. Constant current source will make the Zener diode to operate at affixed point &

it is applied to the Non – inverting terminal of error amplifier. The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.

2. Error Amplifier:

Error amplifier is a high gain differential amplifier with 2 input (inverting & Non- inverting). The Non-inverting terminal is connected to the internally generated reference voltage. The Inverting terminal is connected to the full regulated output voltage.

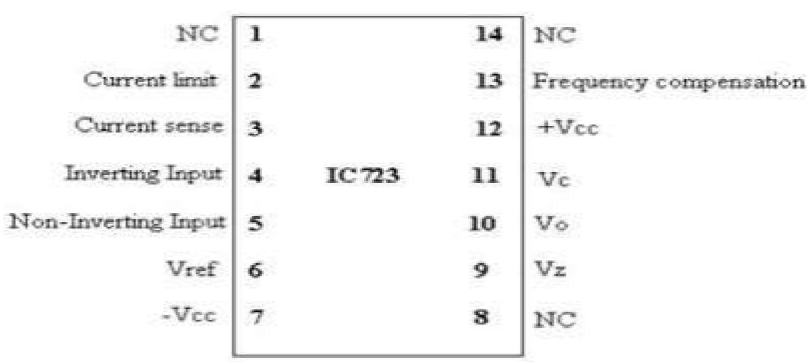
3. Series Pass Transistor:

Q1 is the internal series pass transistor which is driven by the error amplifier. This transistor actually acts as a variable resistor & regulates the output voltage. The collector of transistor Q1 is connected to the Un-regulated power supply. The maximum collector voltage of Q1 is limited to 36Volts. The maximum current which can be supplied by Q1 is 150mA.

4. Circuitry to limit the current:

The internal transistor Q2 is used for current sensing & limiting. Q2 is normally OFF transistor. It turns ON when the IL exceeds a predetermined limit. Low voltage, Low current is capable of supplying load voltage which is equal to or between 2 to 7Volts.Pin diagram of IC723 in figure

Vload = 2 to 7V and Iload= 50mA



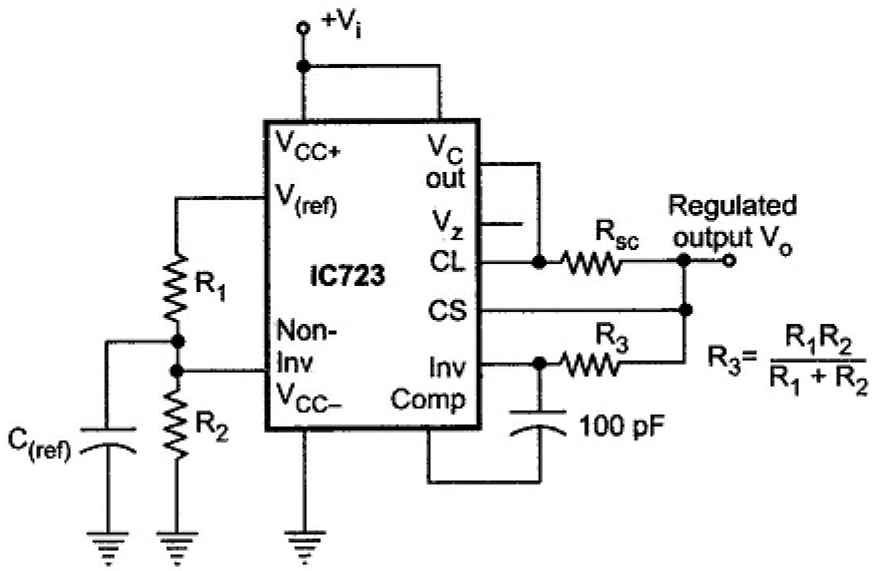
Pin diagram of IC723

Describe the working of IC723 voltage regulator and explain how it can be used as Low voltage regulator.[APR/MAY2021]

Describe the working of IC723 voltage regulator and explain how it can be used as High voltage regulator.[APR/MAY2021]

Summarize the working principle of IC723 general purpose voltage regulator. (12) [APR/MAY 2016]

IC 723 LOW voltage Regulator



Basic low-voltage regulator

Basic Low Voltage Regulator

The resistor, R_{sc} is connected between CL and CS pins. The current limit transistor remains non-conductive unless drops across R_{sc} is 0.6 V (equal to V_{BE} drop). The value of R_{sc} can be found out by following equation

$$R_{sc} = \frac{V_{sense}}{I_{limit}} = \frac{0.6}{I_{limit}} \qquad \ldots (1)$$

I_{limit} can be selected as 1.2 to 1.5 times the maximum load circuit. Potential divider made up of R_1 and R_2 is connected between V_{ref} and non-inverting terminals.

$$V_{non\text{-}inverting} = V_{ref} \times \frac{R_2}{R_1 + R_2} \qquad \ldots (2)$$

As the series pass transistor is working as emitter follower.

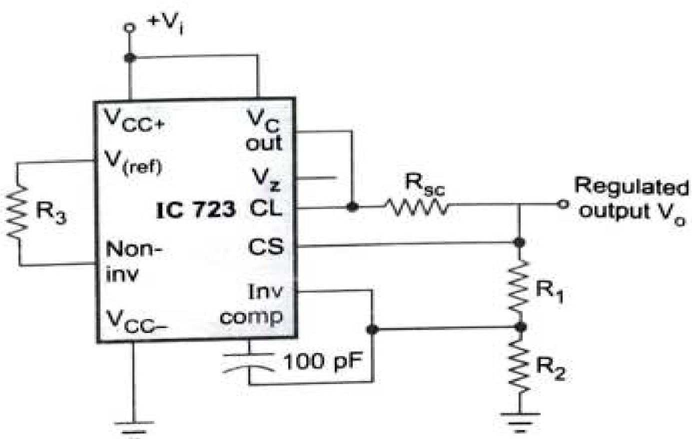
$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2} \quad \dots (3)$$

R_1 and R_2 can be between 1 kΩ to 10 kΩ.

$$R_3 = R_1 \parallel R_2 \quad \therefore R_3 = \frac{R_1 R_2}{R_1 + R_2} \quad \dots (4)$$

Maximum load current can be 150 mA.

Basic High voltage regulator



Basic high-voltage regulator (V_o = 7 to 37 volts)

Basic Positive High Voltage Regulator

For this type, output voltage varies from +7 V to +37 V and $I_L \leq 150$ mA.

The non-inverting terminal connected to V_{ref} through R_3. Due to this arrangement the error amplifier acts as non-inverting amplifier.

The gain $\boxed{A = 1 + \frac{R_1}{R_2}}$

The output voltage is,

$$\boxed{V_o = V_{ref}\left(1 + \frac{R_1}{R_2}\right) = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right)} \quad \text{... (8.12.7)}$$

$$\boxed{R_{sc} = \frac{0.6}{I_{limit}} = \frac{V_{sense}}{I_{sc}}} \quad \text{... (8.12.8)}$$

$$\boxed{R_3 = R_1 \parallel R_2 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)} \quad \text{... (8.12.9)}$$

This is also called basic **high voltage low current regulator.**

Low voltage High current Regulator

8.12.4.2 Low Voltage High Current Regulator

Output voltage from +2 to +7 V and load current can be more than 150 mA. For this one transistor is connected externally, shown as Q_1 in the Fig. 8.12.5.

The functional equations are similar to that of basic low voltage regulator circuit.

$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

$$R_{sc} = \frac{0.6}{I_{limit}}$$

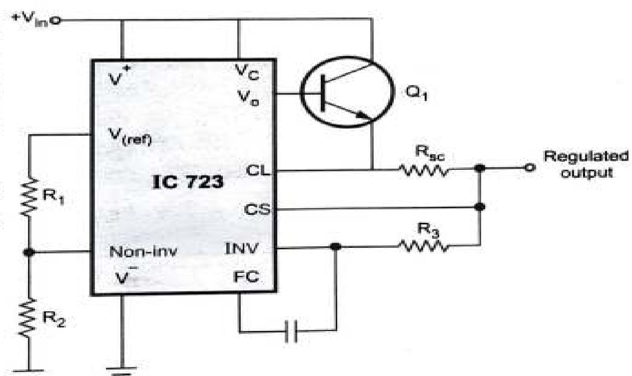


Fig. 8.12.5

$$\text{Power dissipation of transistor} = [V_{i(max)} - V_{o(min)}] \times I_{L(max)} \quad \text{... (8.12.5)}$$

$$\text{Power dissipation of IC} = [V_{i(max)} - V_{o(min)}] \times \frac{I_{L(max)}}{h_{fe\,(min)\text{ of }Q_1}} \quad \text{... (8.12.6)}$$

8.12.4.4 Positive High Voltage High Current Regulator

For this type, output voltage from +7 V to +37 V and load current I_L > 150 mA. For this a external transistor Q_1 is connected, as shown in the Fig. 8.12.7.

For this different expressions are similar to basic high voltage regulator and reproduced for the convenience.

$$V_o = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right)$$

$$R_{sc} = \frac{0.6}{I_{limit}} = \frac{V_{sense}}{I_{sc}}, \quad R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

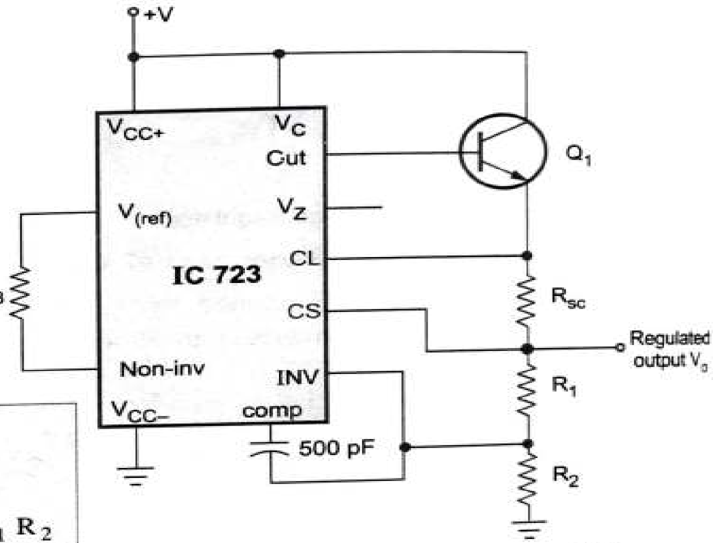


Fig. 8.12.7 Positive high voltage regulator

While the power dissipation of transistor Q_1 and the IC is given by the same expressions as given by the equations (8.12.5) and (8.12.6).

EXPLAIN THE OPTO COUPLERS/OPTO ISOLATORS AND FIBRE OPTIC IC

Opto couplers or Opto isolators is a combination of light source & light detector in the same package. They are used to couple signal from one point to other optically, by providing a complete electric isolation between them. This kind of isolation is provided between a low power control circuit & high power output circuit, to protect the control circuit.

Characteristics of opto coupler:

(i) Current Transfer Ratio:

It is defined as the ratio of output collector current (Ic) to the input forward current (If)

CTR = Ic/If * 100%. Its value depends on the devices used as source & detector.

(ii) Isolation voltage between input & output:

It is the maximum voltage which can exist differentially between the input & output without affecting the electrical isolation voltage is specified in K Vrms with a relative humidity of 40 to 60%.

(iii) Response Time:

Response time indicates how fast an opto coupler can change its output state. Response time largely depends on the detector transistor, input current & load resistance.

(iv) Common mode Rejection:

Even though the opto couplers are electrically isolated for dc & low frequency signals, an impulsive input signal (the signal which changes suddenly) can give rise to a displacement current Ic= Cf*dv/dt. This current can flow between input & output due to the capacitance Cf existing between input & output. This allows the noise to appear in the output.

Depending on

the type of light source & detector used we can get a variety of opto couplers.

They are as follows,

Explain the OPTO COUPLERS/OPTO ISOLATORS AND FIBRE OPTIC(A/M 2017) ,N/D 2016

1.LED PHOTODIODE OPTOCOUPLER

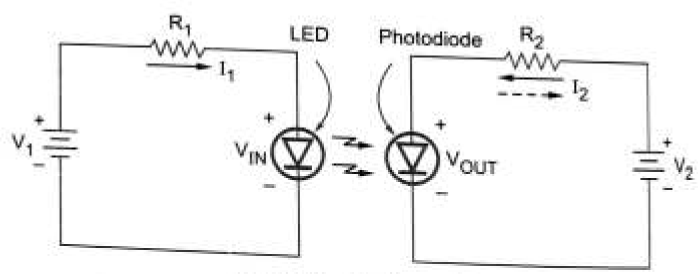
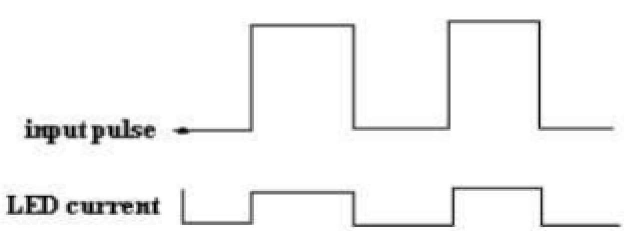


Fig. 8.27.1 Optocoupler

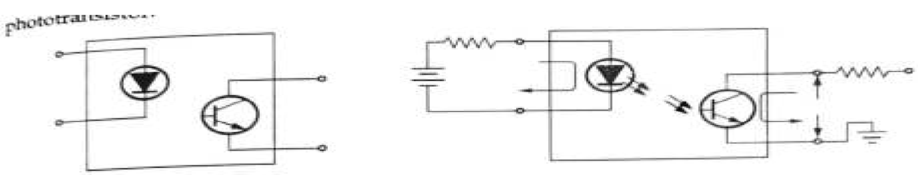


LED photodiode and its waveforms are shown in above figure , here the infrared LED acts as a light source & photodiode is used as a detector.

The advantage of using the photodiode is its high linearity. When the pulse at the input goes high, the LED turns ON. It emits light. This light is focused on the photodiode. In response to this light the photocurrent will start flowing though the photodiode. As soon as the input pulse reduces to zero, the LED turns OFF & the photocurrent through the photodiode reduces to zero. Thus the pulse at the input is coupled to the output side.

$$V_{out} = V_2 - I_2 R_2$$

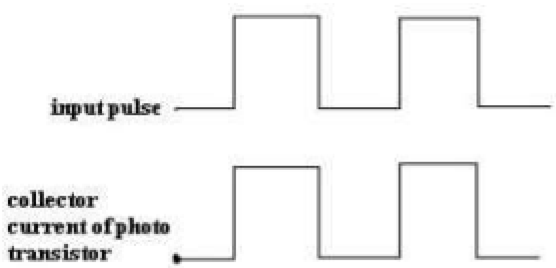
LED – PHOTOTRANSISTOR OPTO COUPLER



(a) Optoisolator (b) Optoisolator circuit

Fig. 8.27.1

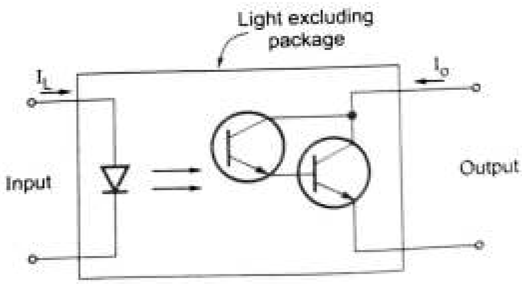
When the input voltage forward biases the LED, light transmitted to the phototransistor turns it on, resulting current through the external load, as shown in Fig. 8.27.1 (b).



The LED phototransistor opto coupler and its waveforms shown in figure . An infrared LED acts as a light source and the phototransistor acts as a photo detector.

- This is the most popularly used opto coupler, because it does not need any additional amplification.
- When the pulse at the input goes high, the LED turns ON. The light emitted by the LED is focused on the CB junction of the phototransistor.
- In response to this light photocurrent starts flowing which acts as a base current for the phototransistor.
- The collector current of phototransistor starts flowing. As soon as the input pulse reduces to zero, the LED turns OFF & the collector current of phototransistor reduces to zero. Thus the pulse at the input is optically coupled to the output side.
- The input & output waveforms are 180º out of phase as the output is taken at the collector of the phototransistor

LED –DARLINGTON OPTOCOUPLER



(b) LED-photodarlington

Advantages of Opto coupler:

- Control circuits are well protected due to electrical isolation.
- Wideband signal transmission is possible.
- Due to unidirectional signal transfer, noise from the output side does not get coupled to the input side.
- Interfacing with logic circuits is easily possible.
- It is small size & light weight device.

Disadvantages:

- Slow speed.
- Possibility of signal coupling for high power signals.

Applications:

Opto couplers are used basically to isolate low power circuits from high power circuits.
At the same time the control signals are coupled from the control circuits to the high power circuits.

- Some of such applications are,

i. AC to DC converters used for DC motor speed control
ii. High power choppers
iii. High power inverters

- One of the most important applications of an opto coupler is to couple the base driving signals to a power transistor connected in a DC-DC chopper

8.25.2 Design Considerations for Video Amplifier

From the equations for 3 dB frequencies and for voltage gain in the previous example we can conclude the following design considerations for video amplifier

1. To increase the bandwidth the gain must be reduced by decreasing R_L.
2. The load capacitance should be as small as possible.
3. If discrete circuit is used choose the transistor having high value of f_T and low value of base spreading resistor $r_{bb'}$.
4. Use CE-CB cascode pair as an amplifier because its high frequency is better than the CE amplifier.
5. Use one or more negative feedback loops to increase the bandwidth of the amplifier.

The TIMER IC 555

Applications

Astable multivibrator

Monnostable multivibrator

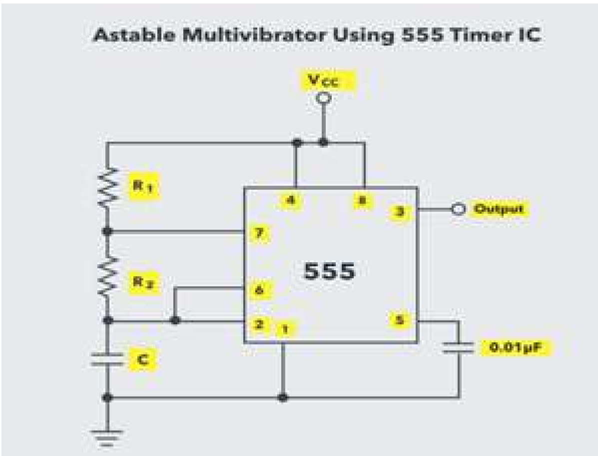
Explain the IC 555 can be used as a Astable Multivibrator. Drive an expression for frequency of oscillations. (If this question asked in Big question should draw internal diagram and explain the operation)

What are the modes of operation of a timer? Draw the functional diagram of a square wave generator using timer and derive its duty cyle. .[APR/MAY2021](understand)

With neat diagram, explain the operation of an astable and monostable multivibrator[NOV/DEC 2017] [NOV/DEC 2018]

Atable multivibrator

It is also called as Free Running Multivibrator. It has no stable states and continuously switches between the two states without application of any external trigger.



Schematic Diagram

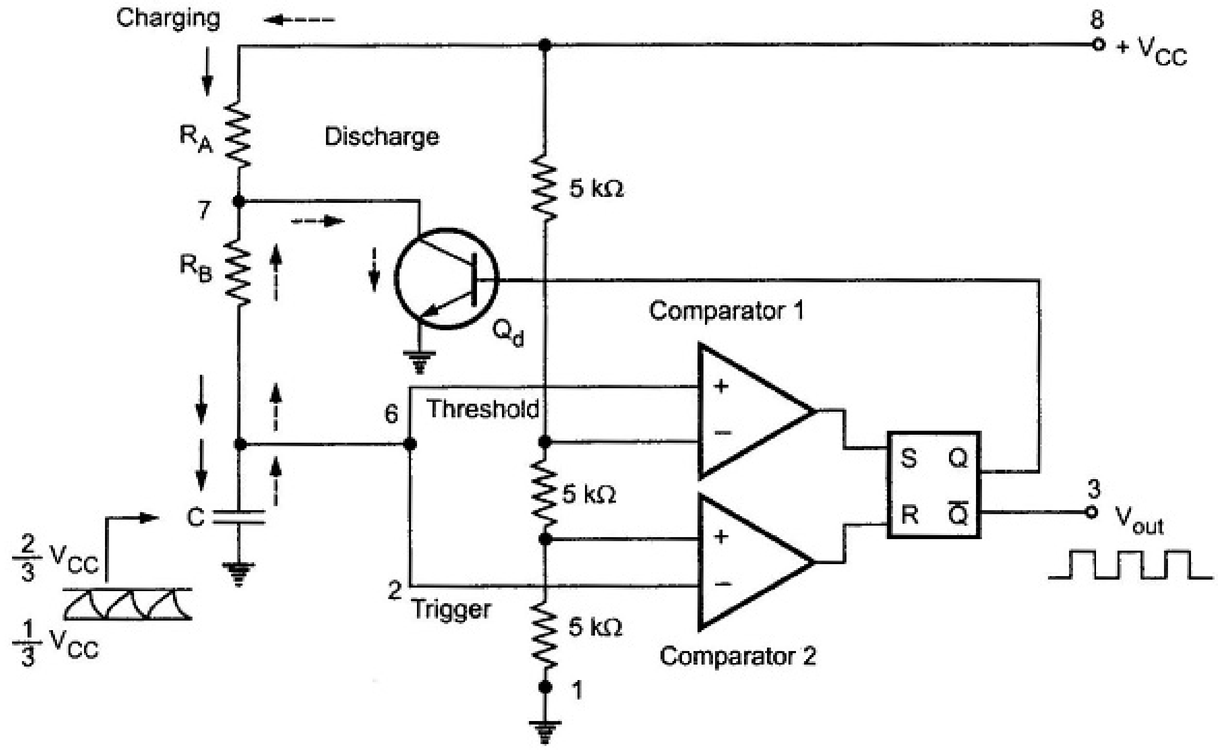
The pins 2 and 6 are connected and hence there is no need for an external trigger pulse. It will self trigger and act as a free running multivibrator (oscillator). The rest of the connections are as follows: pin 8 is connected to supply voltage (V_{CC}). Pin 3 is the output terminal and hence the output is available at this pin. Pin 4 is the external reset pin. A momentary low on this pin will reset the timer. Hence, when not in use, pin 4 is usually tied to V_{CC}.

The control voltage applied at pin 5 will change the threshold voltage level. But for normal use, pin 5 is connected to ground via a capacitor (usually 0.01µF), so the external noise from the terminal is filtered out. Pin 1 is ground terminal. The timing circuit that determines the width of the output pulse is made up of R_1, R_2 and C.

Operation

The following schematic depicts the internal circuit of the IC 555 operating in astable mode. The RC timing circuit incorporates R_1, R_2 and C.

The following schematic depicts the internal circuit of the IC 555 operating in astable mode. The RC timing circuit incorporates R_1, R_2 and C.

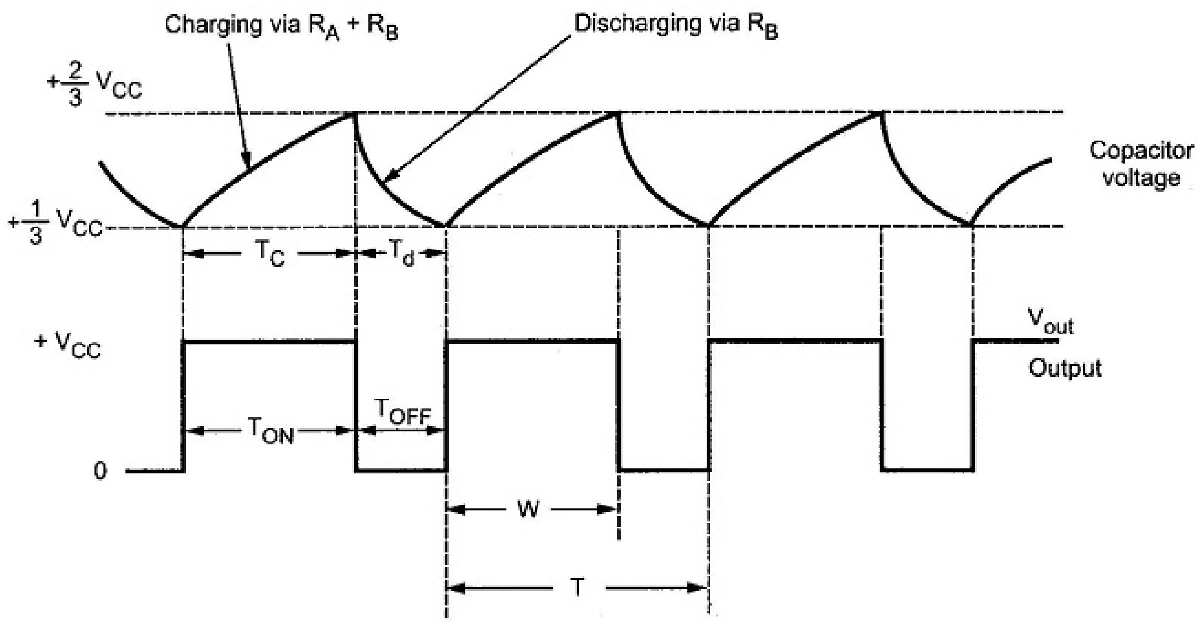


When the flip-flop is set, Q is high which drives the transistor Q_d in saturation and the capacitor gets discharged. Now the capacitor voltage is nothing but the trigger voltage. So while discharging, when it becomes less than 1/3 V_{CC}, comparator 2 output goes high. This resets the flip-flop hence Q goes low and $\overline{Q}$ goes high.

The low Q makes the transistor off. Thus capacitor starts charging through the resistances R_A, R_B and V_{CC}. The charging path is shown by thick arrows in the Fig. 2.105. As total resistance in the charging path is $(R_A + R_B)$, the charging time constant is $(R_A + R_B)$ C.

Now the capacitor voltage is also a threshold voltage. While charging, capacitor voltage increases i.e. the threshold voltage increases. When it exceeds 2/3 V_{CC}, then the comparator 1 output goes high which sets the flip-flop. The flip-flop output Q becomes high and output at pin 3 i.e. $\overline{Q}$ becomes low. High Q drives transistor Q_d in saturation and capacitor starts discharging through resistance R_B and transistor Q_d. This path is shown by dotted arrows in the Fig. 2.105. Thus the discharging time constant is R_B C. When capacitor voltage becomes less than 1/3 V_{CC}, comparator 2 output goes high, resetting the flip-flop. This cycle repeats.

Thus when capacitor is charging, output is high while when it is discharging the output is low. The output is a rectangular wave. The capacitor voltage is exponentially rising and falling. The waveforms of Astable Multivibrator using 555 Timer IC are shown in the Fig



Waveforms of astable operation

. Duty Cycle of Astable Multivibrator:

Generally the charging time constant is greater than the discharging time constant. Hence at the output, the waveform is not symmetric. The high output remains for longer period than low output. The ratio of high output period and low output period is given by a mathematical parameter called **duty cycle**. **It is defined as the ratio of ON time i.e. high output to the total time of one cycle.**

$$W = \text{time for output is high} = T_{ON}$$

$$T = \text{time of one cycle}$$

$$\therefore \quad D = \text{duty cycle} = \frac{W}{T}$$

$$\therefore \quad \% D = \frac{W}{T} \times 100 \%$$

The charging time for the capacitor is given by,

$$T_c = \text{Charging time} = 0.693 (R_A + R_B) C$$

While the discharge time is given by,

$$T_d = \text{Discharging time} = 0.693\, R_B\, C$$

Hence the time for one cycle is

$$T = T_c + T_d = 0.693\,(R_A + R_B)\,C + 0.693\, R_B\, C$$
$$= 0.693\,(R_A + 2\,R_B)\,C$$

While

$$W = T_c = 0.693\,(R_A + R_B)\,C$$

$$\therefore \quad \%D = \frac{W}{T}\times 100 = \frac{0.693\,(R_A + R_B)\,C}{0.693\,(R_A + 2\,R_B)\,C}\times 100$$

$$\therefore \quad \%\,D = \frac{(R_A + R_B)}{(R_A + 2\,R_B)}\times 100$$

While the frequency of oscillations is given by,

$$f = \frac{1}{T} = \frac{1}{0.693\,(R_A + 2\,R_B)C}$$

$$\therefore \quad f = \frac{1.44}{(R_A + 2\,R_B)C}\ \text{Hz}$$

If R_A is much smaller than R_B, duty cycle approaches to 50% and output waveform approaches to square wave.

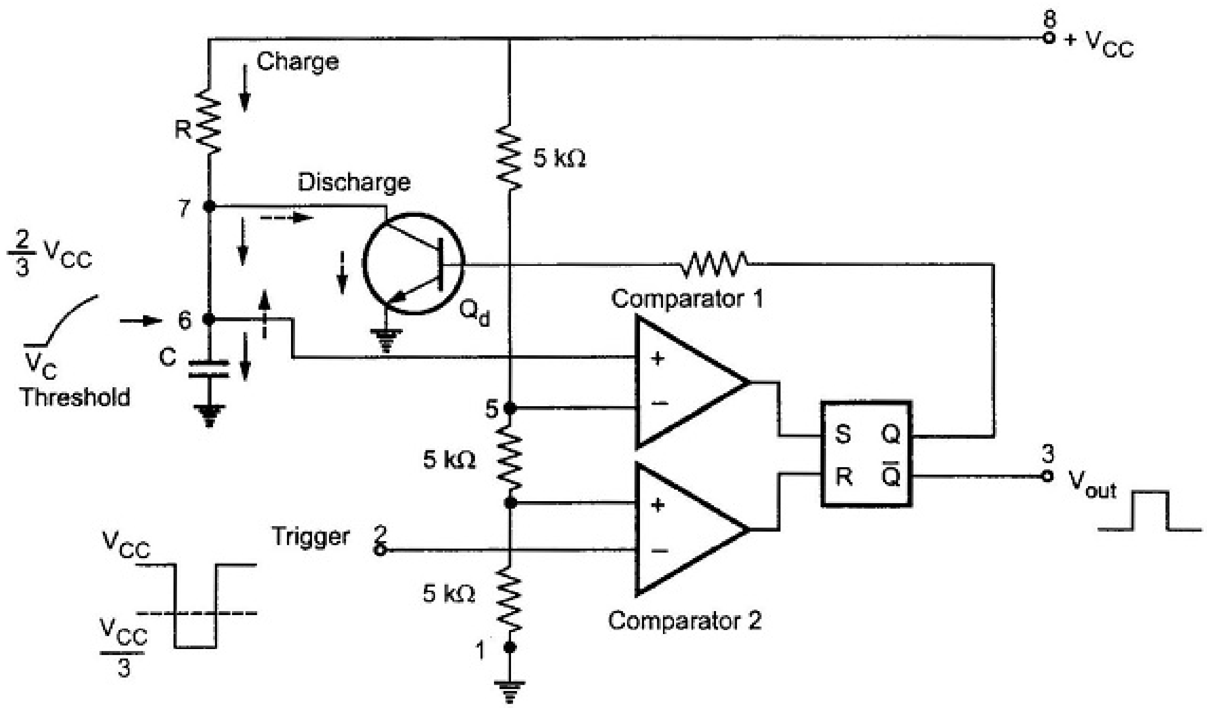
Application of Astable Multivibrator using IC 555:

The various Application of Astable Multivibrator using IC 555 are,

1. Square wave generation
2. FSK generator
3. Voltage controlled oscillator (VCO)

Monostable Multivibrator Using 555 IC

The IC 555 timer can be operated as a Monostable Multivibrator Using IC 555 by connecting an external resistor and a capacitor as shown in the Fig



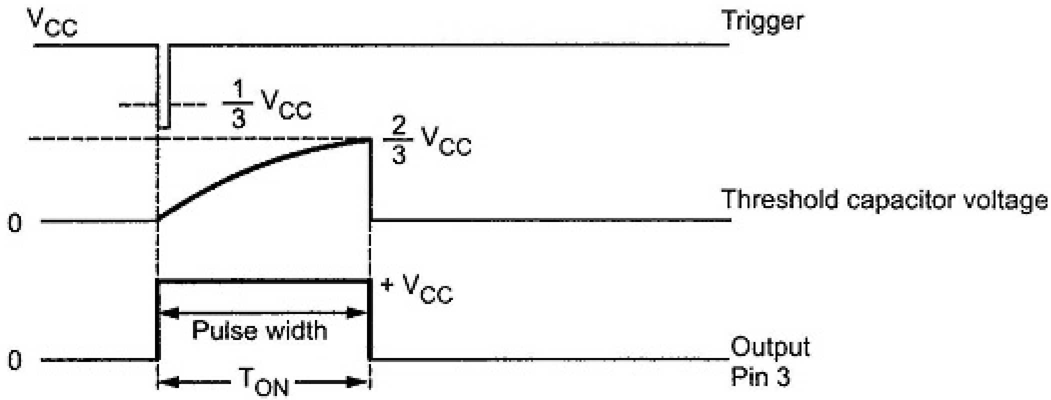
Monostable operation of 555

The circuit has **only one stable state**. When trigger is applied, it produces a pulse at the output and returns back to its stable state. The duration of the pulse depends on the values of R and C. As it has only one stable state, it is called one shot **multivibrator**.

Working of 555 Timer as Monostable Multivibrator:

The flip-flop is initially set i.e. Q is high. This drives the transistor Q_d in saturation. The capacitor discharges completely and voltage across it is nearly zero. The output at pin 3 is low.

When a trigger input, a low going pulse is applied, then circuit state remains unchanged till trigger voltage is greater than 1/3 V_{CC}. When it becomes less than 1/3 V_{CC}, then comparator 2 output goes high. This resets the flip-flop so Q goes low and $\overline{Q}$ goes high. Low Q makes the transistor Q_d off. Hence capacitor starts charging through resistance R, as shown by dark arrows in the Fig.



Waveforms of monostable operation

The voltage across capacitor increases exponentially. This voltage is nothing but the threshold voltage at pin 6. When this voltage becomes more than 2/3 V_{CC}, then comparator 1 output goes high. This sets the flip-flop i.e. Q becomes high and $\bar{Q}$ low. This high Q drives the transistor Q_d in saturation. Thus capacitor C quickly discharges through Q_d as shown by dotted arrows in the wave forms Figure

So it can be noted that V_{out} at pin 3 is low at start, when trigger is less than 1/3 V_{CC} it becomes high and when threshold is greater than 2/3 V_{CC} again becomes low, till next trigger pulse occurs. So a rectangular wave is produced at the output. The pulse width of this rectangular pulse is controlled by the charging time of capacitor. This depends on the time constant RC. Thus RC controls the pulse width. The waveforms are shown in the above Figure.

Derivation of Pulse Width:

The voltage across capacitor increases exponentially and is given by

$$V_C = V\,(1 - e^{-t/CR})$$

If $$V_C = 2/3\ V_{CC}$$

then $$\frac{2}{3} V_{CC} = V_{CC}\,(1 - e^{-t/CR})$$

$$\frac{2}{3} - 1 = -e^{\,t/CR}$$

$$\frac{1}{3} = e^{-t/CR}$$

$$\therefore \quad -\frac{t}{CR} = -1.0986$$

$$\therefore \quad t = +1.0986\ CR$$

$$\therefore \quad t \approx 1.1\ CR$$

where

- C in farads,
- R in ohms,
- t in seconds.

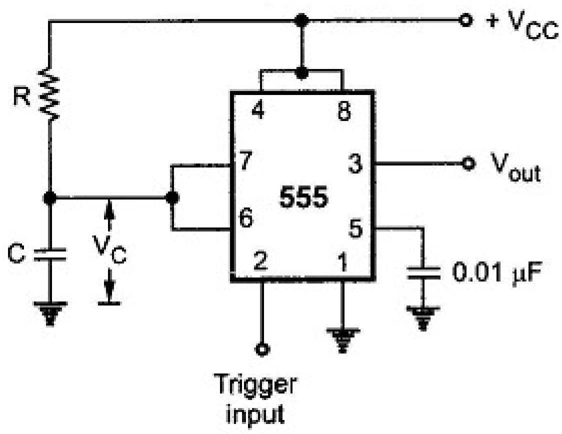
Thus, we can say that voltage across capacitor will reach 2/3 V_{CC} in approximately 1.1 times, time constant i.e. 1.1 RC

Thus the pulse width denoted as W is given by,

$$W = 1.1\ RC.$$

Schematic Diagram:

Generally a schematic diagram of the IC 555 circuits is shown which does not include comparators, flip-flop etc. It only shows the external components to be connected to the 8 pins of IC 555. Thus, the schematic diagram of Monostable Multivibrator Using IC 555 is shown in the Fig



555 timer as monostable multivibrator

The external components R and C are shown. To avoid accidental reset, pin 4 is connected to pin 8 which is supply $+V_{CC}$. To have the noise filtering of control voltage, the pin 5 is grounded through a small capacitor of 0.01 μF.

Monostable Multivibrator Using IC 555 Applications:

The various applications of Monostable Multivibrator Using IC 555 are,

1. Frequency divider
2. Pulse width modulation
3. Linear ramp generator
4. Pulse position modulation
5. Missing pulse detector
6. Timer in relay

Problems

Describe the 555 Timer IC. Design a Astable Multivibrater Circuit to generate output Pulses of 25%, 50% duty cycle using a 555 Timer IC, with choice of C = 0.01,uF, Frequency as 4.0 KHz (April May 2017)

Design a wave generator using 555 timer for a frequency of 110Hz and 80% duty cycle.Assume C=

0.16µF..[Nov/Dec 2018](Create)

A 555 timer is configured in as table mode with R A=2k ohm RB =6k ohm and C=0.1µF.Determine the

frequency of oscillation. (4) [APR/MAY 2016

2 marks

1. Mention some applications of 555 timer (DEC2009))
*Oscillator
*pulse generator
*ramp and square wave generator
*mono-shot multivibrator
*burglaralarm
*traffic light control.
2.List the applications of 555 timer in monostable mode of operation: [NOV/DEC'13]

*Missing pulse detector
*Linear ramp generator
*Frequency divider
*Pulse width modulation.
3. List the applications of 555 timer in Astable mode of operation: (MAY/JUNE2010)[NOV/DEC 2013]

*FSK generator
*Pulse-position modulator

4. What is a voltage regulator? (MAY 2010)

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature, and ac line voltage variations.

5.Give the classification of voltage regulators: (MAY 2010)

Series / Linear regulators
Switching regulators.

6.What is a linear voltage regulator?(Remember)

Series or linear regulator uses a power transistor connected in series between the unregulated dc input and the load and it conducts in the linear region .The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor.

7.What is a switching regulator?(Remember)

Switching regulators are those which operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continously.This give improved efficiency over series regulators.

8.What are the advantages of IC voltage regulators?(Remember) (April /May 2017)

*low cost
*highreliability
*reduction in size
*excellent performance

9. Give some examples of monolithic IC voltage regulators:(Remember)

78XX series fixed output, positive voltage regulators
79XX series fixed output, negative voltage regulators
723 general purpose regulators.

10.What is the purpose of having input and output capacitors in three terminal IC regulators?[Apr/May 2021]

A capacitor connected between the input terminal and ground cancels the Inductive effects due to long distribution leads. The outputcapacitor improves the transient response.

11.**Define line regulation. [NOV/DEC 2013],[NOV/DEC 2014][APR/MAY 2018]**

Line regulation is defined as the percentage change in the output voltage for a change in the inputvoltage. It is expressed in mill volts or as a percentage of the output voltage.

12.Define load regulation. [NOV/DEC 2014]

Load regulation is defined as the change in output voltage for a change in load current. It is expressed in millivolts or as a percentage of the output voltage.

13.What is meant by current limiting? (Remember) [APR/MAY 2015]

Current limiting refers to the ability of a regulator to prevent the load current from increasing above a preset value.

14.Give the drawbacks of linear regulators:(Remember)

*The input step down transformer is bulky and expensive because of low line frequency.
*Because of low line frequency, large values of filter capacitors are required to decrease the ripple.
*Efficiency is reduced due to the continuous power dissipation by the transistor as it operates in the linear region

15.What is the advantage of monolithic switching regulators? (MAY 2010)

*Greater efficiency isachieved as the power transistor is made to operate as low impedance switch.Power transmitted across the transistor is in discrete pulses rather than as a steady current flow

*By using suitable switching loss reduction technique, the switching frequencycan be increased so as to reduce the size and weight of the inductors and capacitors.

16. What is an opto-coupler IC? Give examples. (MAY 2010) [MAY/JUNE 2014]

Opto-coupler IC is a combined package of a photo-emitting device and a photo sensing device.
Examples for opto-coupler circuit: LED and a photo diode, LED and photo transistor, LED and Darlington.
Examples for opto-coupler IC: MCT 2F, MCT 2E.

17. Mention the advantages of opto-couplers:(Remember) [Apr/May 2021]B

*Better isolation between the two stages.
*Impedance problem between the stages is eliminated.
*Wide frequency response.
*Easily interfaced with digital circuit.
*Compact and light weight.
*Problems such as noise, transients, and contact bounce are eliminated.

18. What is an isolation amplifier? Mention it's application (MAY/JUNE 2010) [APR/MAY 2016]

An isolation amplifier is an amplifier that offers electrical isolation between its input and output terminals.

19. What is the need for a tuned amplifier? (Remember) (MAY 2009)

In radio or TV receivers, it is necessary to select a particular channel among all other available channels. Hence some sort of frequency selective circuit is needed that will allow us to amplify the frequency band required and reject all the other unwanted signals and this function is provided by a tuned amplifier.

.

20. Write the frequency of oscillation (f0) equation for triangularwave generator) (MAY10)

f0=R3/4R1C1R2

21. How frequency to voltage converted onOP-AMPS. (MAY 2010)

A Frequency to voltage converter produces an output voltage, whose amplitude is a function of frequency of the input signal. The input signal may be a sine wave, a square wave or a pulse train. The F/V converter is essentially an FM detector or discriminator.

22. What is video amplifier? (MAY/JUNE 2010)

The video or wideband amplifiers are designed to provide a relatively flat gain versus frequency response characteristics for the range offrequencies required to transmit video information.

25. Define Multivibrators. Mention its types.[APR/MAY 2019] (MAY/JUNE 2010)[MAY/JUNE 2014]

Multivibrators are regenerative circuits, which are mainly used in timing applications. Based on their operational characteristics they can be classified into

•AstableMultivibrators
•MonostableMultivibrators
• BistableMultivibrator

What are thethree different wave forms generated by ICL8038?[APR/MAY 2010]
Sine wave, Square wave & Triangular wave.

26. What is meant by thermal shutdown applied to voltage regulators?[NOV/DEC 2010]
The IC has a temperature sensor which turns off the IC when it becomes too hot. The output current will drop and remain there until IC has cooled significantly.

27. What is an opto-coupler IC? Mention its applications. [APR/MAY 2011]
It is combined package of LED and Photodiode.

28.Define the duty cycle inAstablemultivibrator using IC 555. [APR/MAY 2011]
Duty cycle = (Rb/ R
a+2Rb
)*100

29. What are the limitations of three terminal regulators [APR/MAY 2012]
1. No short circuit protection.
2. Output voltage is fixed.

30.What is switched capacitor filter. (Remember) [NOV/DEC 2013]

A switched capacitor filter is a three terminal element which consistsof capacitors, periodic switches and op-amps whose open circuit voltage transfer function represents filter characteristics.
37. Give the formula for period of oscillations in an op-amp as table circuit. [May/June 13]

T = 2RC ln(1+β / 1-β)

31. Define duty cycle of a periodic pulse wave form. [May / June 2013]

Duty cycle = (Rb / Ra+2Rb)*100

32. State the two conditions for oscillations? [APR/MAY 2015]

1. The loop gain is equal to unity in absolute magnitude and
2. Thephase shiftaround the loop is zeroor an integer multiple of 2π

33. What is the purpose of connecting a capacitor at the input and the output side of an IC voltage

regulator? [NOV/DEC 2015]

The figure above shows the application of LM340 IC as a voltage regulator. Pins 1, 2, and 3 are the input, output and ground When there is quite a distance (in cms) from the IC to the filter capacitor of the unregulated power

supply, there may occur unwanted oscillations within the IC due to lead inductances within the circuit. In order to remove this unwanted oscillation, the capacitor C1 has to be placed as shown in the circuit.
Capacitor C2 is sometimes used to improve the transient response of the circuit.
Any device in the LM 340 series needs a minimum input voltage at least 2 to 3 V greater than the regulated output voltage. Otherwise, it will stopregulating. Furthermore, there is a maximum input voltage because of excessive power dissipation.

34. Mention two applications of frequency to voltage converter.(Remember) [NOV/DEC 2015]

1. Frequency to voltage converter in tachometers.
2. Frequency difference measurement.

35. Write the advantages of switching regulator over series voltage regulators. [R2008 NOV/DEC 2015]

	Linear regulator	Switching regulator
Buck Boost Buck/Boost Inverting	Possible Impossible Impossible Impossible	Possible Possible Possible Possible
Efficiency	V_o/V_{in} Mostly low	Approx. 95% Usually high
Output power	Generally several watts Depending on thermal design	Large power possible
Noise	Low	Switching noise exists
Design	Simple	Complicated
Parts count	Low	High
Cost	○	△

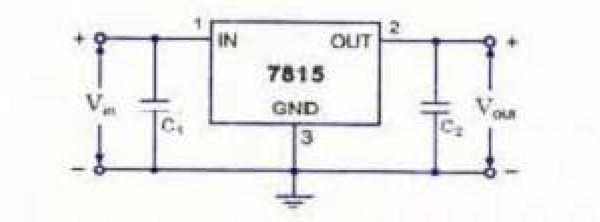
36 Distinguish the principle of linear regulator and a switched mode powersupply. (April/May 2017)

A switching power supply operates by constantly switching the source on and off; the rate of which is dictated by the needed voltage at the output. A linear power supply is often used because of its simplicity.
Linear regulators exist in packaged ICs that only need a rectified voltage source to operate.
49) Define current transfer ratio of an opto-coupler?[Nov/Dec 2017

The current transfer ratio refers to the ratio of the output collector current (Ic)to the input forward

current(If)CTR ={Ic/If}*100

Draw a fixed voltage regulator circuit and state its operations?[Nov/Dec 2017]



Connection of 7815 Voltage Regulator

38 .List the applications of multivibrator??[Nov/Dec 2018](Remember)

Frequency divider
Pulse width Modulation
Linear ramp generator

Square wave generator
VCO
Schmitt trigger

39. State the function of optocoupler. [APR/MAY 2019])

Optocoupler provides electrical isolation between two circuits

EPC Questions

1. Explain the square wave generator, triangular wave generator and Saw tooth wave generator with neat diagram (A/M 2020, N/D 2018,A/M 2019,A/M 2016.2014
2. Explain switched capacitor filter , audio power amplifier, Video Amplifier opto coupler, Isolation Amplifier (April May 2017), [APR/MAY 2016][NOV/DEC 2017][APR/MAY 2019
3. Explain the functional block diagram r and basic low voltage and high voltage regulator.
4. With neat diagram, explain the operation of an astable and monostable multivibrator .Drive duty cycle A/M 2021, [NOV/DEC 2017] [NOV/DEC 2018]
5. With neat diagram, explain the operation of an monostable multivibrator [NOV/DEC 2017] [NOV/DEC 2018]