

MOHAMED SATHAK A.J. COLLEGE OF ENGINEERING

 $({\sf Approved}\,{\sf by}\,{\sf AICTE}, {\sf New}\,{\sf Delhi}\,{\sf and}\,{\sf Affiliated}\,{\sf to}\,{\sf Anna}\,{\sf University}, {\sf Chennai})$





Department of Electronics and Communication Engineering Innovative Teaching Methods

Activity Title	Role Play			
Faculty Name/Department	Dr.I.Manju / ECE			
Mapped Course Name & Code	CEC370 Low Power IC Design			
Date	25.08.23			
Benefitted Students (Year / Sem / Dept)	III/V/ECE			
Topic	Pipelining Approach to achieve low power			
Description	Role play exercises give students the opportunity to assume the role of a process or concept. These roles can be performed by individual students, in pairs, or in groups help to understand engineering concepts. In the above activity students assumed the roles of registers and logic blocks to perform the process of pipelining. Various scenarios were enacted to understand the tradeoffs between area, speed and low power.			
Course Outcomes (CO)	CO2: Explain the fundamentals of architectural approaches in low power design.			
Performance Indicator (PI)	1.4.1			
Mail ID (for review)	ece.manju@msajce-edu.in			
Activity Photos	Siruseri, Tamil Nadu, India Mohamed Sathak Campus Rd, Siruseri, Tamil Nadu 603103, India Lat 12.835657° Long 80.219434° 25/08/23 09:15 AM GMT +05:30			

Topics/ Questions:

- 1. Normal Circuit Operation
- 2. Pipelining Approach to achieve low power
- 3. Hardware replication approach to achieve low power

Marks:

Group Name	Reg. No.	Topic	Marks		
			Presentation (10)	Subject Knowledge (10)	Total (20)
A	Roll no: 1-11	Normal Circuit Operation	10	9	19
В	Roll no: 12-22	Hardware replication approach to achieve low power.	10	8	18
С	Roll no: 23-33	Pipelining Approach to achieve low power.	9	10	19

Outcome:

- 1. Better understanding on the tradeoffs between area, speed and low power.
- 2. Better understanding on the low power architectural methods.