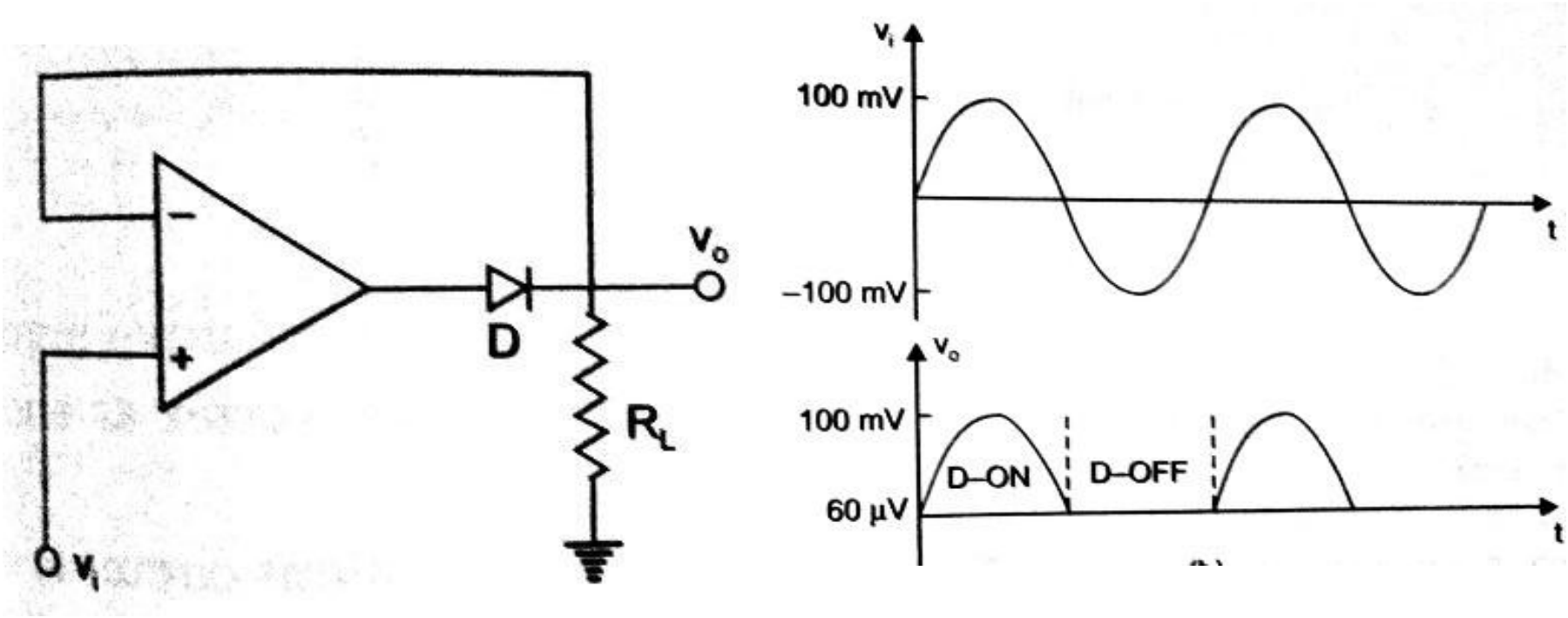
UNIT-II

Applications of Op Amp

Precision Rectifier

- A precision rectifier differs from ordinary diode rectifier.
- If a ordinary diode is used, the cut in voltage is 0.6V for silicon or 0.3 for germanium. So a input voltage greater than cut in voltage can only be rectified.
- This drawback is eliminated in precision rectifier by placing a ordinary diode in feed back path of an OPAMP.
- The actual cut in voltage of diode is divided by large open loop gain of OPAMP (10^4). So the cut in Voltage restriction can be reduced substantially.
- Even input signal in the range of milli -volts can be effectively rectified.

Precision Rectifier



$$^{0.6}/_{10^4} = 60\mu V$$

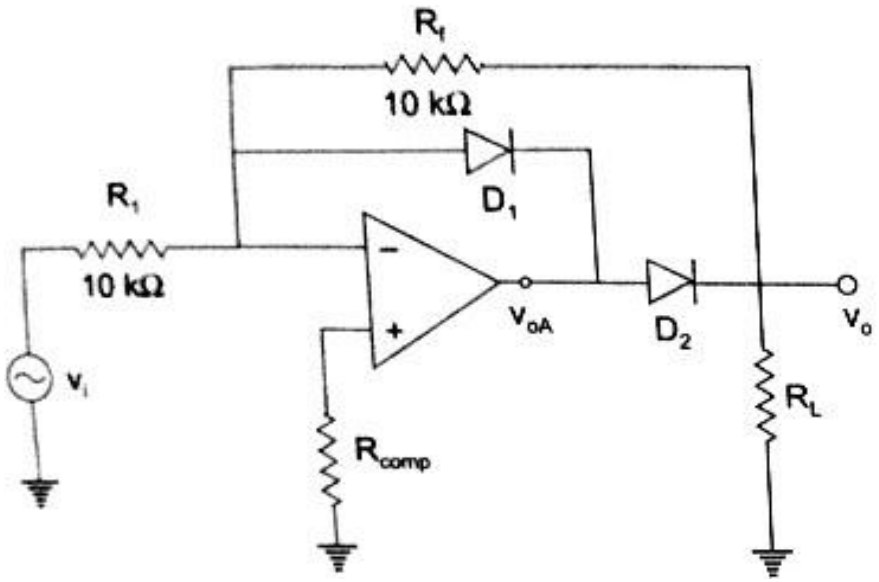
Application Precision Diode

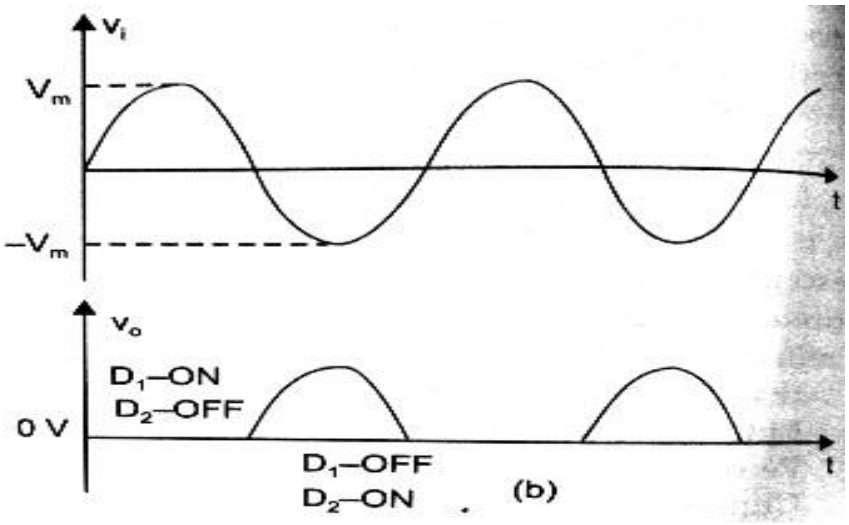
- Half wave rectifier
- Full wave rectifier
- Peak value detector
- Clipper
- Clamper

Half Wave Rectifier

Half Wave Rectifier

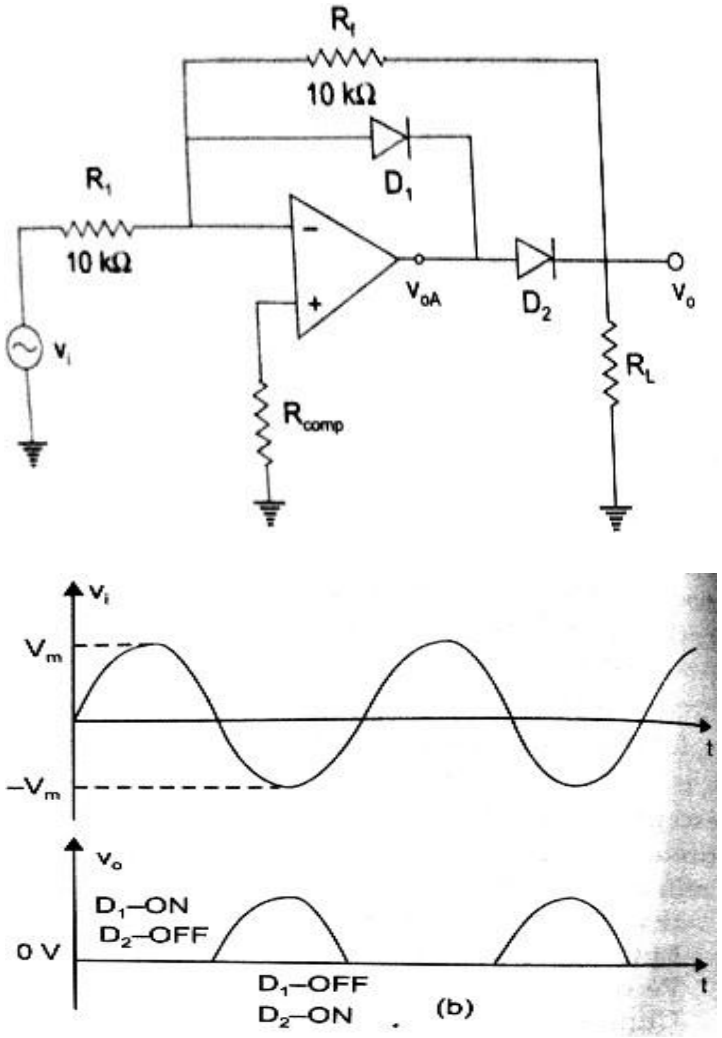
- Two diodes D1 and D2 are connected in the feedback path of OPAMP to form a half wave rectifier.





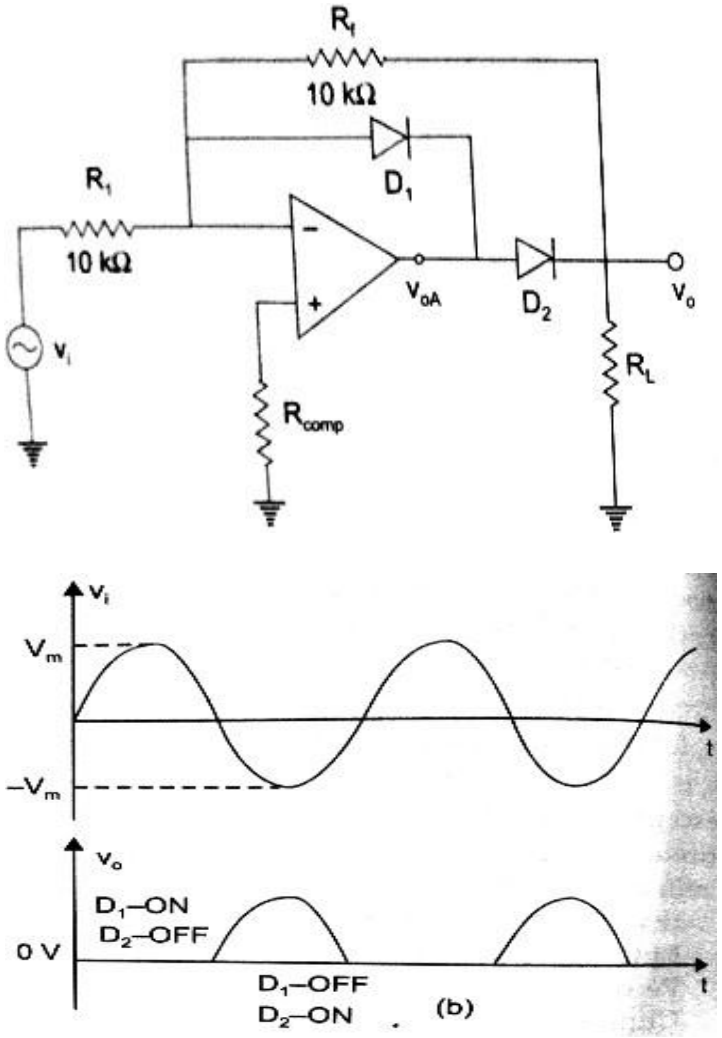
During Positive Half Cycle

- Since the input Vi is applied at inverting terminal of OPAMP, the output V_{OA} is negative half cycle for the positive half cycle of Vi
- D1 is forward bias and D2 is reverse biased when input is positive half cycle.
- No current flows at output during the positive half cycle of input voltage.



During Negative Half Cycle

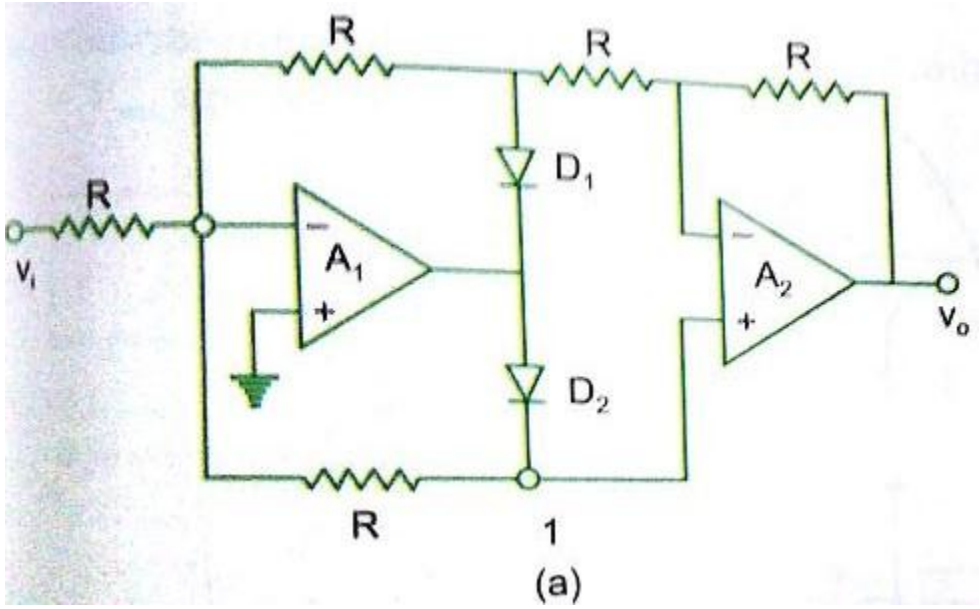
- input Vi is negative half cycle applied at inverting terminal of OPAMP, the output V_{OA} is positive half cycle for the negative half cycle of Vi
- D1 is reverse bias and D2 is forward biased when input is negative half cycle.
- Current flows at output during the negative half cycle of input voltage.



Full Wave Rectifier

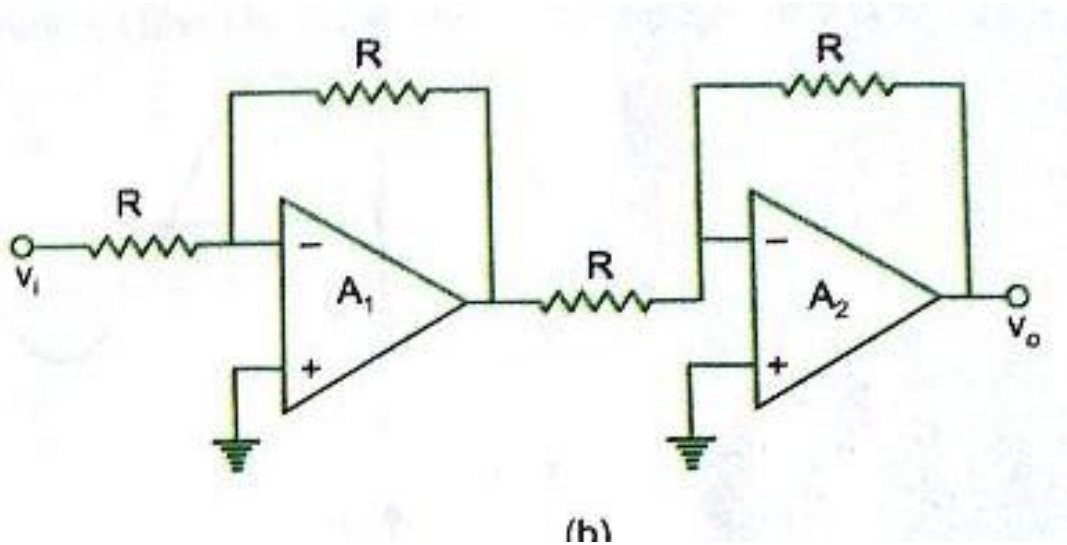
Full Wave Rectifier

- Two OPAMP and two diodes can be combined to perform full wave rectification.



During Positive Half Cycle

- For positive input voltage Vi>0, diode D1 is ON and D2 is OFF.
- Both the OPAMP A1 and A2 act as inverter.
- Equivalent circuit

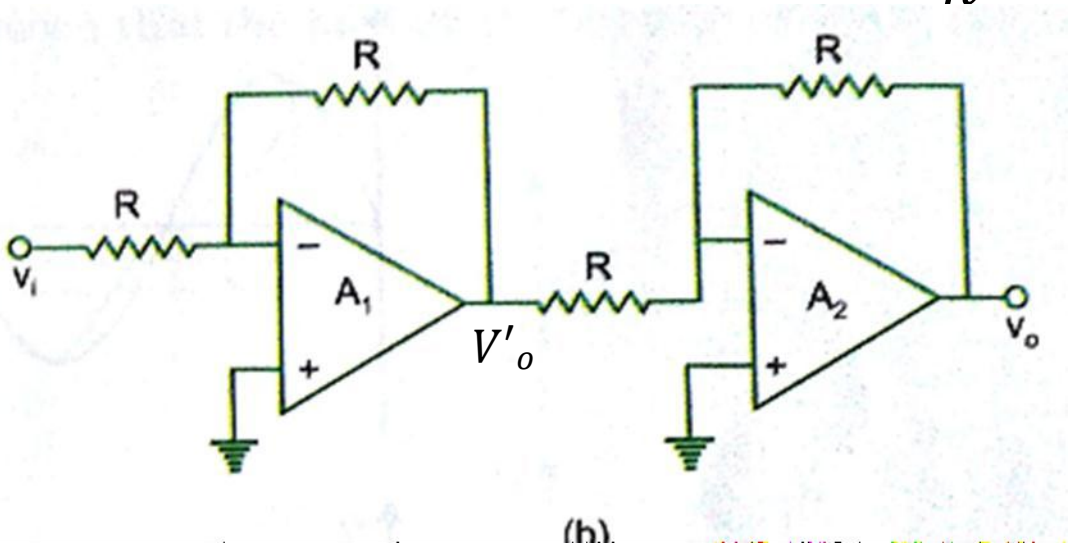


During Positive Half Cycle

A1 OPAMP Output : $V'_o = -\left(\frac{R}{R}\right) V_{in} = -V_{in}$

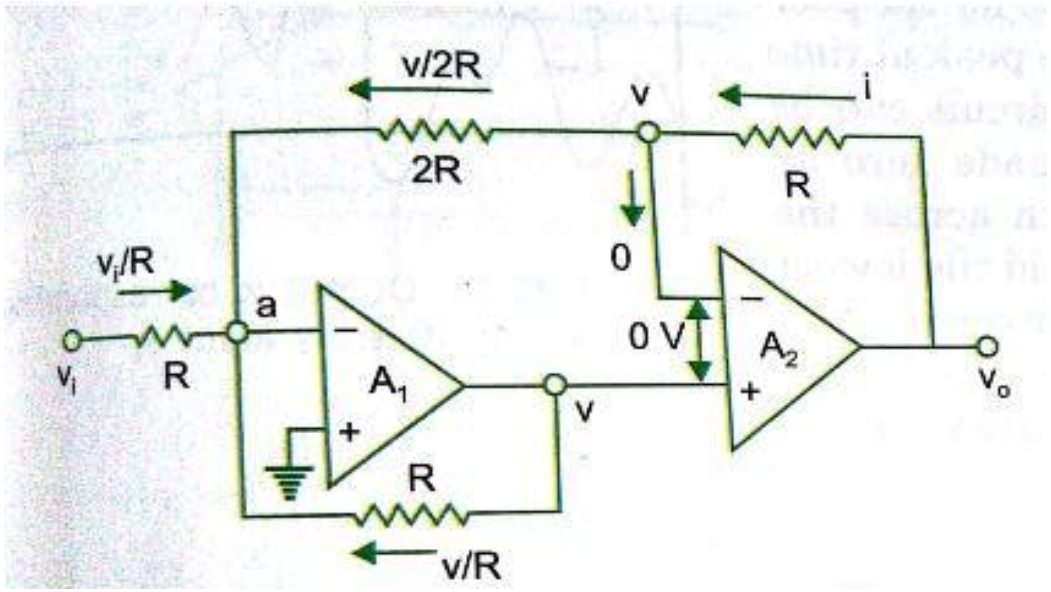
A2 OPAMP Output:

$$V_o = -\left(\frac{R}{R}\right) V'_o = -V'_o = -(-V_{in}) = V_{in}$$



During Negative Half Cycle

- For positive input voltage Vi<0, diode D1 is OFF and D2 is ON.
- OPAMP A1 act as inverter and OPAMP A2 act as Non-inverter
- Equivalent circuit

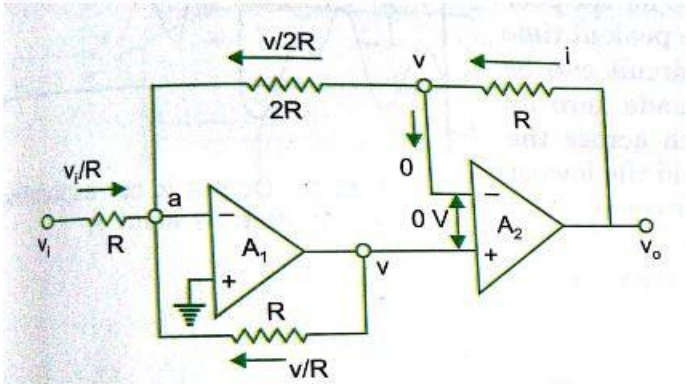


During Negative Half Cycle

- KCL at Node 'a' gives

$$\frac{v_i}{R} + \frac{v}{2R} + \frac{v}{R} = 0 \qquad (1)$$

$$v = -\frac{2}{3} v_i \qquad (2)$$

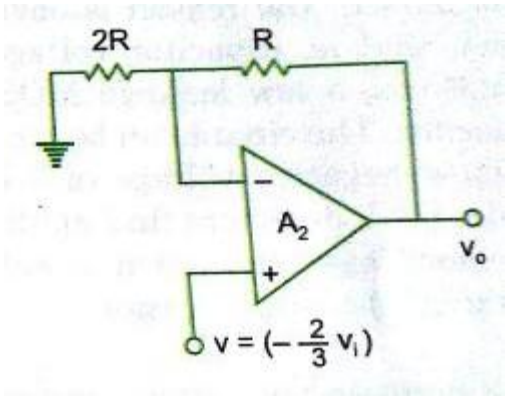


1st OPAMP output is connected to Non inverting terminal of 2nd OPAMP

$$v_o = \left(1 + \frac{R}{2R}\right) v \qquad (3)$$

Substitute (2) in (3)

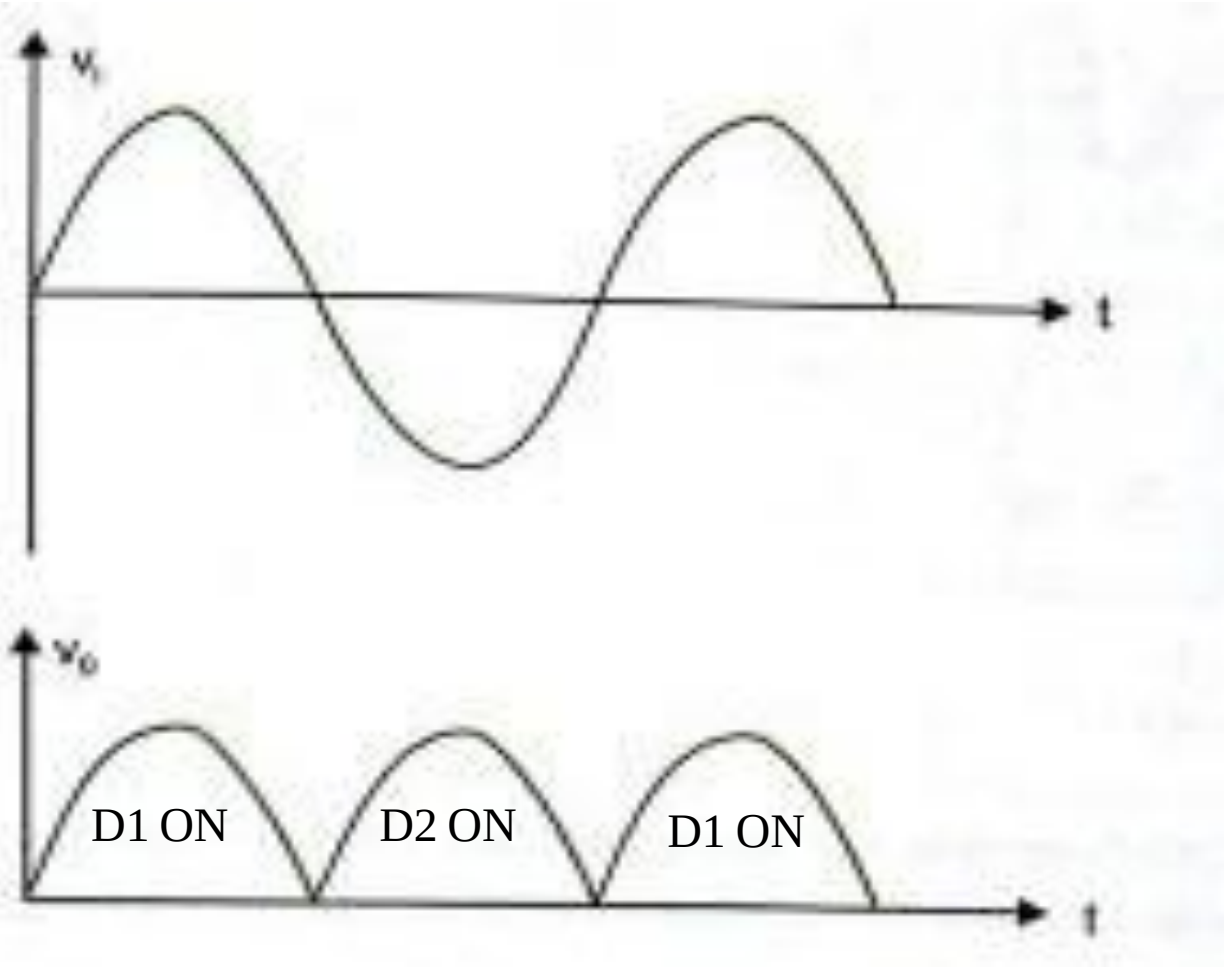
$$v_o = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3} v_i\right) = -v_i$$



Input voltage also negative half cycle

$$v_o = -(-v_i) = v_i$$

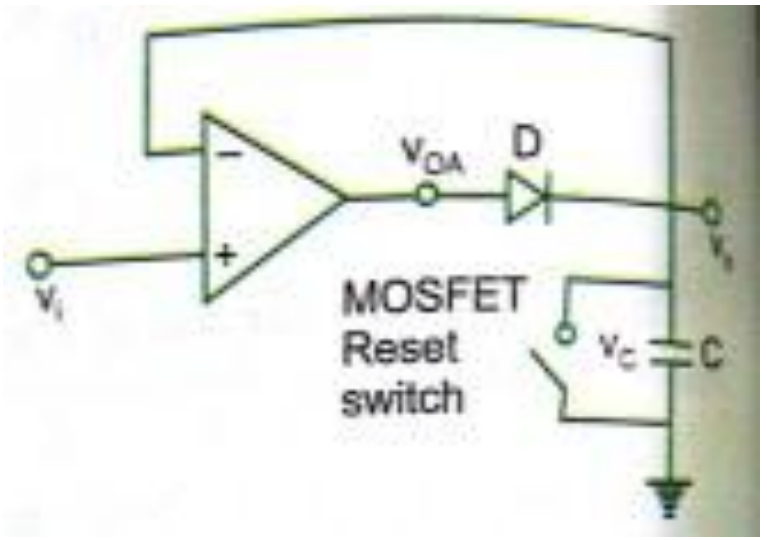
During Positive Half Cycle



Peak Detector

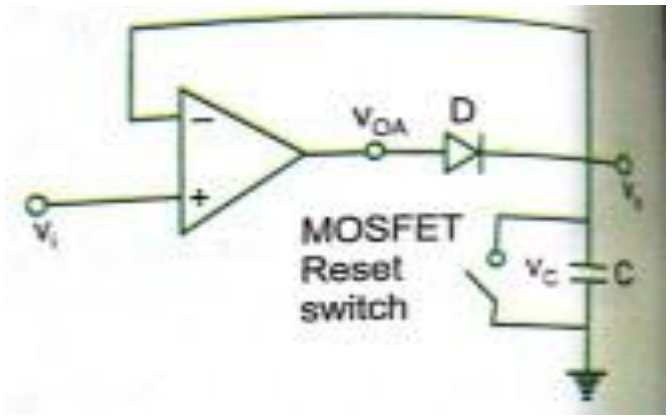
Peak Detector

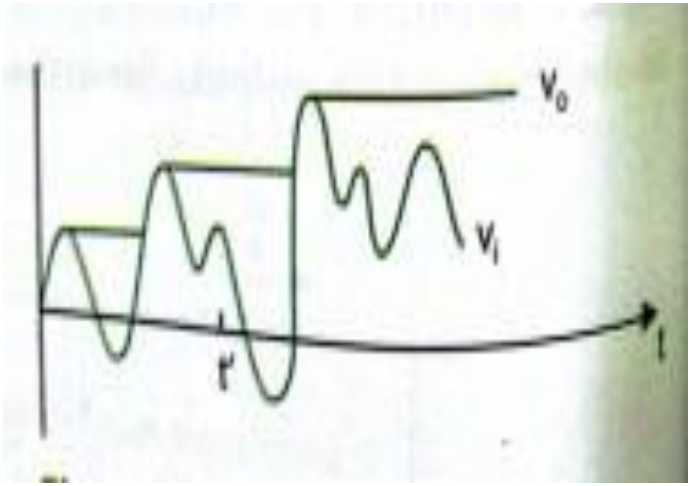
- The circuit which stores the highest value (peak) of the given input signal is called as peak detector.
- This is achieved by charging a capacitor.
- If a higher peak value comes along, this new value is stored.
- This highest peak value stored until the capacitor is discharged.



Peak Detector

- When input Vi exceeds Vc, the diode D is forward biased and the circuit is voltage follower, the output voltage Vo follows Vi as long as Vi exceeds Vc.
- When Vi drops below Vc, the diode becomes reverse biased and capacitor holds the charge till input voltage again attains a value greater than Vc.
- The circuit can be reset, that is, capacitor voltage can be made zero by connecting a low leakage MOSFET switch across the capacitor.
- The circuit can be modified to hold the lowest or most negative voltage of a signal by reversing the diode.





Peak Detector Application

- Test and measurement instrumentation
- Amplitude modulation (AM) Communication

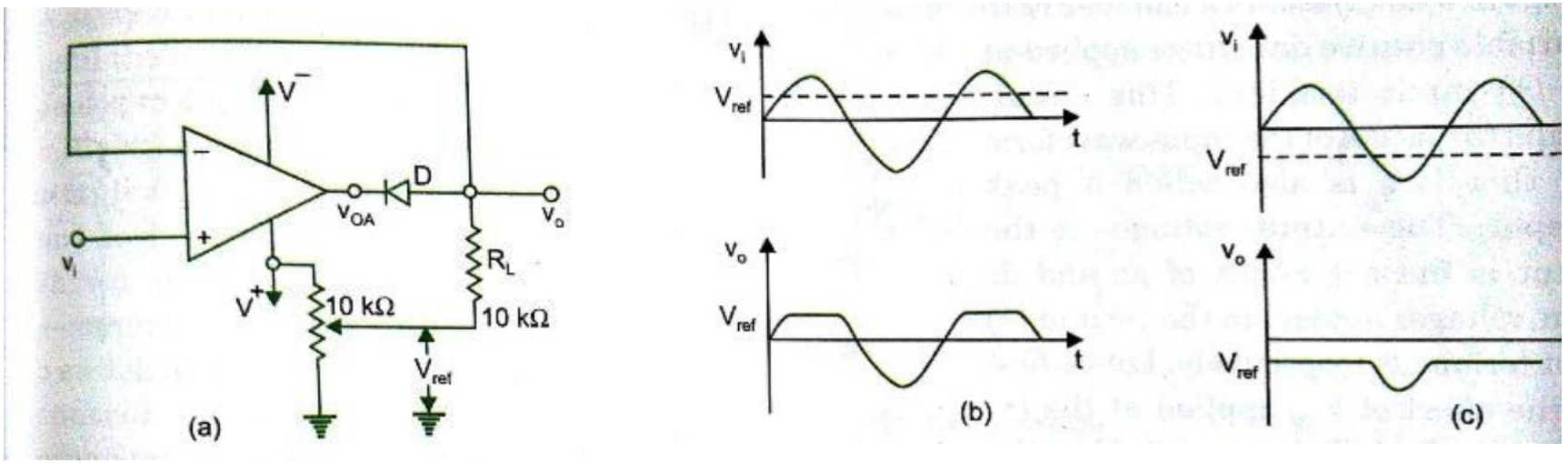
Clipper

Clipper

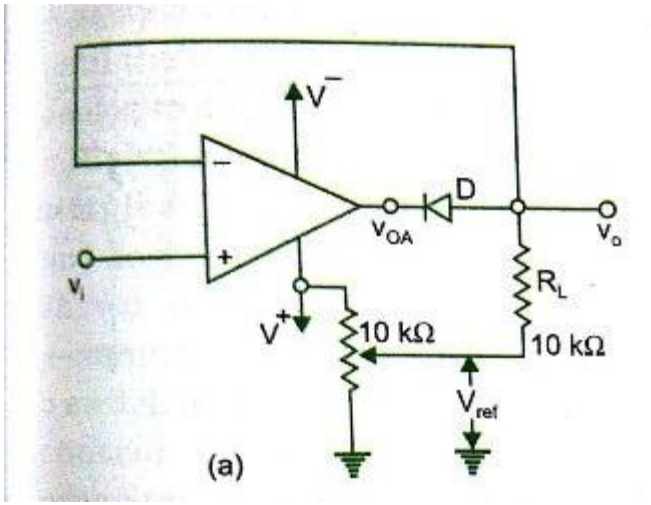
- An OPAMP and diode can perform clipping operation.
- A clipper is a circuits which to remove undesired portion of the input waveform.
- Depending on which portion a clipper removes.
  - Positive Clipper
  - Negative Clipper

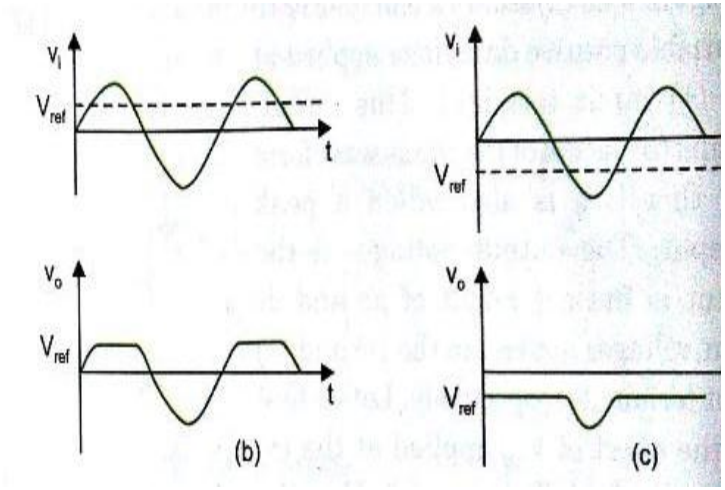
Positive Clipper

- The clipping level is determined by the reference voltage v_{ref} and could be obtained from the positive supply voltage v^{+}.



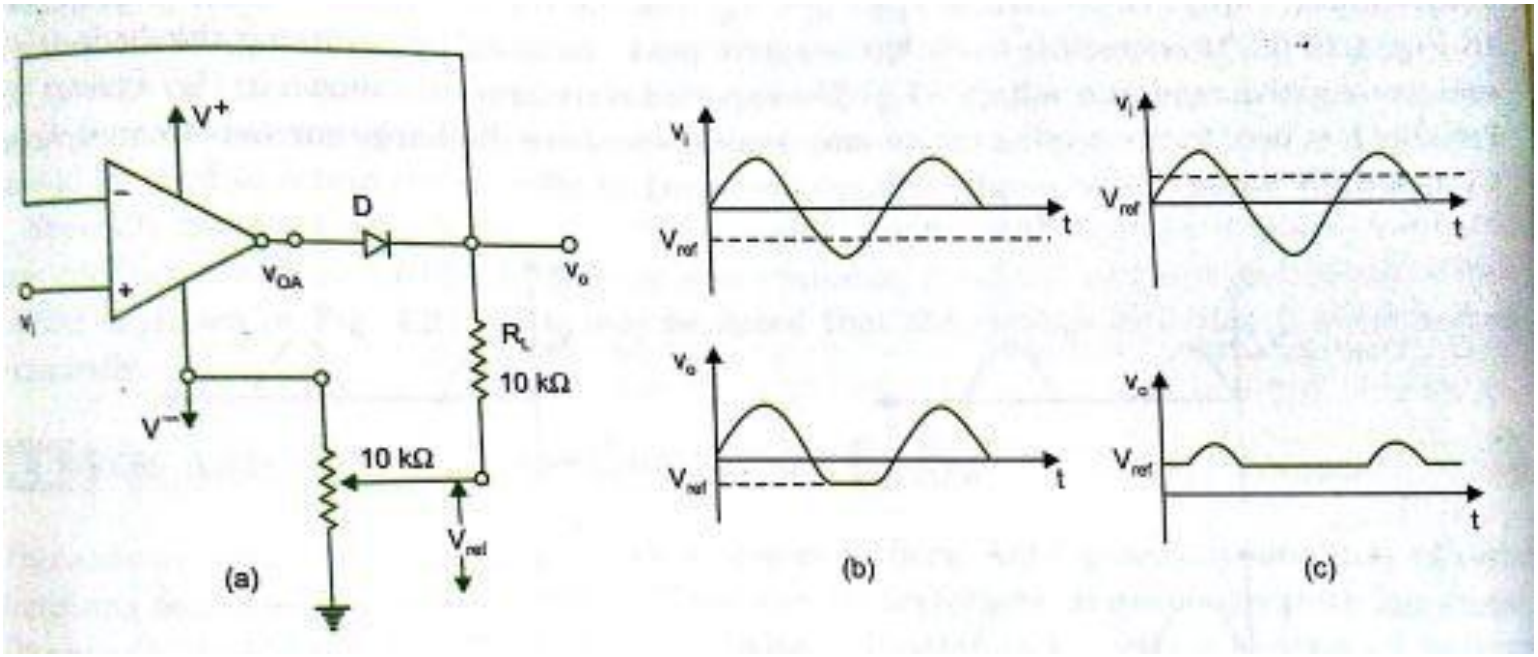
- It can seen that the portion of the output voltage for $v_o > v_{ref}$ are clipped off.
- For input voltage $v_o < v_{ref}$ diode D conducts .
- The OPAMP works as a voltage follower and output v_o follows input v_i till $v_o \leq v_{ref}$
- When v_i is greater than v_{ref}, the output v_{OA} of the OPAMP is larger enough to drive D into cutoff.
- The OPAMP operates in the open-loop and output voltage $v_o = v_{ref}$.
- However, if v_{ref} is made negative, then the entire output waveform above v_{ref} will get clipped off.





Negative Clipper

- The positive clipper can be easily converted into a negative clipper by simply reversing diode D and changing polarity of reference voltage v_{ref}.
- The negative clipper clips off the negative parts of the input signal below the reference voltage.

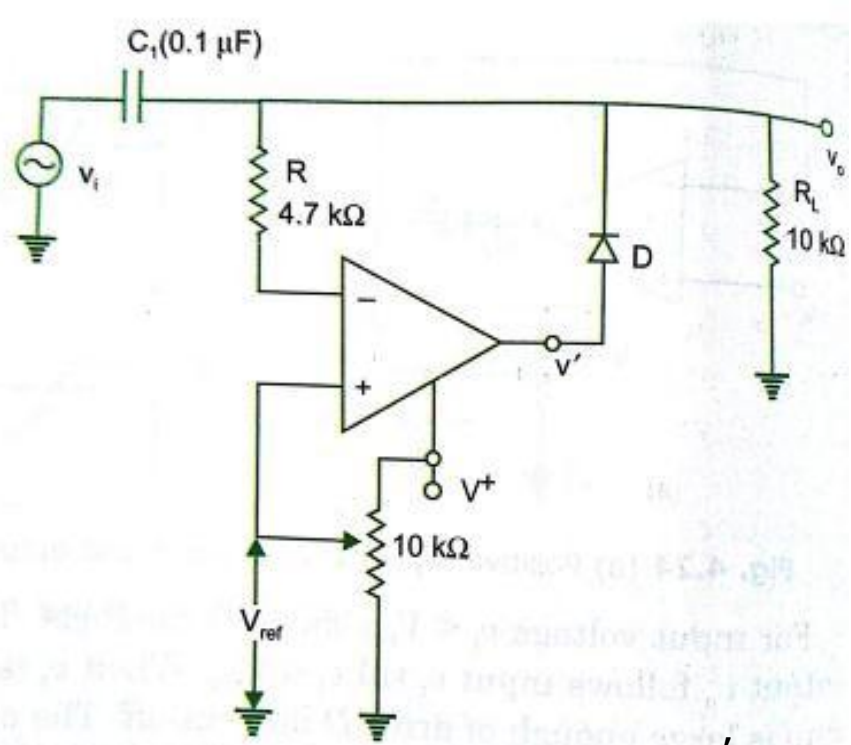


Clamper

Clamper

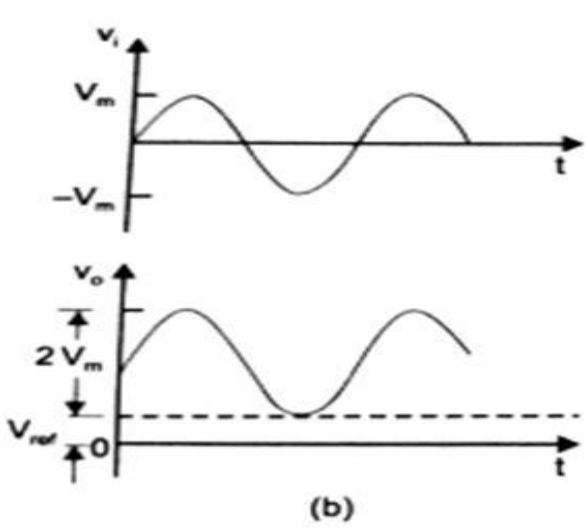
- The clamper is also known as dc inserter or restorer.
- The circuit is used to add a desired dc level to the output voltage (or) the output is clamped to a desired dc level.
- If clamped dc level is positive, it is called positive clamper.
- If clamped dc level is negative, it is called negative clamper.

- The output voltage in a circuit is the net result of ac and dc input voltages applied to the (-) and (+) input terminals.

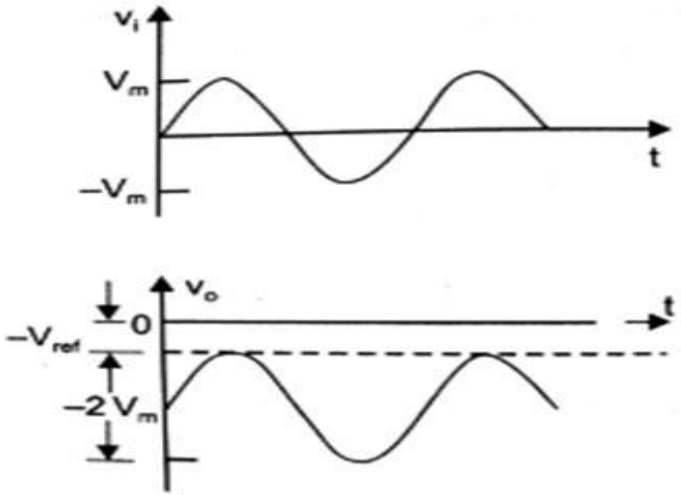


- v_{ref} applied to the (+) terminal, the output of OPAMP v' is also positive.
- So that the diode D is forward biased. The circuit operates as a voltage follower and therefore output voltage $v_o = +v_{ref}$

- Then consider the ac signal $v_i = v_m sin\omega t$ applied at the (-) input terminals.
- During the negative half cycle of v_i diode D conduct.
- The capacitor C1 charges through diode D to the negative peak voltage v_m.
- However during the positive half cycle D reverse bias. The capacitor retains its previous voltage v_m.
- This v_m is in series with the ac input signal, the output voltages now will be v_i+v_m. The total output voltages is, v_{ref}+v_i+v_m.



(b)



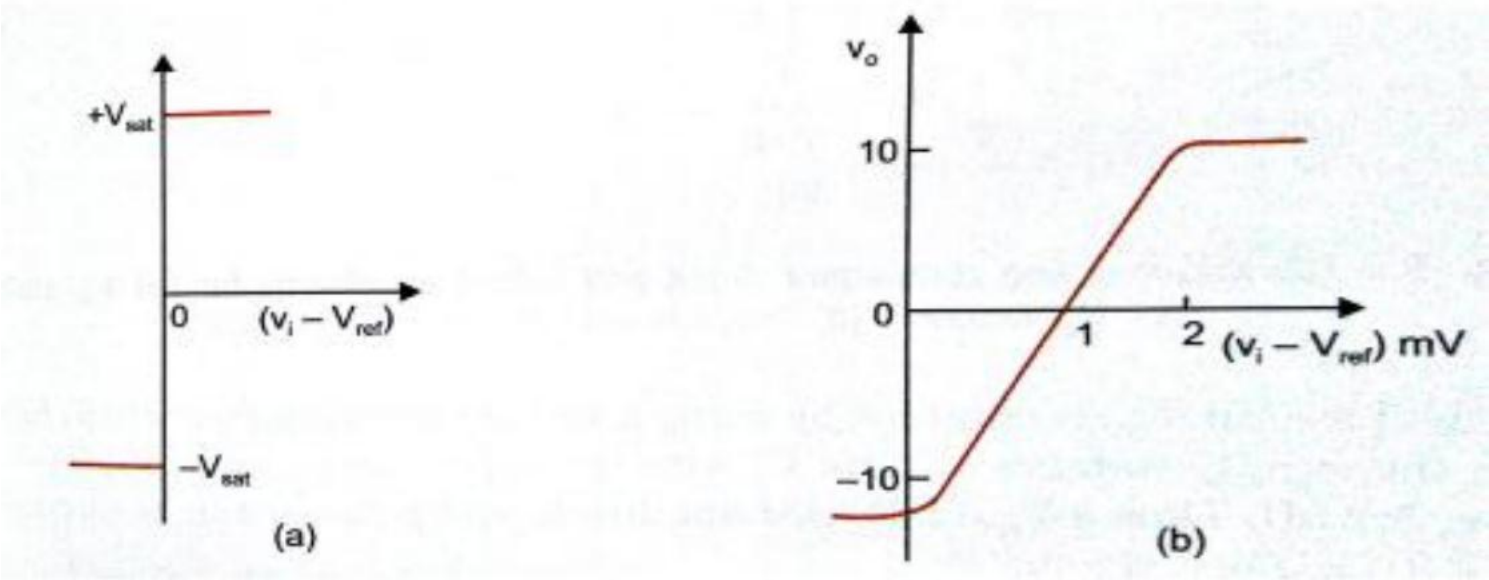
(c)

- To obtain the negative peak clamping by reversing the diode D and using negative reference voltage $-v_{ref}$.
- The resistor R is used for protecting the OPAMP against excessive discharge currents from capacitor C1 especially when the dc supply voltages are switched off.

Comparator

Comparator

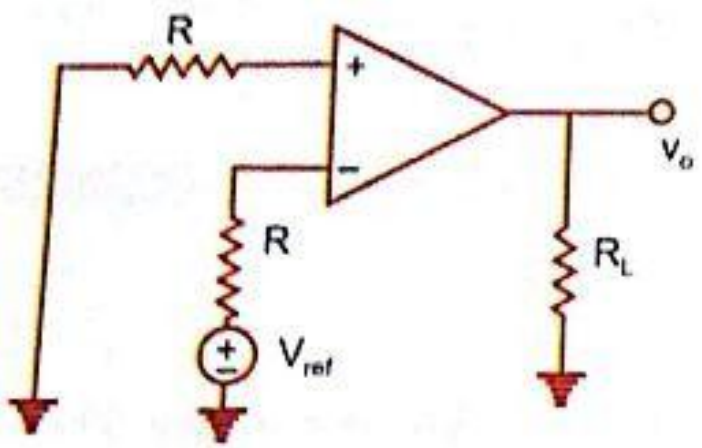
- Comparator is a circuit which compares a signal voltage applied at one input of an OPAMP with a known reference voltage at the other input.
- It is bascally an open loop OPAMP with output $\pm v_{sat} = v_{cc}$

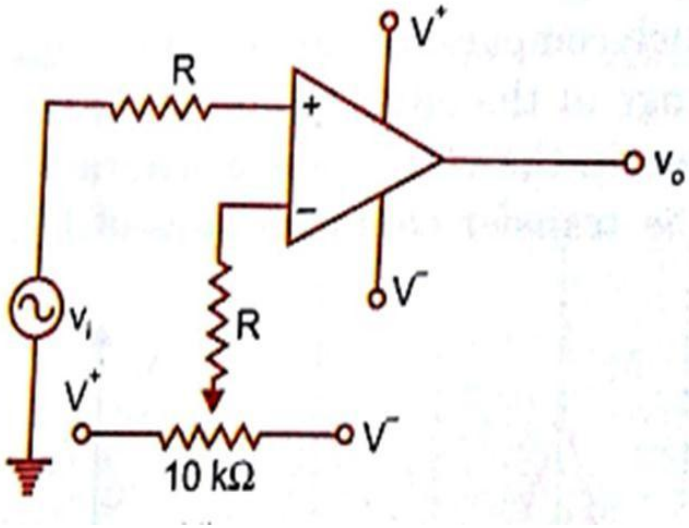


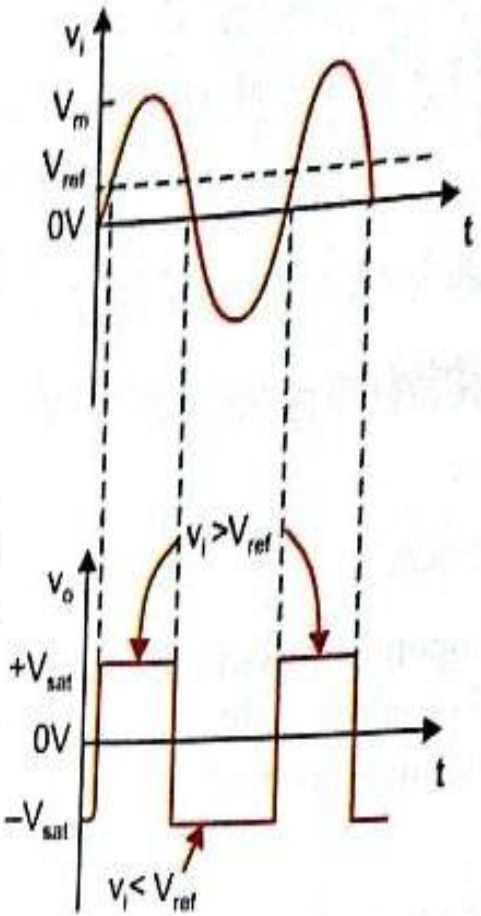
Comparator Types

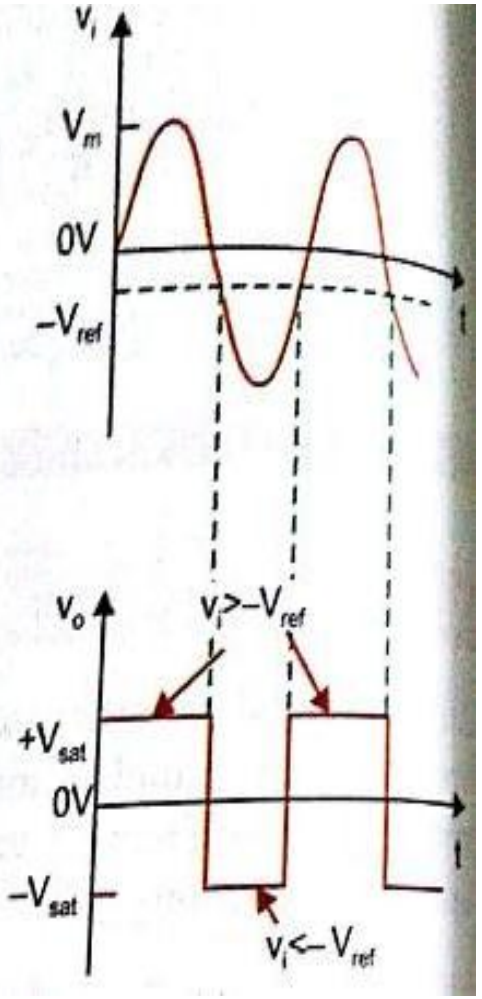
- Non inverting comparator
- Inverting comparator

Non Inverting Comparator



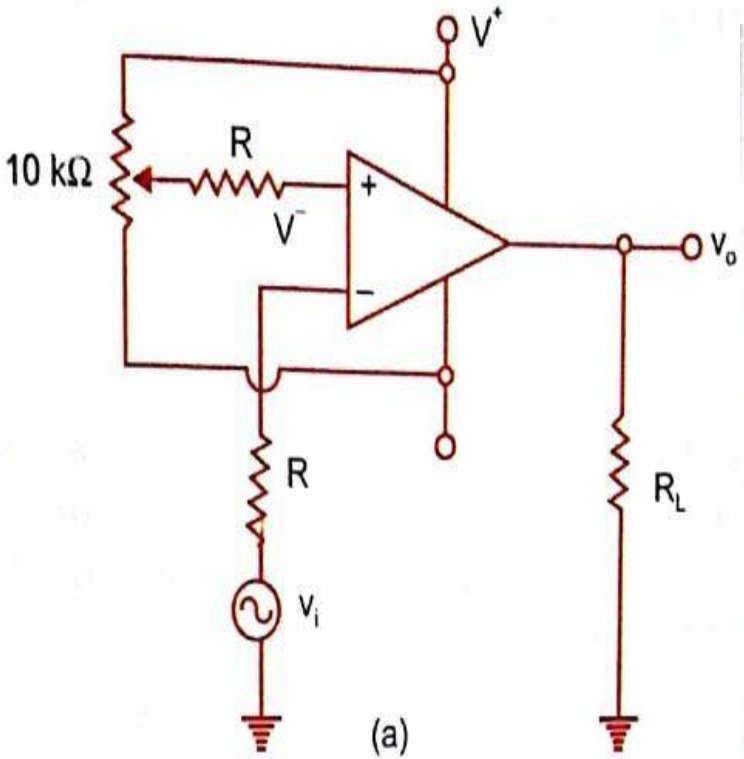


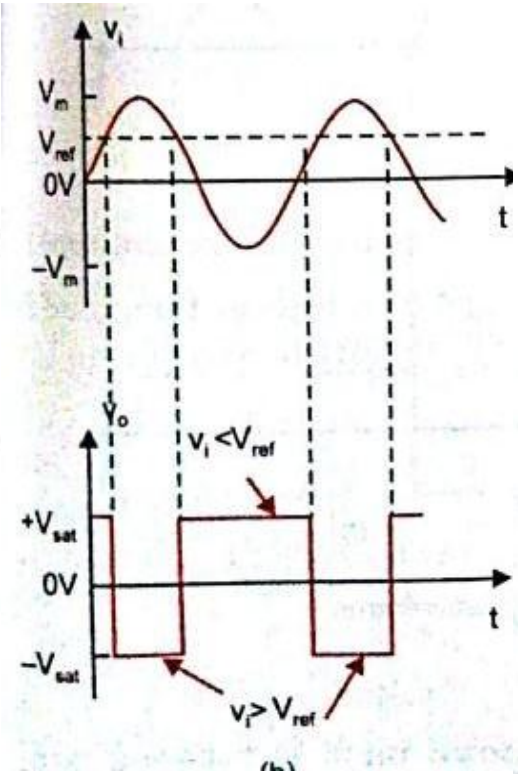


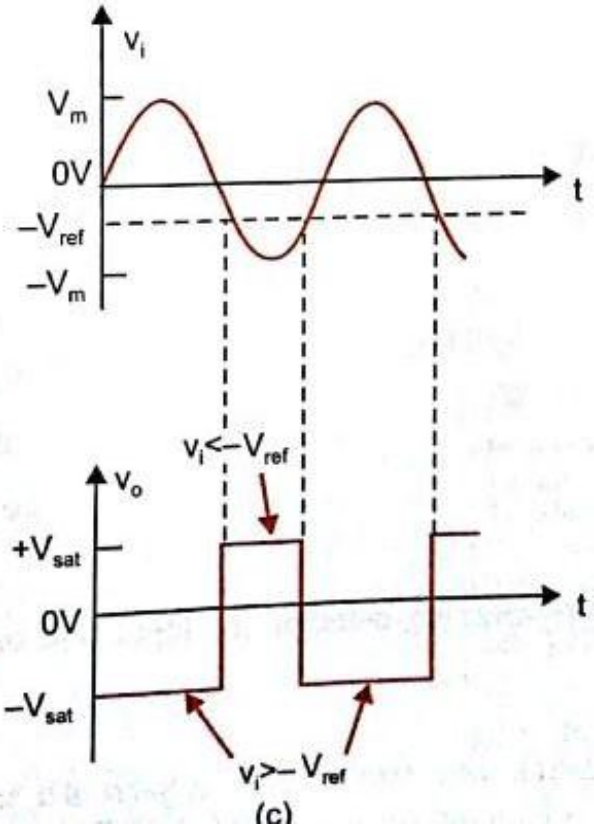


- A fixed reference voltage v_{ref} applied to (-) input and a time varying signal v_i is applied to (+) input.
- The output voltage is $-v_{sat}$ for $v_i < v_{ref}$ and v_o goes to $+v_{sat}$ for $v_i > v_{ref}$
- The practical circuit v_{ref} is obtained by using a 10kΩ potentiometer which forms a voltage divider with the supply voltages $V^+$and V^- with wiper connected to (-) input terminals.

Inverting Comparator







- A fixed reference voltage v_{ref} applied to (+) input and a time varying signal v_i is applied to (-) input.
- The output voltage is $+v_{sat}$ for $v_i < v_{ref}$ and v_o goes to $-v_{sat}$ for $v_i > v_{ref}$
- The practical circuit v_{ref} is obtained by using a 10kΩ potentiometer which forms a voltage divider with the supply voltages $V^+$and V^- with wiper connected to (+) input terminals.

Application of Comparator

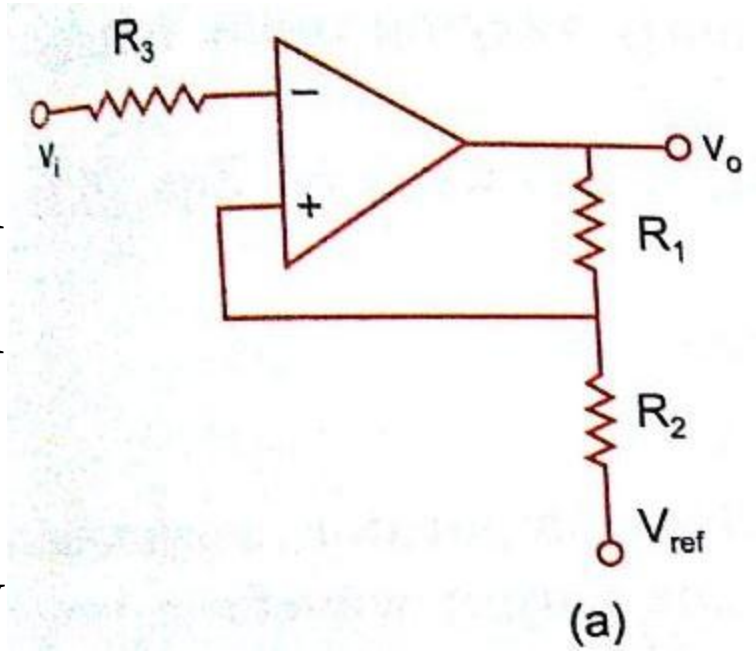
- Zero crossing detector
- Window detector
- Time marker generator
- Phase meter

Schmitt Trigger
(Regenerative Comparator)

Schmitt Trigger

- If positive feedback is added to the comparator circuit, gain can be increased greatly.
- Consequently, the transfer curve of comparator becomes more close to ideal curve.
- Theoretically if the open loop gain $-\beta A_{OL}$ is adjusted unity, then the gain with feedback A_{vf} becomes infinity.
- This result in an abrupt (zero rice time) transition between the extreme values of output voltage.
- In practical circuits, however it may not be possible to maintain loop gain exactly equal to unity for a long time because of supply voltage and temperature variations. So the value greater than unity is chosen.
- This also gives an output waveform virtually discontinuous at the comparison voltage.

- Schmitt trigger is one of the important application of comparator.
- A inverting comparator with positive feedback is called as schmitt trigger.
- The circuit converts any irregular shaped input wave to square wave.

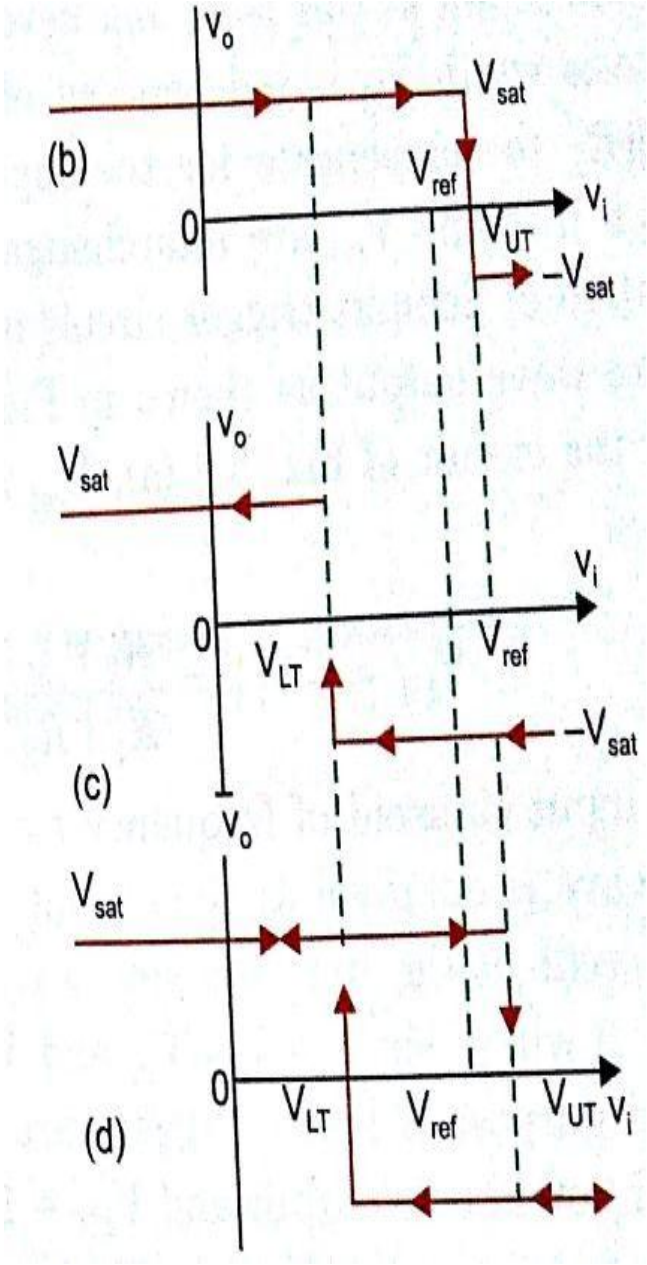


- The input voltage is applied to the (-) input terminal and feedback voltage to the (+) input terminal.
- The input voltage v_i triggers the output voltage v_o every time it exceeds certain voltage levels.
- These voltage levels are called upped threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}).
- The hysteresis width is the difference between these two threshold voltage i.e V_{UT}-V_{LT}

- Suppose the output $v_o = +V_{sat}$. The voltage at (+) input terminal can be obtained by using superposition.

$$V_{UT} = \frac{v_{ref} R_1}{R_1 + R_2} + \frac{R^2 V^{sat}}{R_1 + R_2}$$

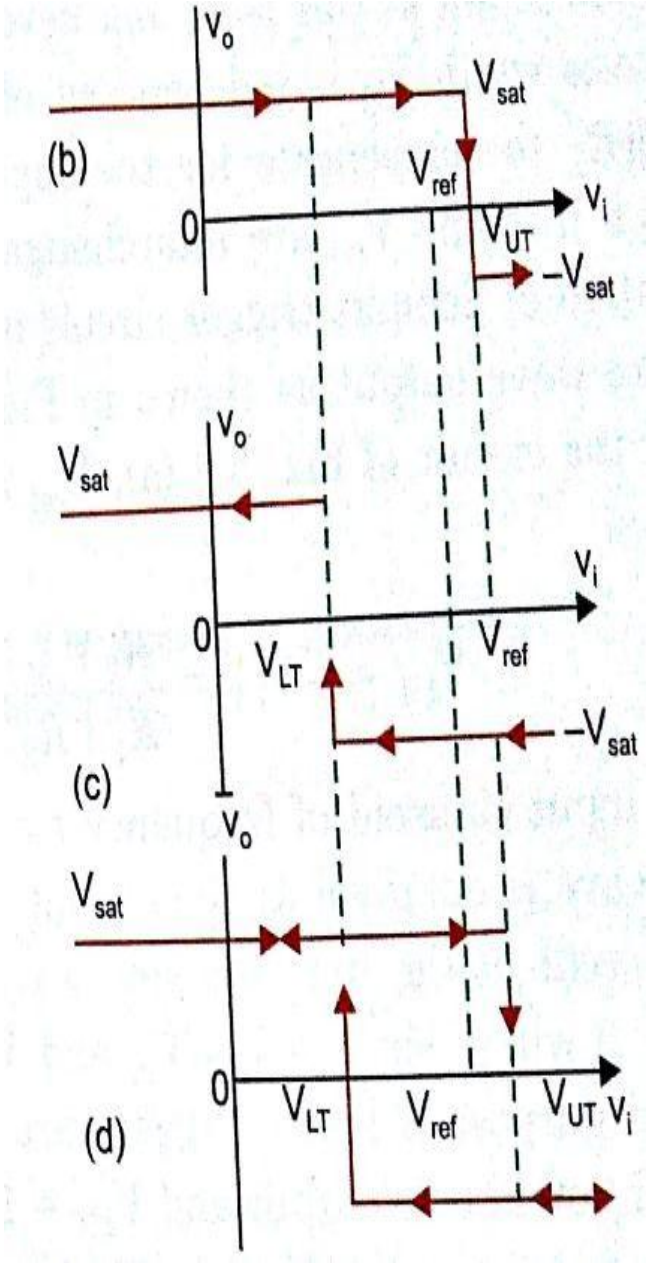
- This voltage is called upper threshold voltage V_{UT}. As long as v_i is less than V_{UT}, the output voltage v_o remains constant at $+V_{sat}$.
- When v_i is just greater than V_{UT}, the output regeneratively switches to $-V_{sat}$ and remains at this level as long as $v_i > V_{UT}$.



- Suppose the output $v_o = -V_{sat}$. The voltage at (+) input terminal can be obtained by using superposition.

$$V_{LT} = \frac{v_{ref} R_1}{R_1 + R_2} - \frac{R^2 V^{sat}}{R_1 + R_2}$$

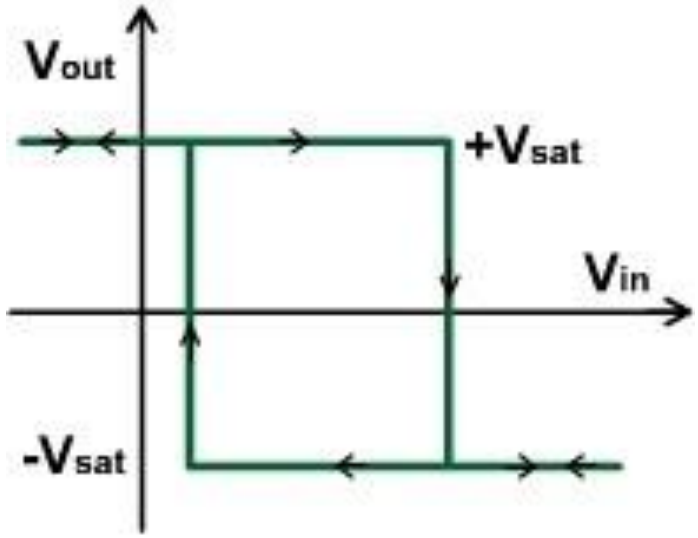
- This voltage is called lower threshold voltage V_{LT}. As long as v_i is greater than V_{LT}, the output voltage v_o remains constant at $-V_{sat}$.
- When v_i is just lesser than V_{LT}, the output regeneratively switches to $+V_{sat}$.

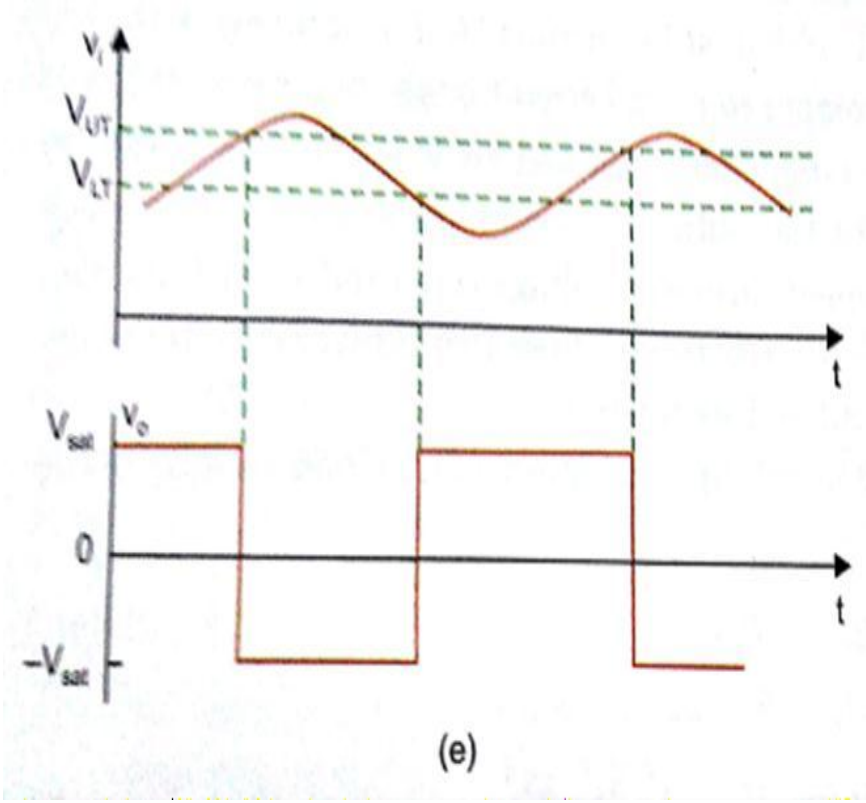


- Note that $V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis width V_H

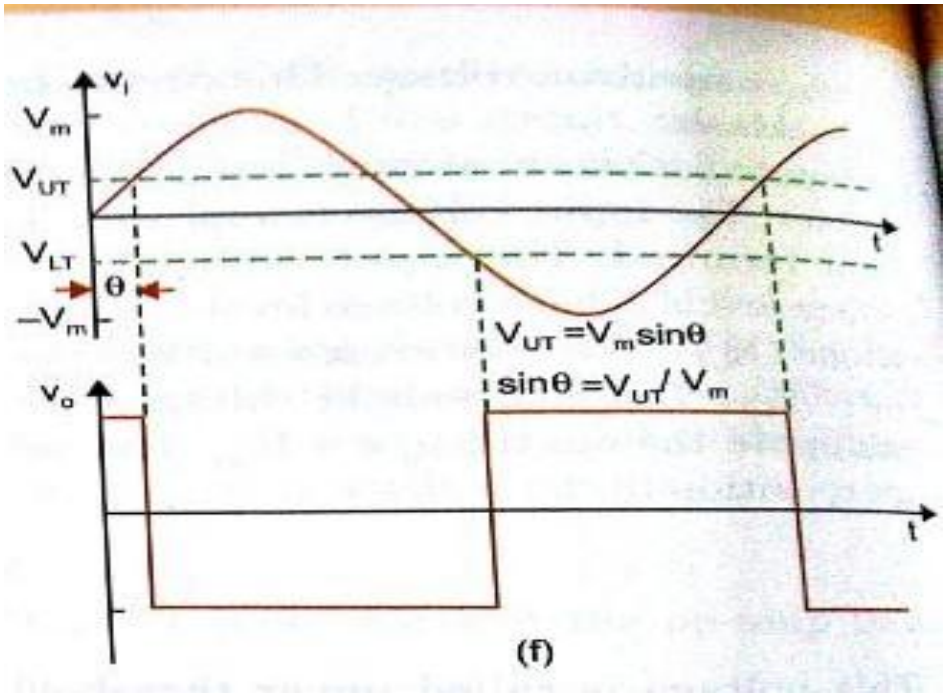
$$V_H = V_{UT} - V_{LT} = \frac{2R_2 V_{sat}}{R_1 + R_2}$$

- Because of the hysteresis, the circuit triggers at a higher voltage for increasing signals than for decreasing ones.
- v_i were smaller than V_H
- V_H is independent of V_{ref}
- The resistor R_3 is chosen equal to $R_1 || R_2$ to compensate for the input bias current




v_i
V_{UT}
V_{LT}
t
V_{sat}
v_o
0
t
$-V_{sat}$

(e)


v_i
V_m
V_{UT}
V_{LT}
θ
$-V_m$
t
$V_{UT} = V_m \sin\theta$
$\sin\theta = V_{UT} / V_m$
v_o
t

(f)

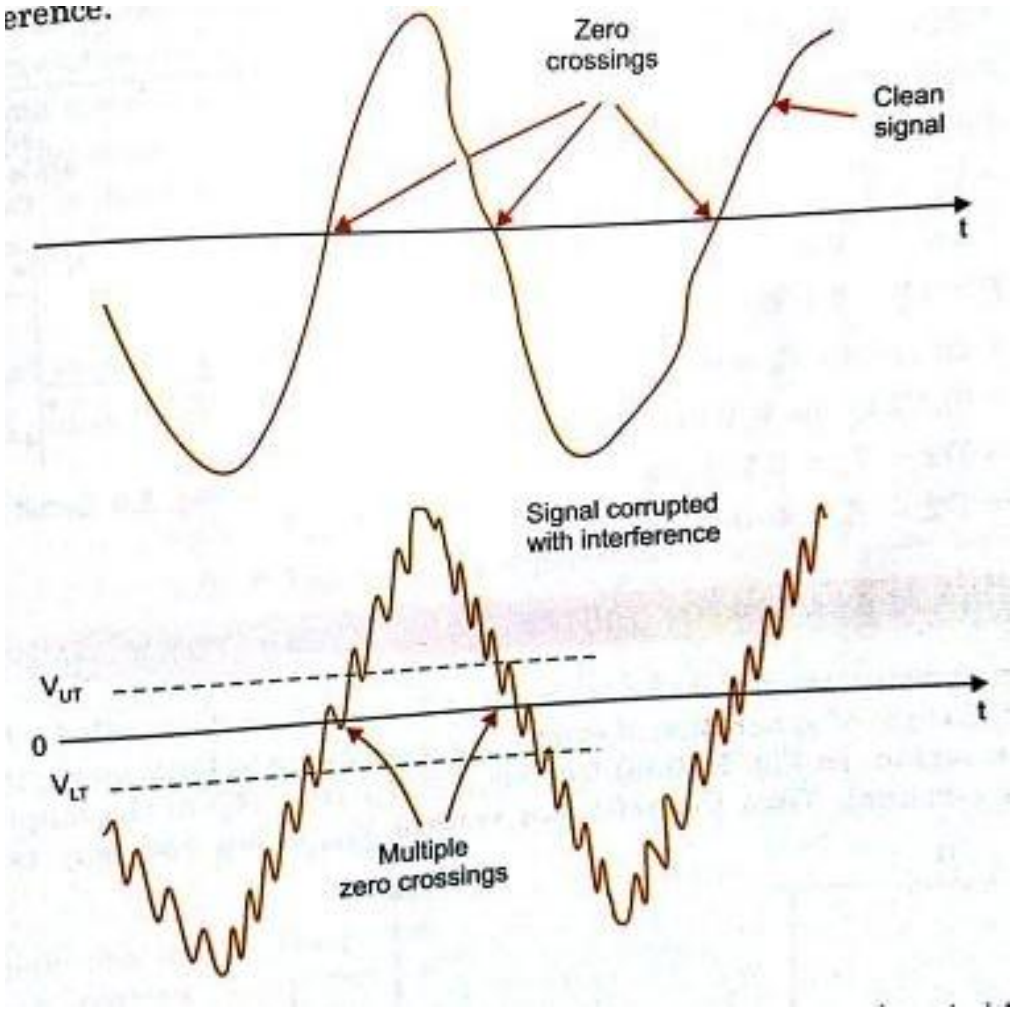
- A non inverting Schmitt trigger is obtained if v_i and V_{ref} are interchanged.
- If in the circuit V_{ref} is chosen as zero volt.

$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

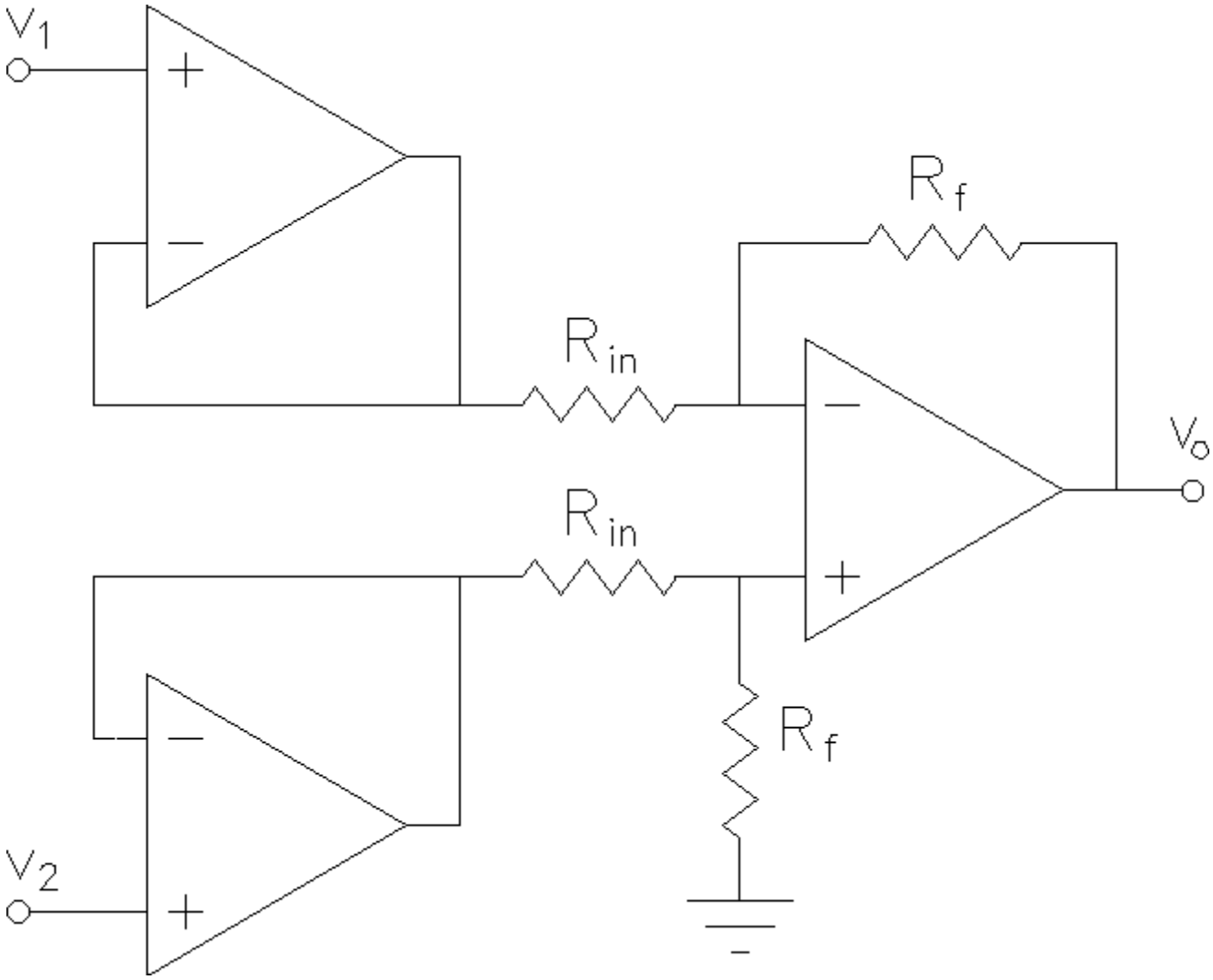
- If an input sinusoidal of frequency f=1/T is applied to such a comparator, a symmetrical square wave is obtained at the output.
- The vertical edge of the output waveform however, will not occur at the time the sine wave passes through zero but is shifted in phase by θ where $\sin\theta = {}^{V_U}_{T} \,/_{V_m}$ and Vm is the peak sinusoidal voltage.

Application

- Interesting application of hysteresis is in the detection and counting of the zero crossing of an arbitrary waveform



Instrumentation Amplifier



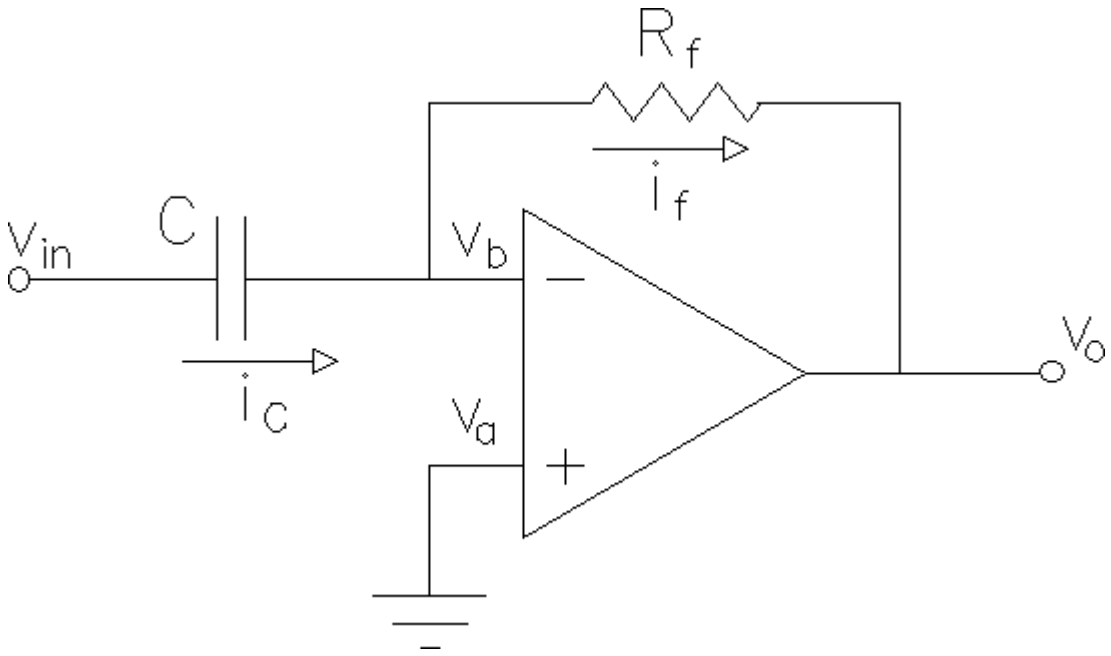
Instrumentation Amplifier

In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

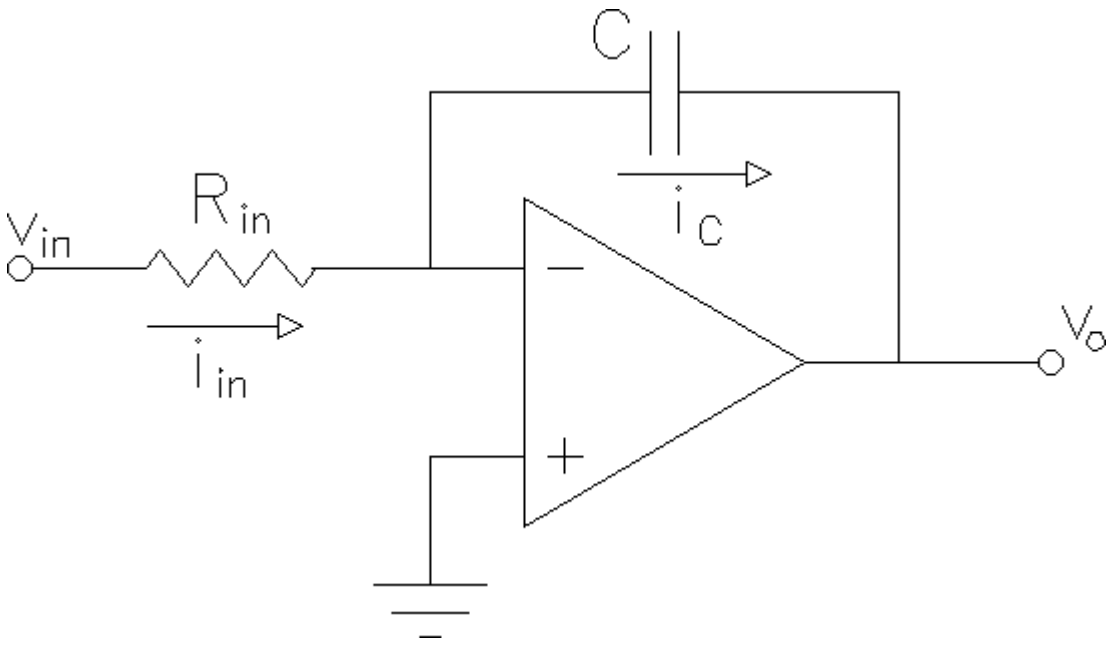
Features of instrumentation amplifier

1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature co-efficient
4. low dc offset
5. low output impedance

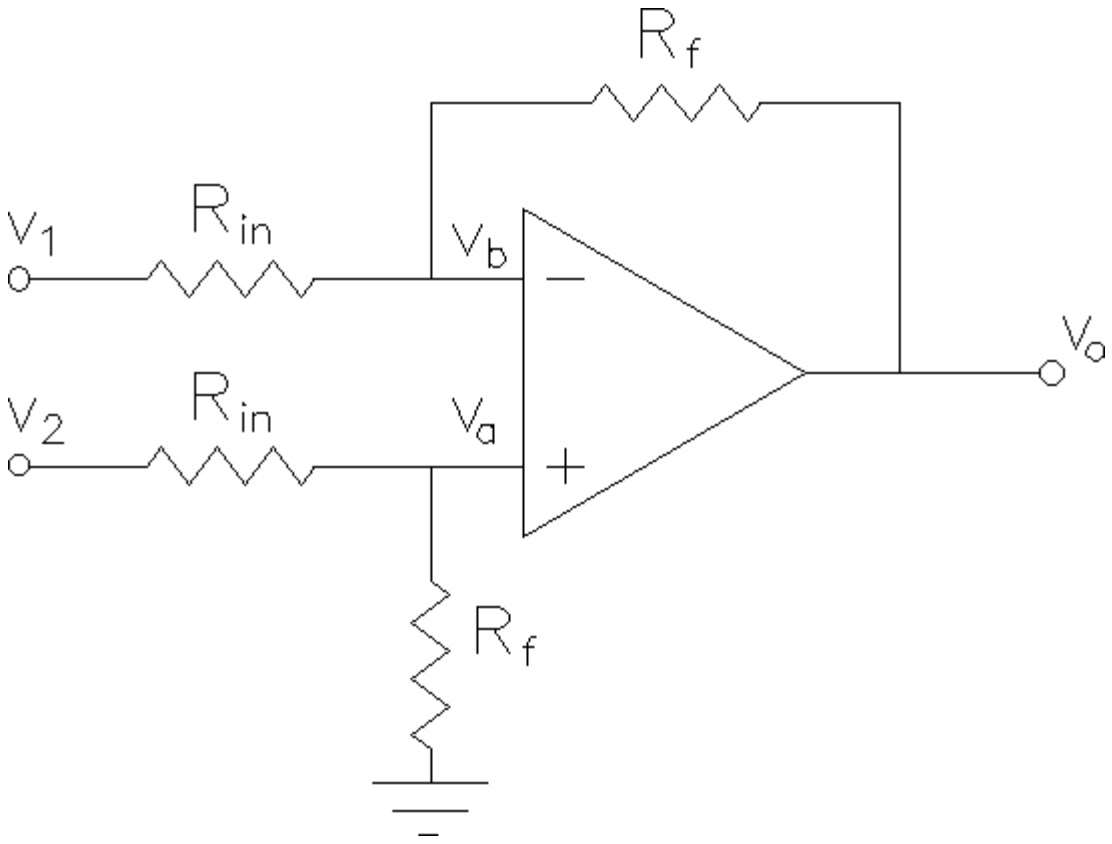
Differentiator



Integrator



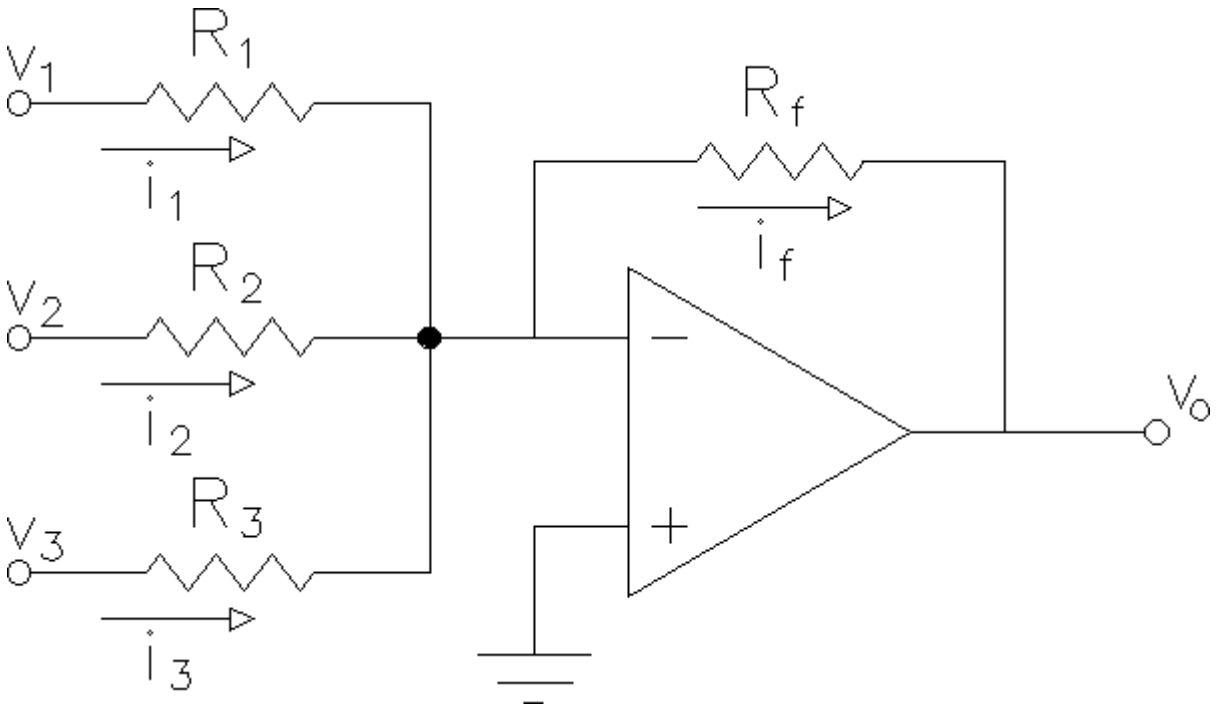
Differential amplifier



Differential amplifier

This circuit amplifies only the difference between the two inputs. In this circuit there are two resistors labeled R_{IN} Which means that their values are equal. The differential amplifier amplifies the difference of two inputs while the differentiator amplifies the slope of an input

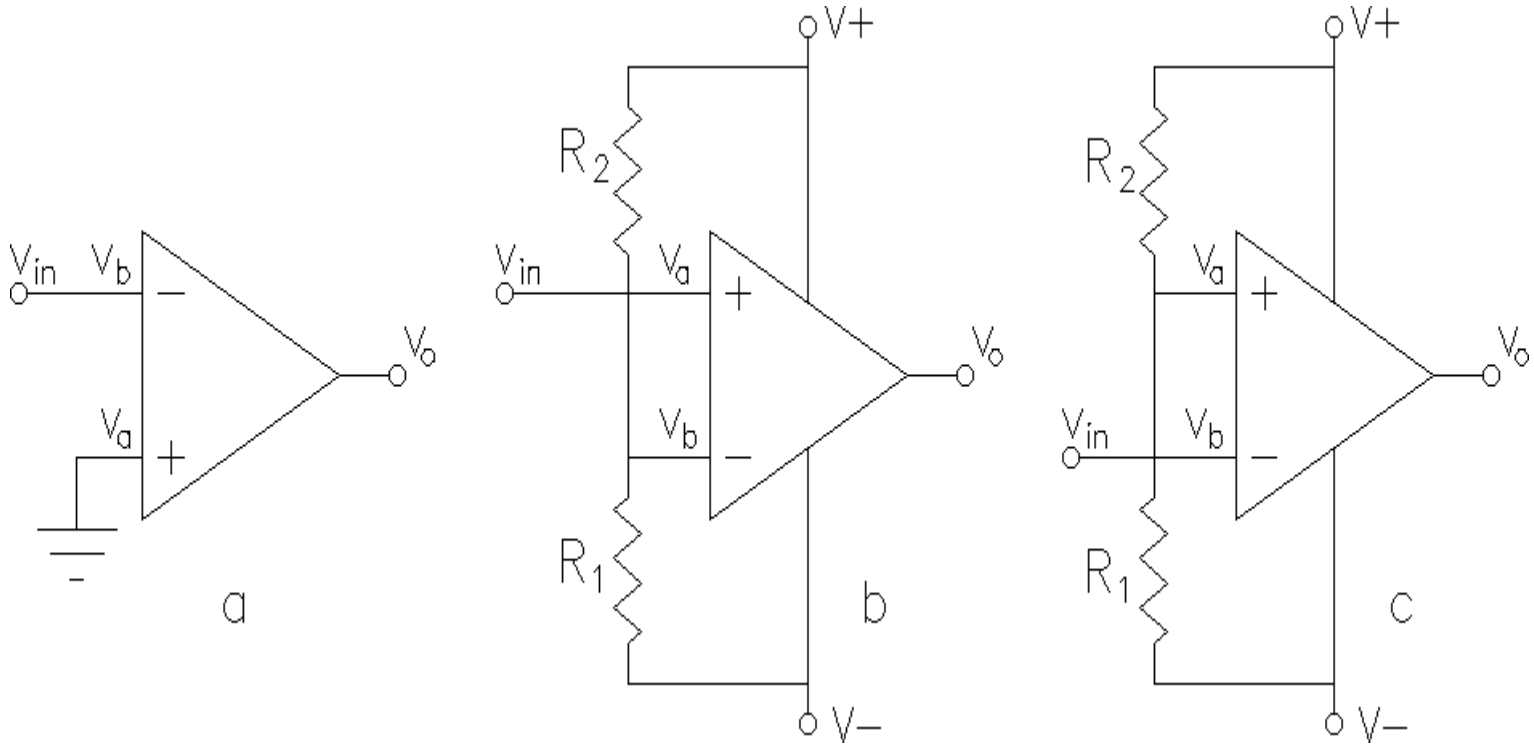
Summer



Comparator

A comparator is a circuit which compares a signal voltage applied at one input of an op- amp with a known reference voltage at the other input. It is an open loop op - amp with output + Vsat

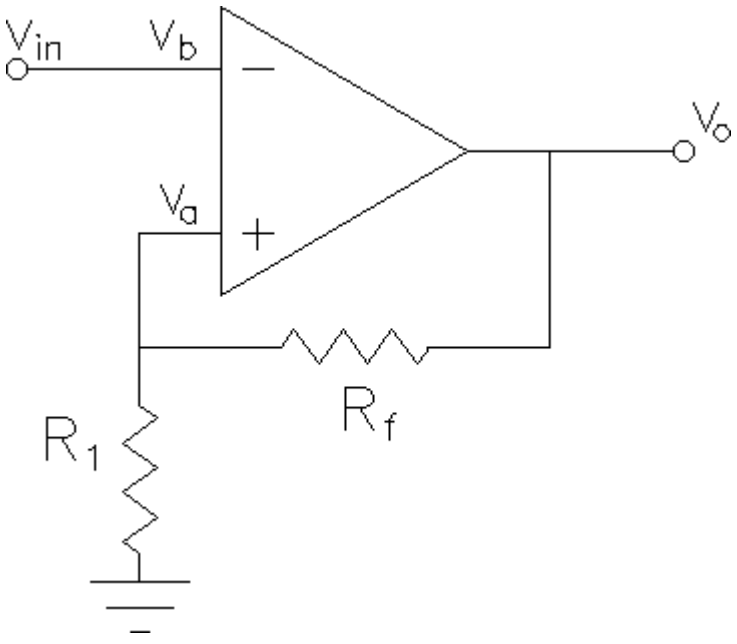
Comparator



Applications of comparator

1. Zero crossing detector
2. Window detector
3. Time marker generator
4. Phase detector

Schmitt trigger



Filter

Filter is a frequency selective circuit that passes signal of specified Band of frequencies and attenuates the signals of frequencies outside the band

Type of Filter

1. Passive filters
2. Active filters

Passive filters

Passive filters works well for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive.For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation

Active filters

Active filters used op- amp as the active element and resistors and capacitors as passive elements. By enclosing a capacitor in the feed back loop , inductor less active filters can be obtained

some commonly used active filters

1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter

Active Filters

- Active filters use op-amp(s) and RC components.
- Advantages over passive filters:
  - op-amp(s) provide gain and overcome circuit losses
  - increase input impedance to minimize circuit loading
  - higher output power
  - sharp cutoff characteristics can be produced simply and efficiently without bulky inductors
- Single-chip universal filters (e.g. switched-capacitor ones) are available that can be configured for any type of filter or response.

Review of Filter Types & Responses

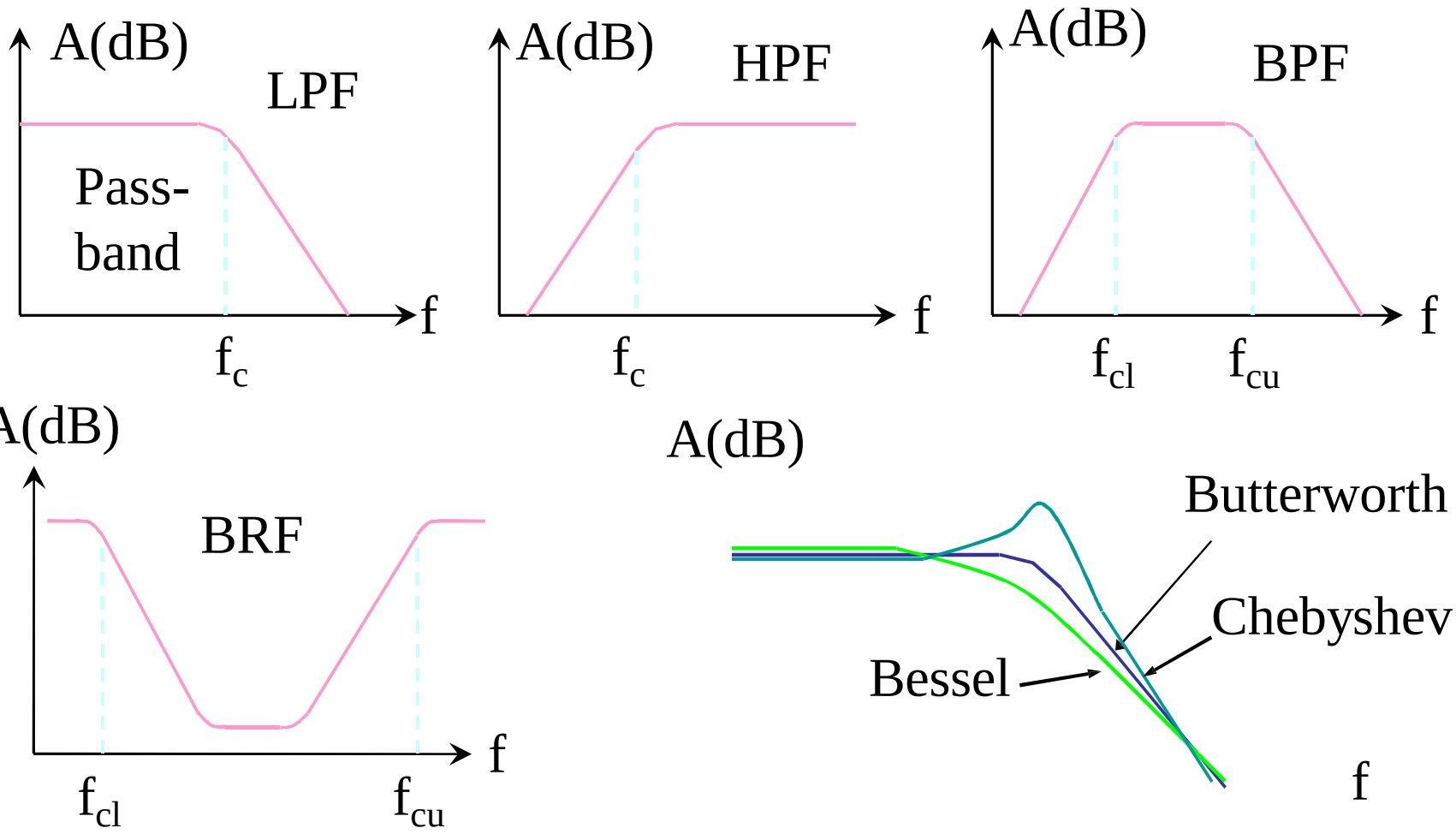
- 4 major types of filters: low-pass, high-pass, band pass, and band-reject or band-stop
- 0 dB attenuation in the pass band (usually)
- 3 dB attenuation at the *critical* or *cutoff frequency*, f_c (for Butterworth filter)
- Roll-off at 20 dB/dec (or 6 dB/oct) per *pole* outside the passband (# of poles = # of reactive elements). Attenuation at any frequency, f, is:

$$atten.(dB)\,at\ f = \log\left(\frac{f}{f_c}\right) x\, atten.(dB)\,at\ f_{dec}$$

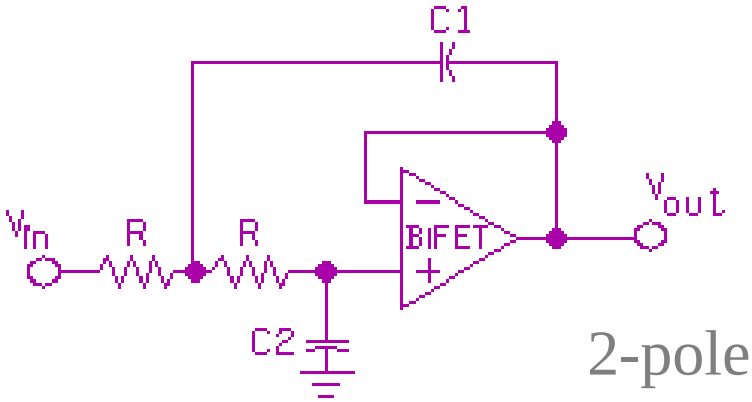
Review of Filters (cont'd)

- Bandwidth of a filter: BW = f_{cu} - f_{cl}
- Phase shift: 45^o/pole at f_c; 90^o/pole at >> f_c
- 4 types of filter responses are commonly used:
  - Butterworth - maximally flat in passband; highly non-linear phase response with frequency
  - Bessel - gentle roll-off; linear phase shift with freq.
  - Chebyshev - steep initial roll-off with ripples in passband
  - Cauer (or elliptic) - steepest roll-off of the four types but has ripples in the passband and in the stop band

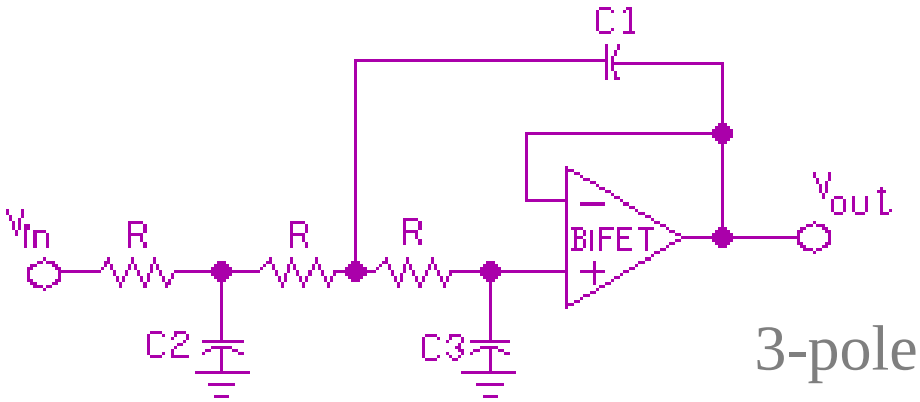
Frequency Response of Filters



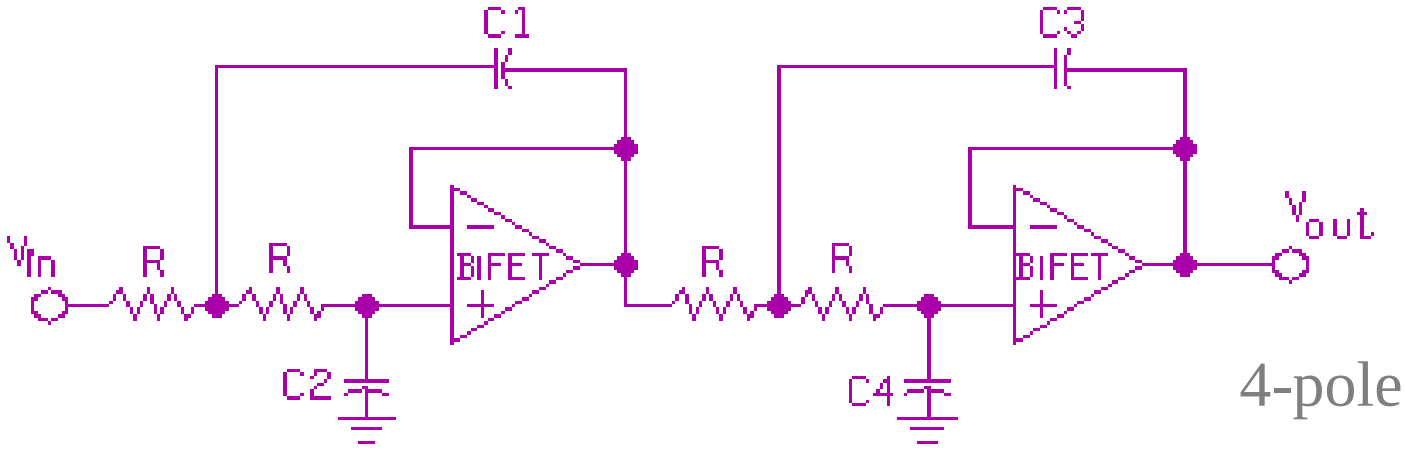
Unity-Gain Low-Pass Filter Circuits



2-pole



3-pole



4-pole

Design Procedure for Unity-Gain LPF

- Determine/select number of poles required.
- Calculate the frequency scaling constant, $K_f = 2\pi f$
- Divide normalized C values (from table) by K_f to obtain frequency-scaled C values.
- Select a desired value for one of the frequency-scaled C values and calculate the impedance scaling factor:

$$K_x = \frac{frequency - scaled\ C\ value}{desired\ C\ value}$$

  - Divide all frequency-scaled C values by K_x
  - Set $R = K_x\ \Omega$

An Example

Design a unity-gain LP Butterworth filter with a critical frequency of 5 kHz and an attenuation of at least 38 dB at 15 kHz.

The attenuation at 15 kHz is 38 dB

⑧ the attenuation at 1 decade (50 kHz) = 79.64 dB.

We require a filter with a roll-off of at least 4 poles.

K_f = 31,416 rad/s. Let's pick C_1 = 0.01 μF (or 10 nF). Then

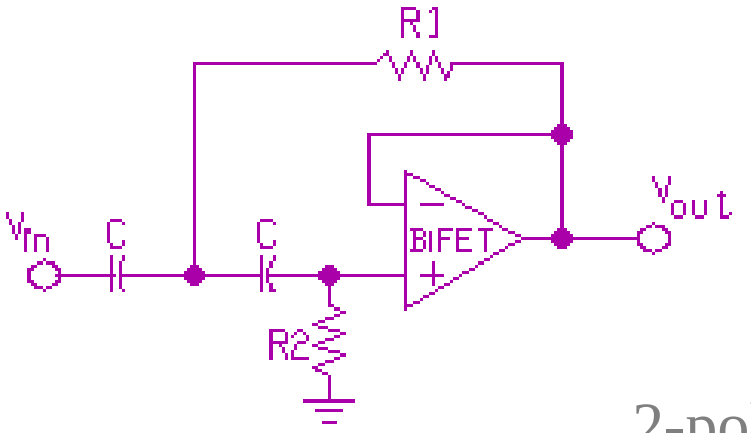
C_2 = 8.54 nF, C_3 = 24.15 nF, and C_4 = 3.53 nF.

Pick standard values of 8.2 nF, 22 nF, and 3.3 nF.

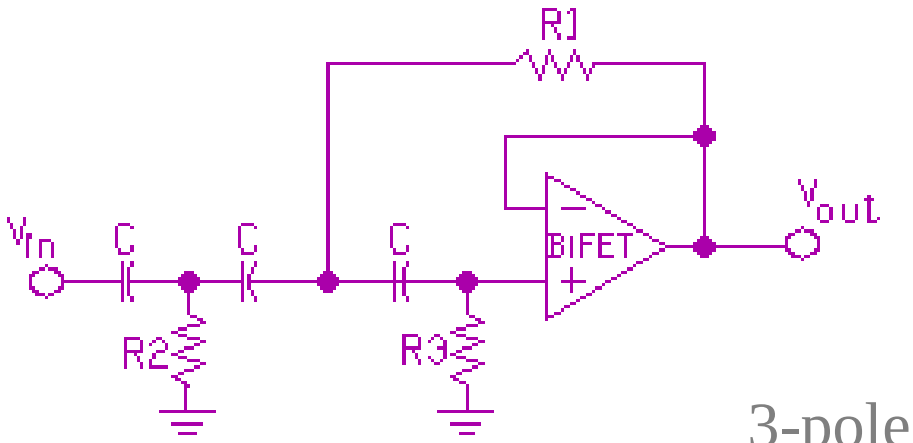
K_x = 3,444

Make all R = 3.6 kΩ (standard value)

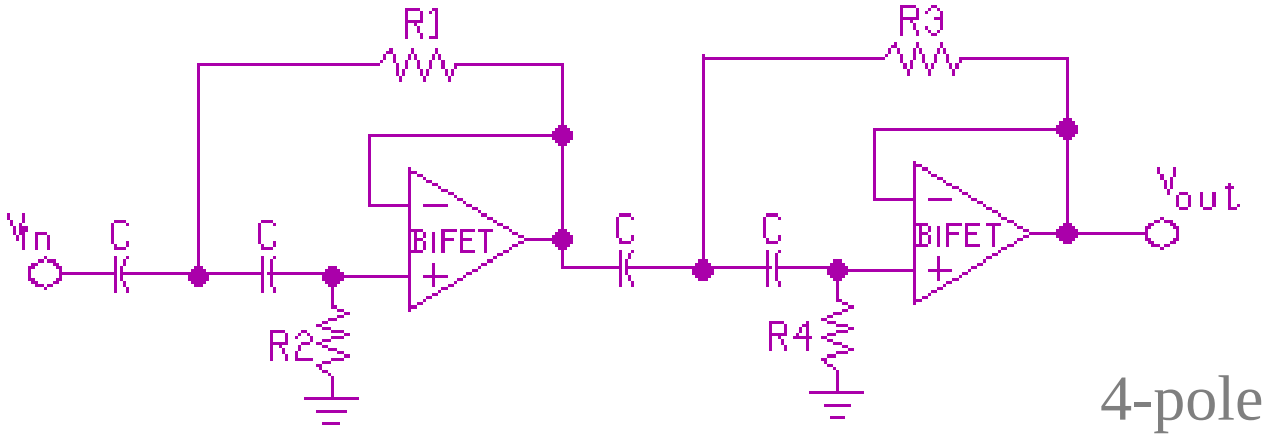
Unity-Gain High-Pass Filter Circuits



2-pole



3-pole



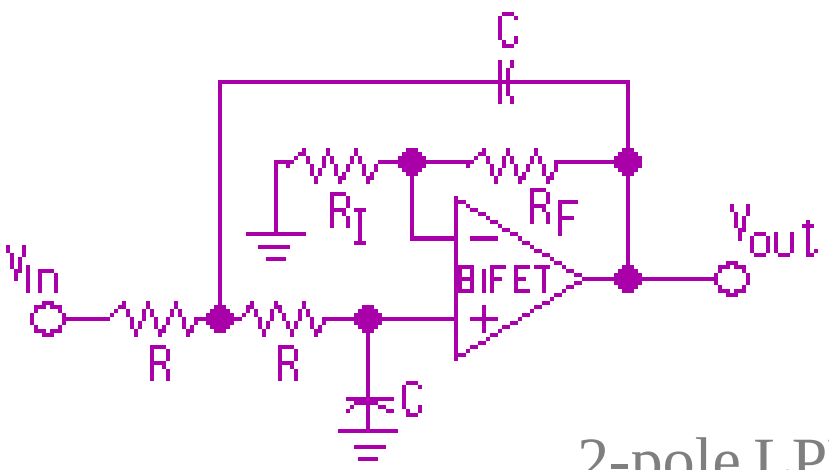
4-pole

Design Procedure for Unity-Gain HPF

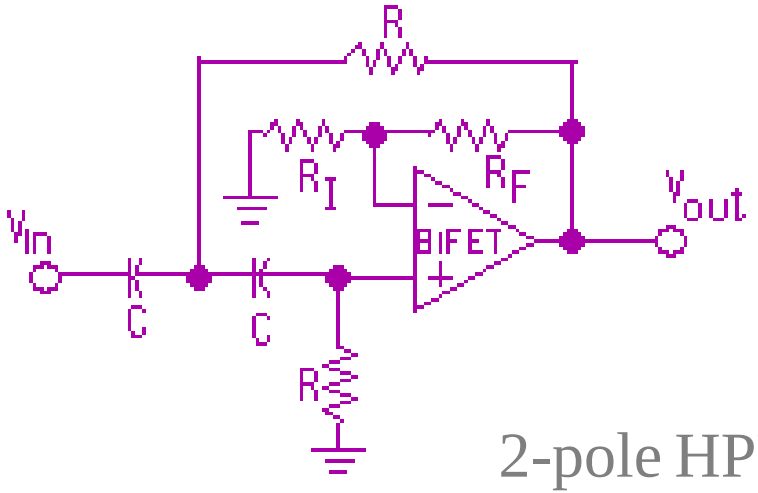
- The same procedure as for LP filters is used except for step #3, the normalized C value of 1 F is divided by K_f. Then pick a desired value for C, such as 0.001 μF to 0.1 μF, to calculate K_x. (Note that all capacitors have the same value).
- For step #6, multiply all normalized R values (from table) by K_x.

E.g. Design a unity-gain Butterworth HPF with a critical frequency of 1 kHz, and a roll-off of 55 dB/dec. (Ans.: C = 0.01 μF, R_1 = 4.49 kΩ, R_2 = 11.43 kΩ, R_3 = 78.64 kΩ.; pick standard values of 4.3 kΩ, 11 kΩ, and 75 kΩ).

Equal-Component Filter Design



2-pole LPF



2-pole HPF

Same value R & same value C are used in filter.

Select C (e.g. 0.01 μF), then:

$$R = \frac{1}{2\pi f_o C}$$

A_v for # of poles is given in a table and is the same for LP and HP filter design.

$$A_v = \frac{R_F}{R_I} + 1$$

Example

Design an equal-component LPF with a critical frequency of 3 kHz and a roll-off of 20 dB/oct.

Minimum # of poles = 4

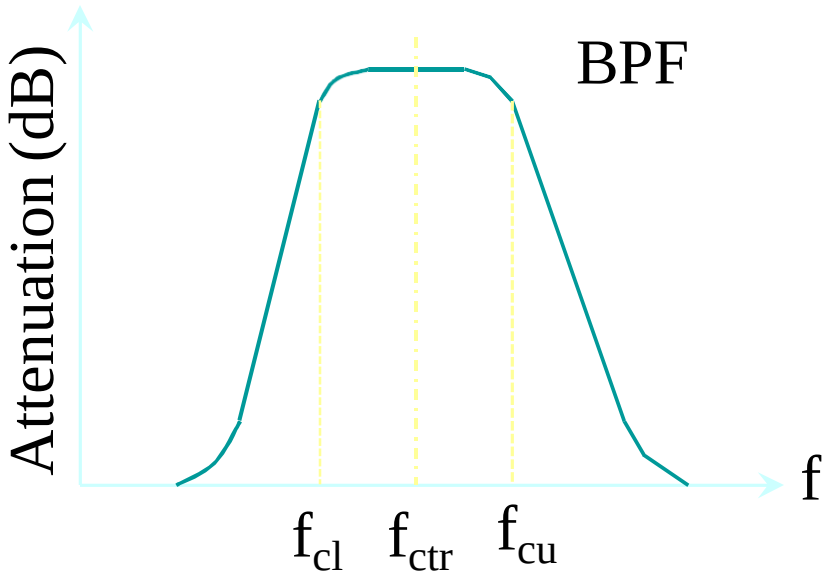
Choose C = 0.01 μF; ⑧ R = 5.3 kΩ

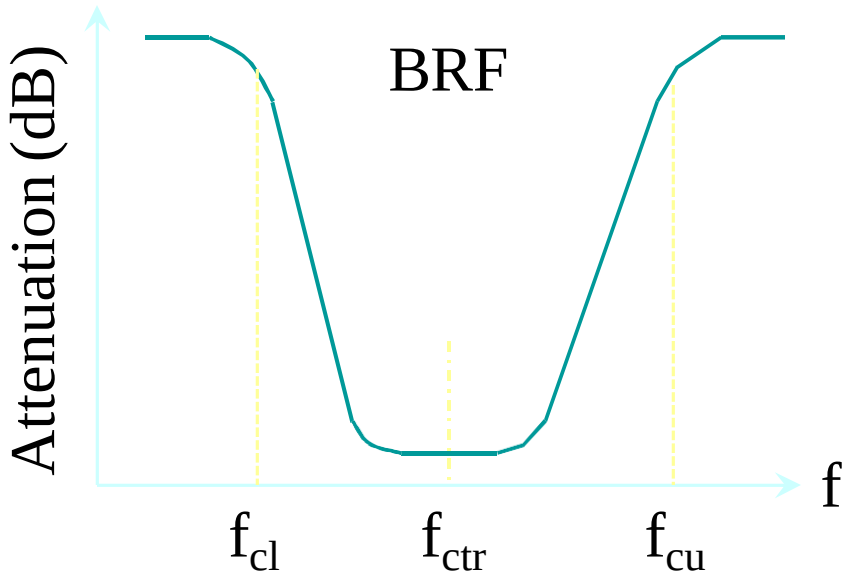
From table, A_{v1} = 1.1523, and A_{v2} = 2.2346.

Choose $R_{I1} = R_{I2}$ = 10 kΩ; then R_{F1} = 1.5 kΩ, and R_{F2} = 12.3 kΩ .

Select standard values: 5.1 kΩ, 1.5 kΩ, and 12 kΩ.

Bandpass and Band-Rejection Filter





The quality factor, Q, of a filter is given by:

$$Q = \frac{f_{ctr}}{BW}$$

where BW = $f_{cu} - f_{cl}$ and

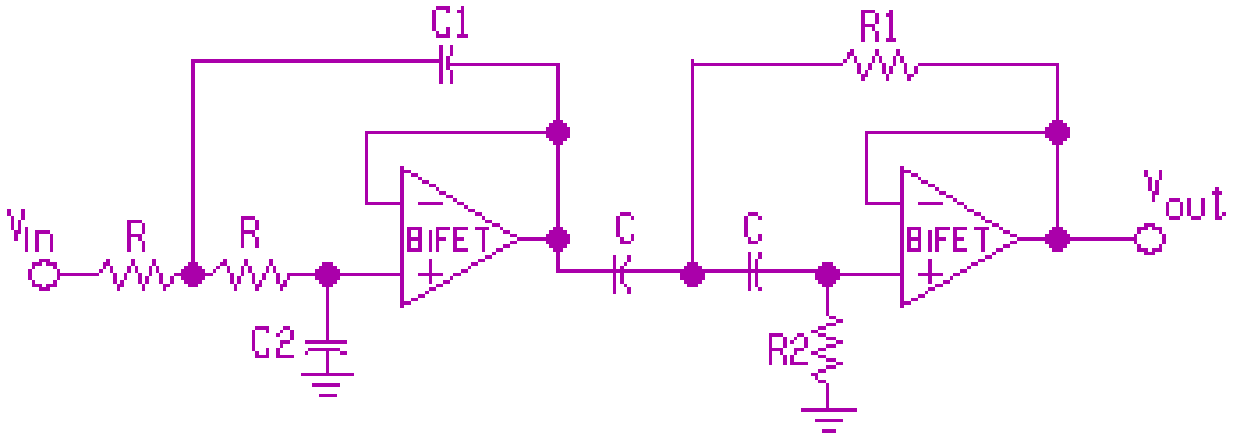
$$f_{ctr} = \sqrt{f_{cu} f_{cl}}$$

More On Bandpass Filter

If BW and f_{centre} are given, then:

$$f_{cl} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} - \frac{BW}{2}\,;\; f_{cu} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} + \frac{BW}{2}$$

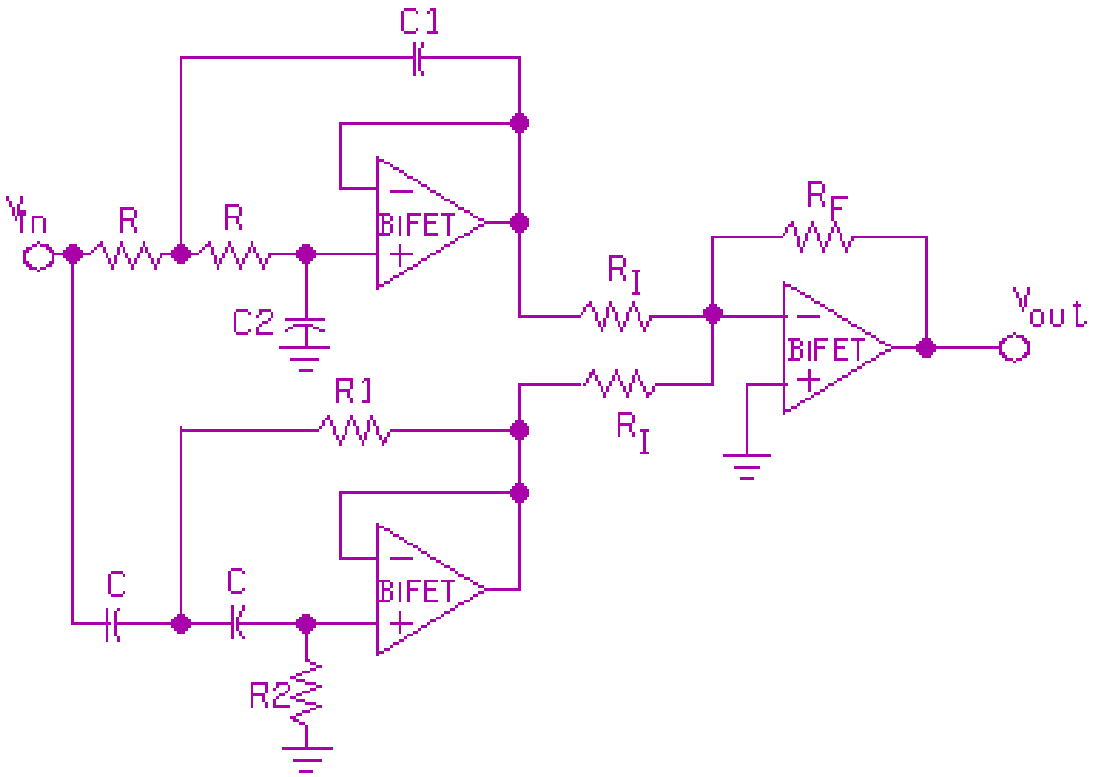
A *broadband* BPF can be obtained by combining a LPF and a HPF:



The Q of this filter is usually > 1.

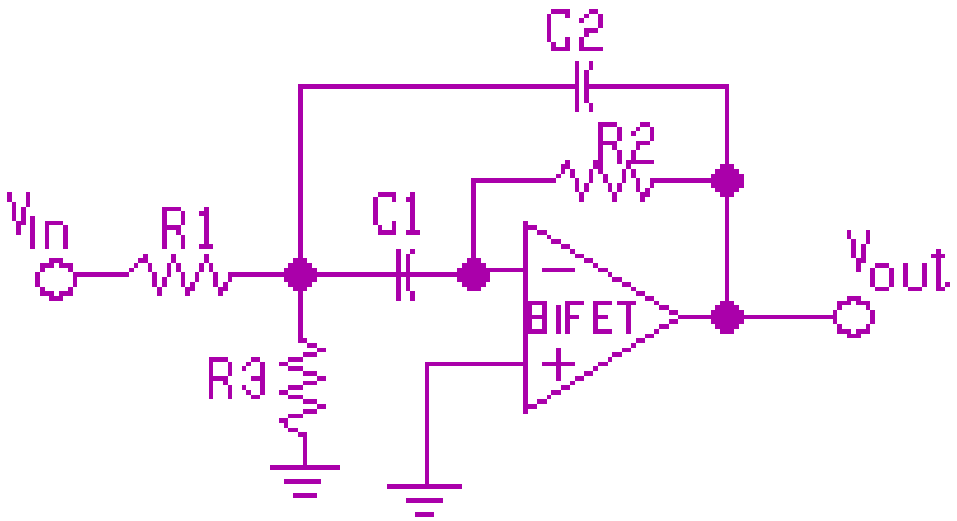
Broadband Band-Reject Filter

A LPF and a HPF can also be combined to give a broadband BRF:



2-pole band-reject filter

Narrow-band Bandpass Filter



$$BW = \frac{f_{ctr}}{Q} = \frac{1}{2\pi R_1 C}$$

$C1 = C2 = C$

$R_2 = 2\,R_1$

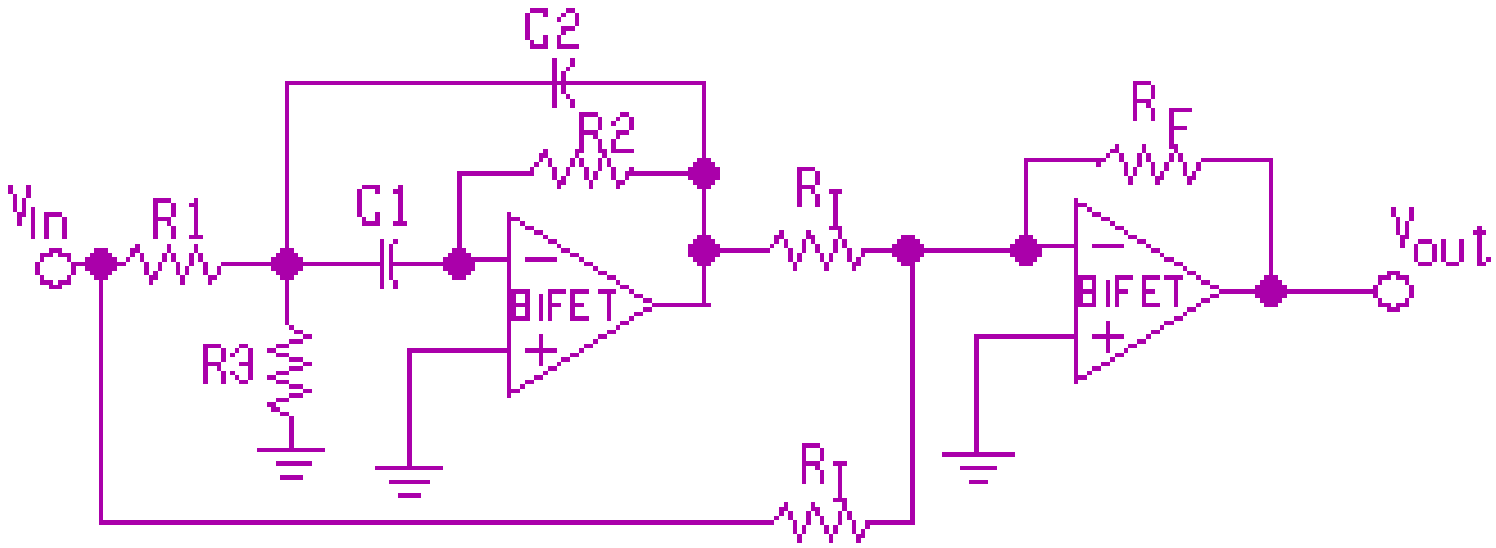
$$R_3 = \frac{R_1}{2Q^2 - 1}$$

$$f_{ctr} = \frac{1}{2\sqrt{2}\pi R_1 C}\sqrt{1 + \frac{R_1}{R_3}}$$

R_3 can be adjusted or trimmed to change f_{ctr} without affecting the BW. Note that $Q < 1$.

Narrow-band Band-Reject Filter

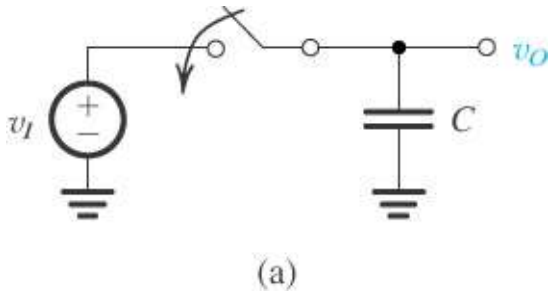
Easily obtained by combining the inverting output of a narrow-band BRF and the original signal:



The equations for R1, R2, R3, C1, and C2 are the same as before.
$R_I = R_F$ for unity gain and is often chosen to be >> R1.

UNIT 4 ADC /DAC

Because digital integrated circuits are economical and accurate, it is convenient to process signals in digital form, for example, to perform algebraic manipulations, to transmit or store signals.



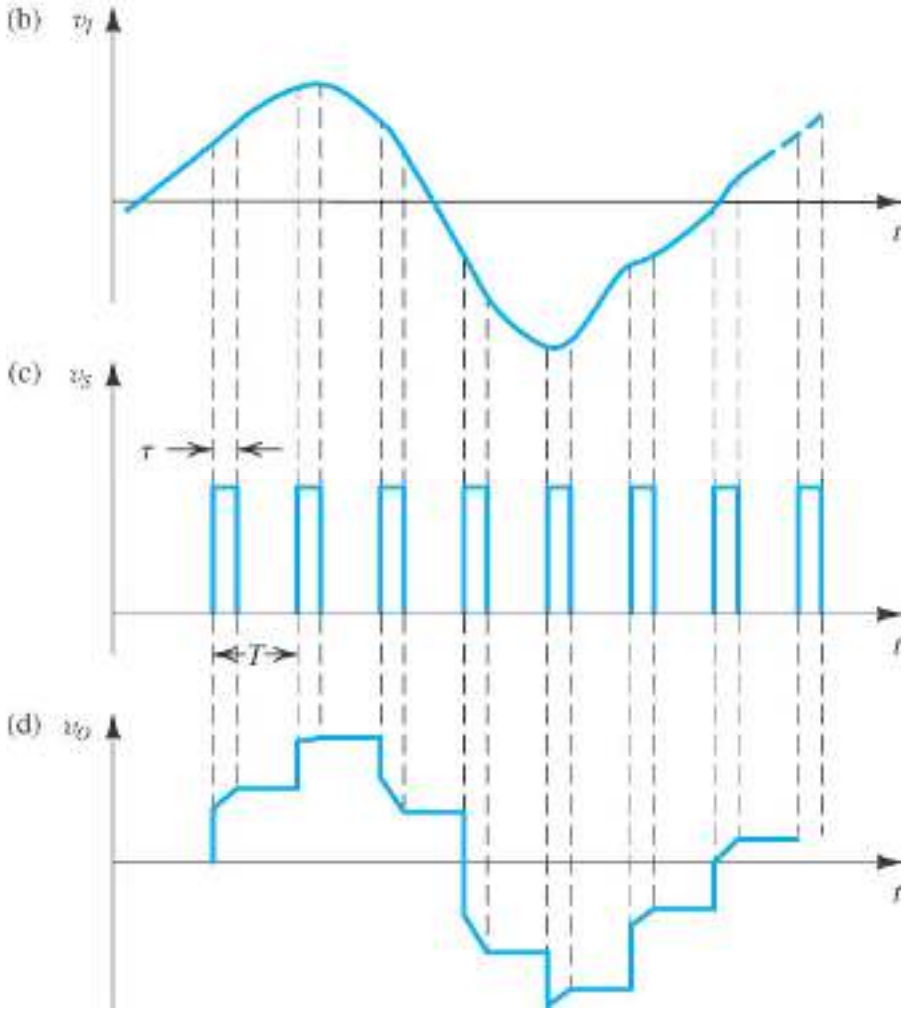


Figure 9.36 The process of periodically sampling an analog signal. **(a)** Sample-and-hold (S/H) circuit. The switch closes for a small part (τ seconds) of every clock period (T). **(b)** Input signal waveform. **(c)** Sampling signal (control signal for the switch). **(d)** Output signal (to be fed to A/D converter).

Analog-to-Digital (A/D) and Digital-to-Analog (D/A) Converters as Functional Blocks

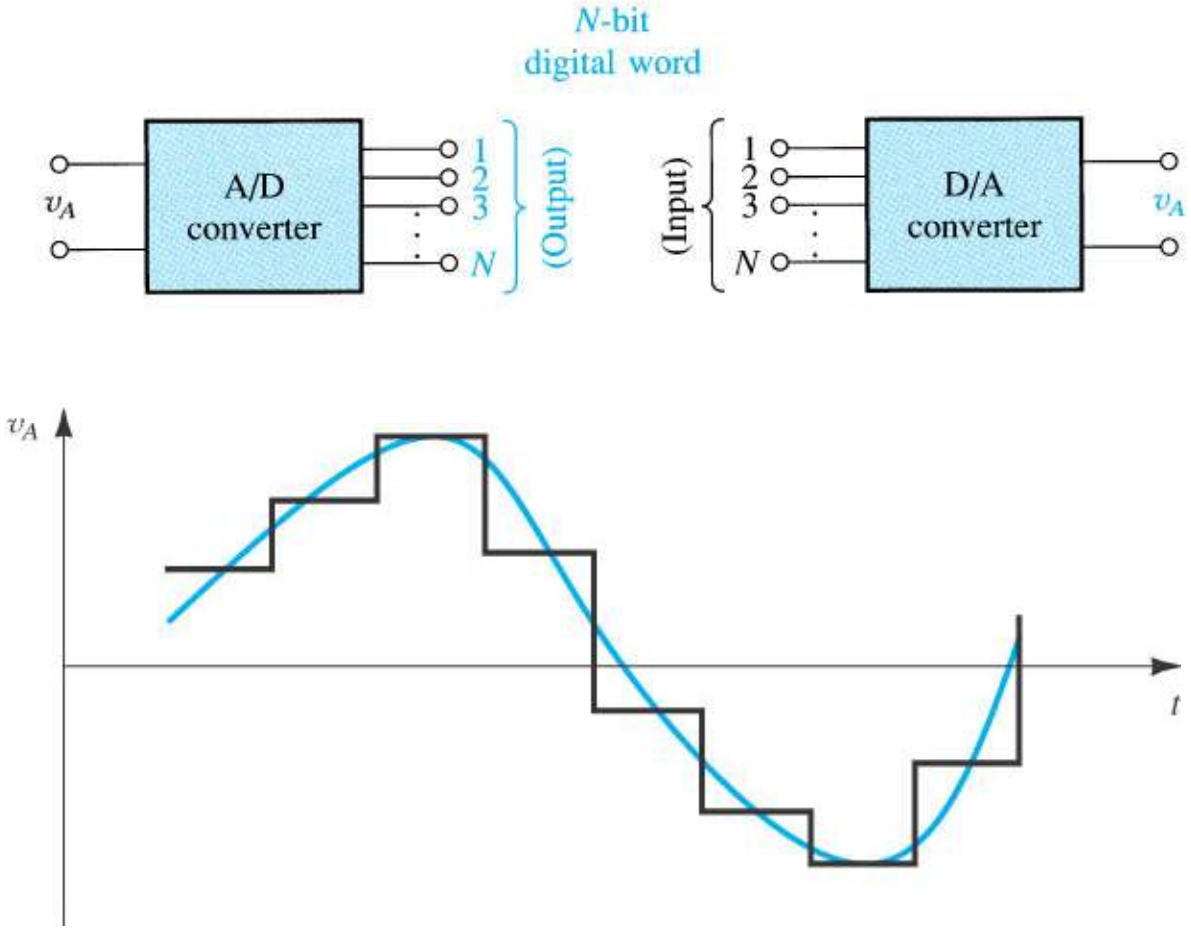
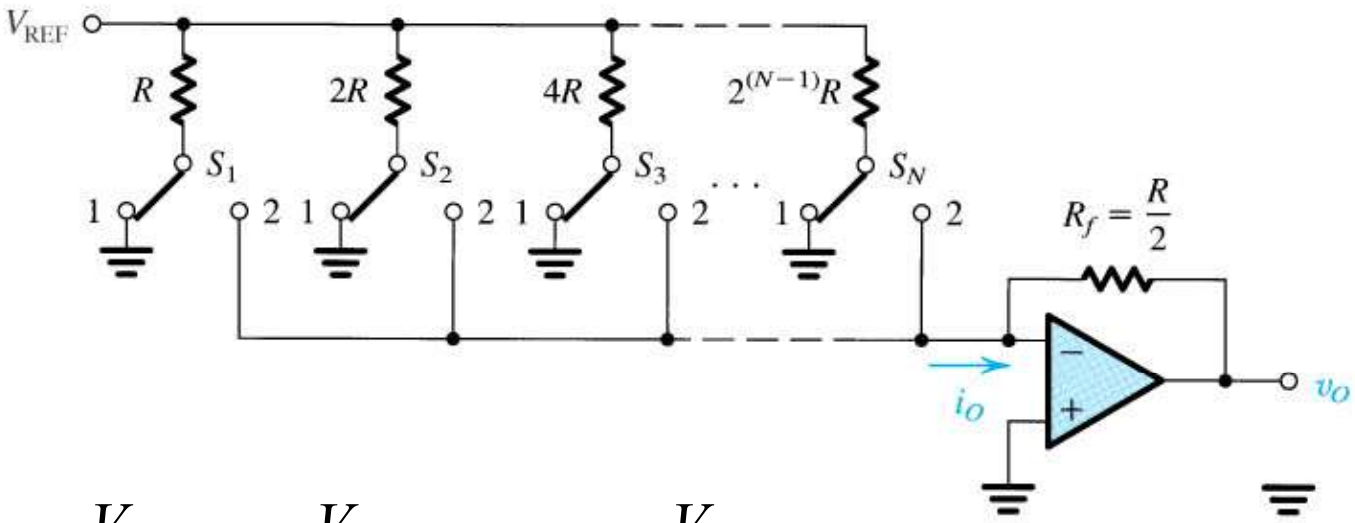


Figure 9.37 The A/D and D/A converters as circuit blocks.

D/A Converter Circuits

- **Binary-weighted registers**

$b_1 b_2 \ldots b_N$



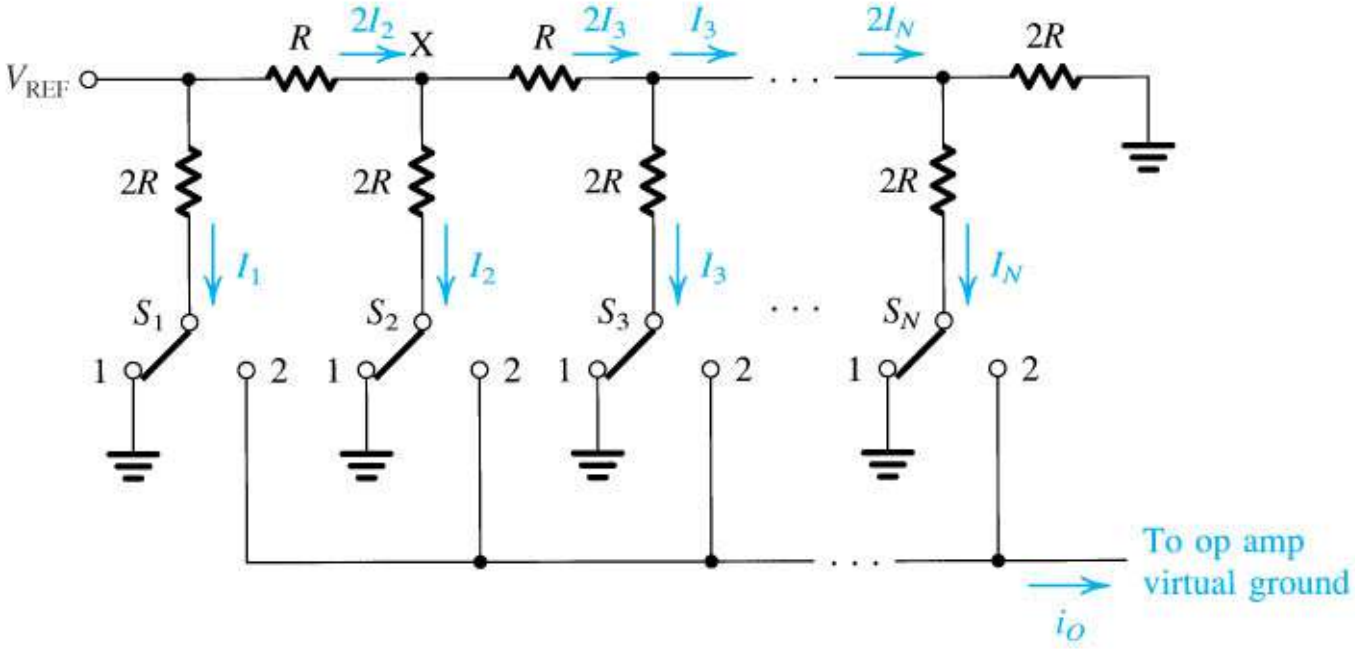
$$i_O = \frac{V_{\text{REF}}}{R} b_1 + \frac{V_{\text{REF}}}{2R} b_2 + \ldots + \frac{V_{\text{REF}}}{2^{N-1}R} b_N$$

$$v_O = -i_O R_f$$

Figure 9.39 An *N*-bit D/A converter using a binary-weighted resistive ladder network.

- ***R*-2*R* ladders**

$b_1 b_2 \ldots b_N$



$$i_O = \frac{V_{\text{REF}}}{R} D$$

Figure 9.40 The basic circuit configuration of a DAC utilizing an *R*-2*R* ladder network.

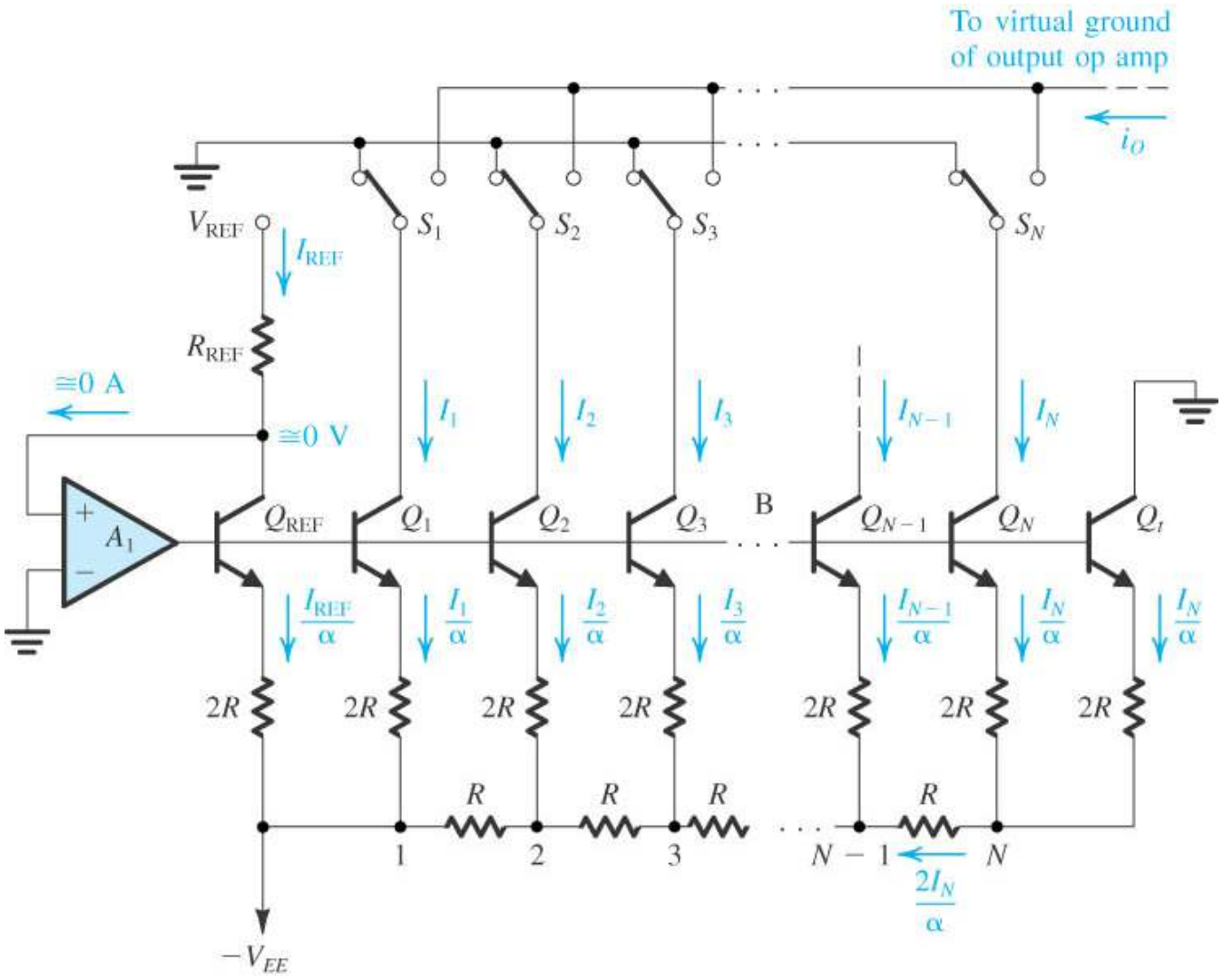


Figure 9.41 A practical circuit implementation of a DAC utilizing an *R*-2*R* ladder network.

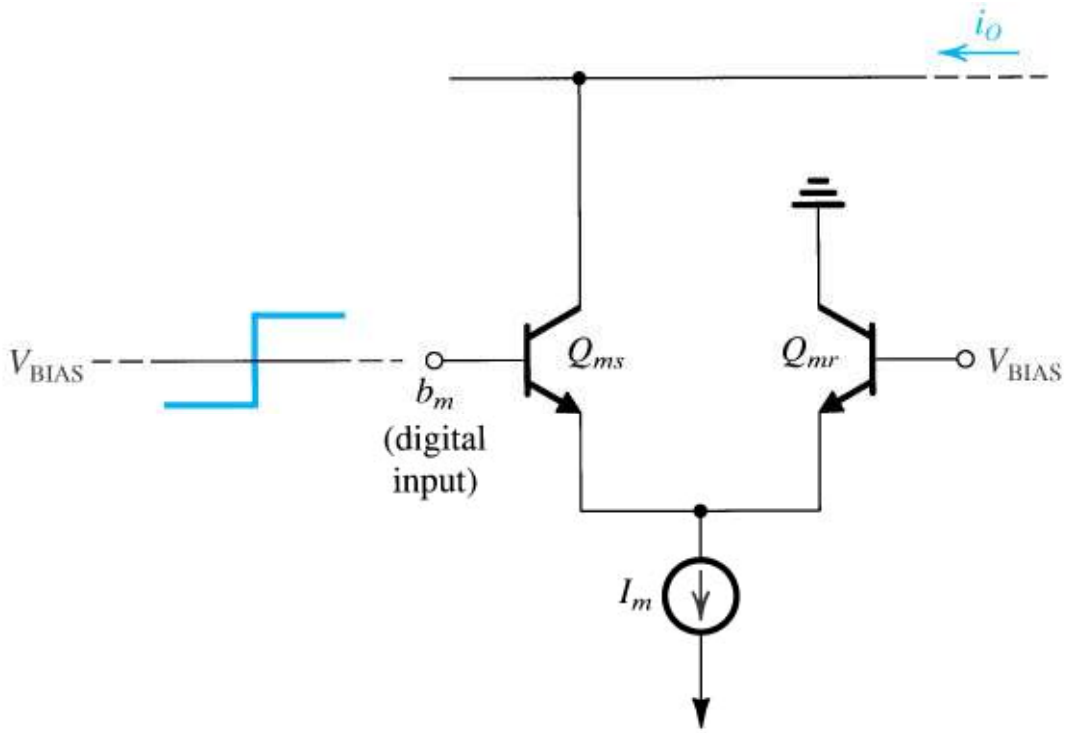


Figure 9.42 Circuit implementation of switch S_m in the DAC of Fig. 9.41. In a BiCMOS technology, Q_{ms} and Q_{mr} can be implemented using MOSFETs, thus avoiding the inaccuracy caused by the base current of BJTs.

A/D Converter Circuits

- **Feedback-type converter**

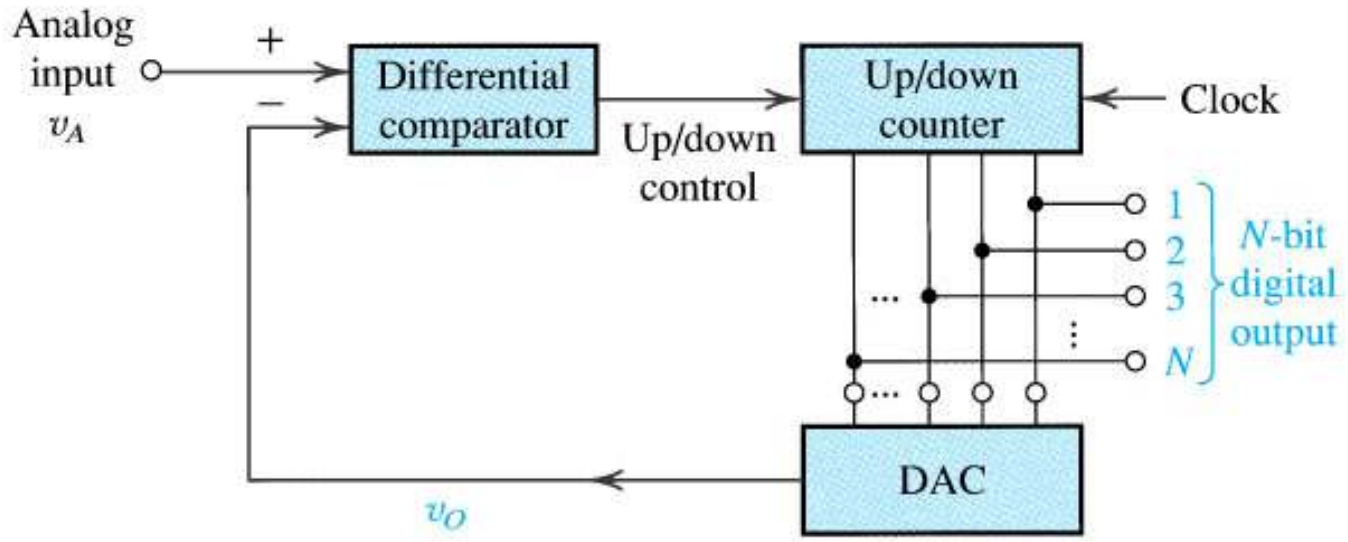
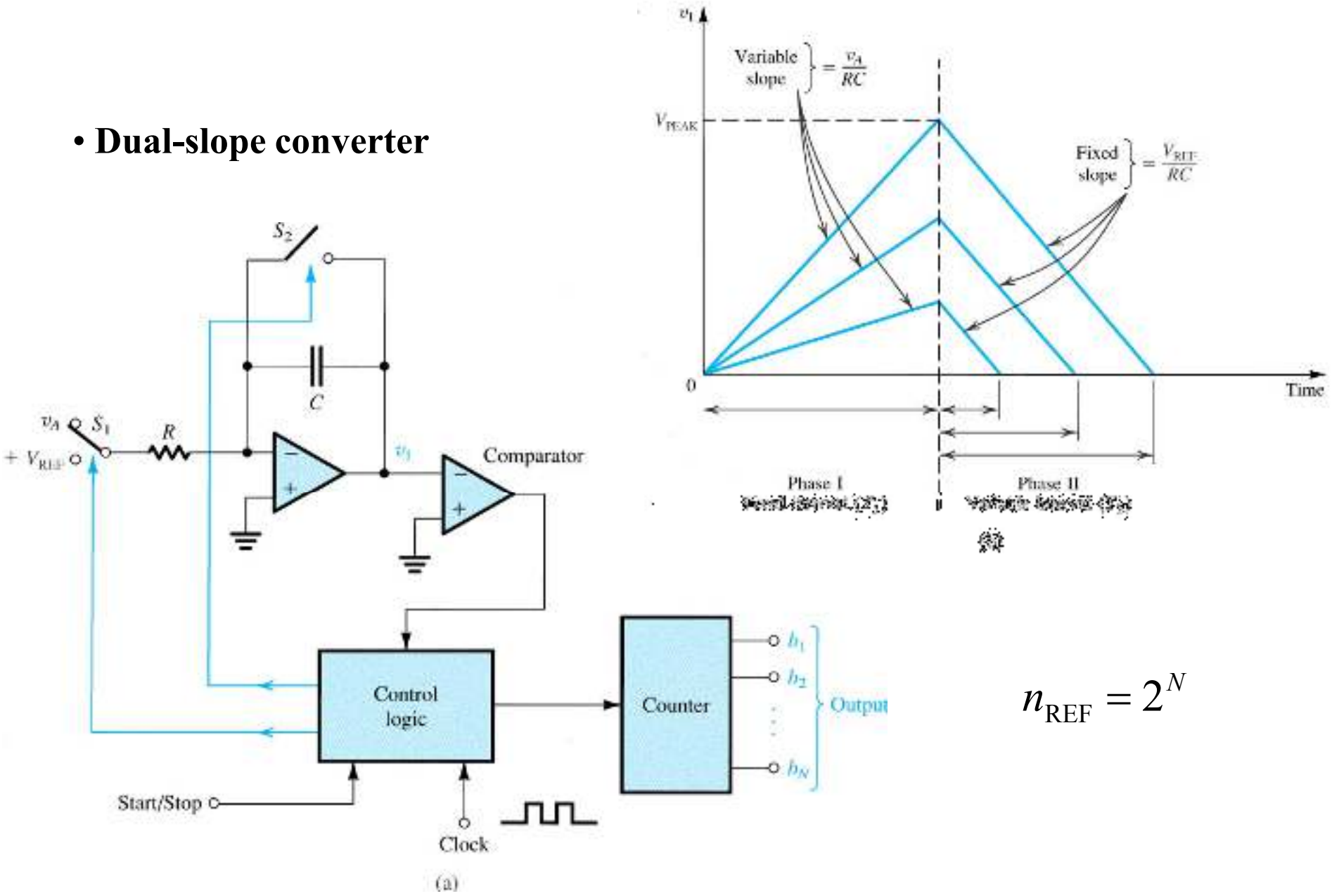


Figure 9.43 A simple feedback-type A/D converter.

- **Dual-slope converter**



$$n_{\text{REF}} = 2^N$$

Figure 9.44 The dual-slope A/D conversion method. Note that v_A is assumed to be negative.

- **Parallel converter**

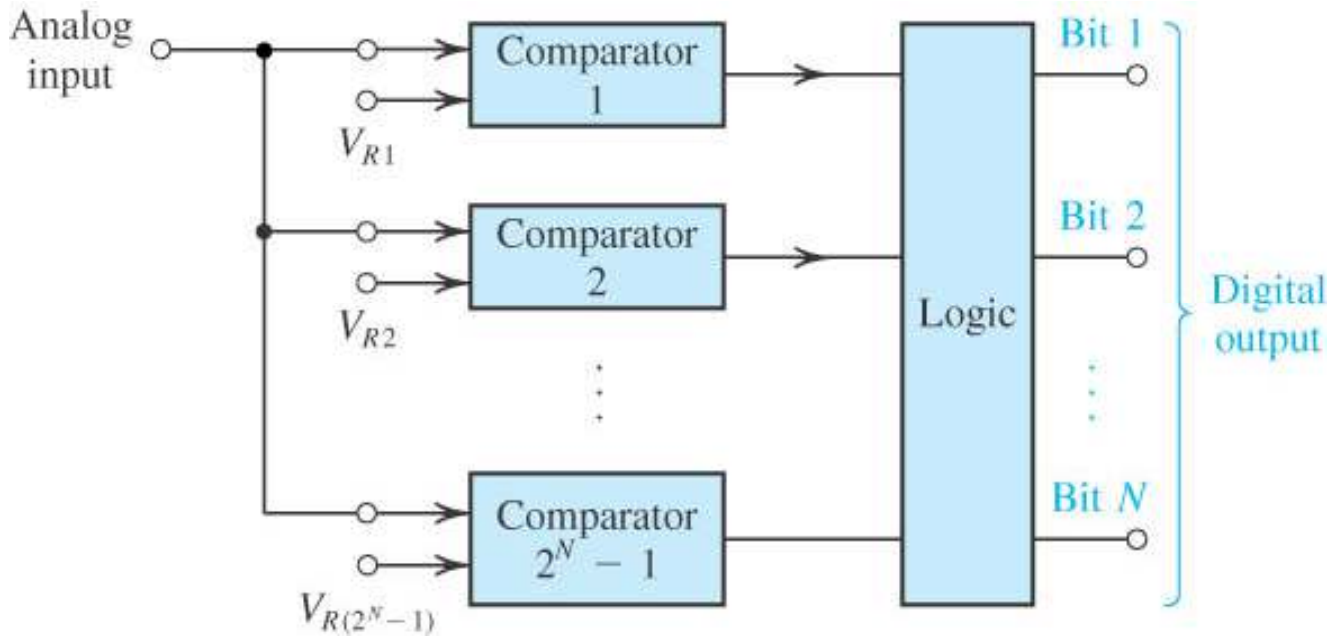


Figure 9.45 Parallel, simultaneous, or flash A/D conversion.

- **Charge-redistribution converter**

a) Sample phase

b) Hold phase

c) Redistribution phase

$$Q = 2C\,v_A$$

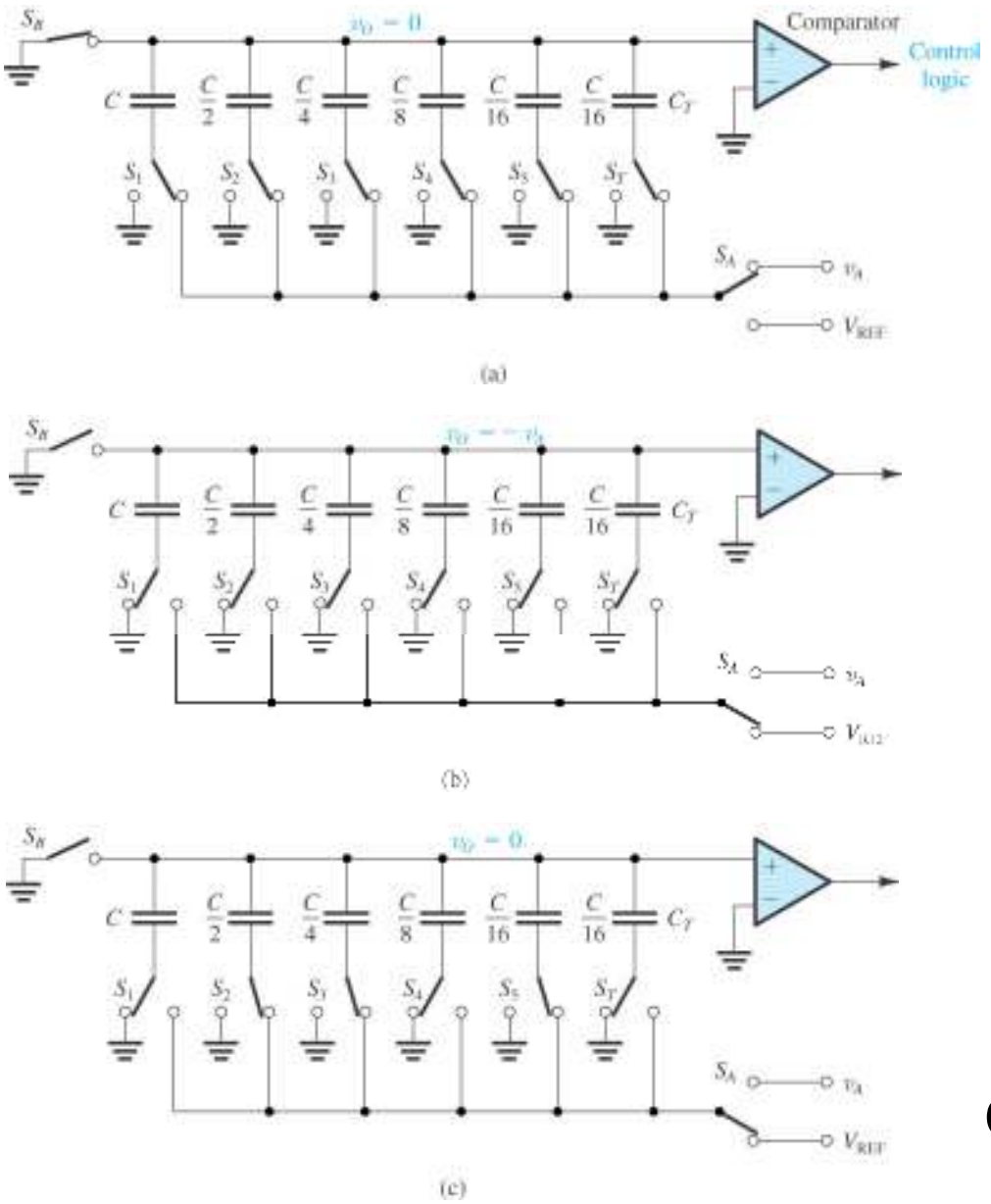


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Figure 9.46 Charge-redistribution A/D converter suitable for CMOS implementation: **(a)** sample phase, **(b)** hold phase, and **(c)** charge-redistribution phase.