

# **ELECTRONIC DEVICES AND CIRCUITS**

## Unit-1

# PN Junction Diode & Special Function Electronic Devices

# Atomic Structure

An atom is composed of :

- Nucleus ( which contains positively charged protons and neutral neutrons)
- Electrons (which are négative charged and that orbit the nucleus)

# Valence Electrons

- Electrons are distributed in various shells at different distances from nucleus
- Electron energy increases as shell radius increases.
- Electrons in the outer most Shell are called as valence electrons
- Elements in the period table are grouped according to the number of valence electrons.

# Valence Electrons

**Table 1.1** A portion of the periodic table

III	IV	V
B	C	
Al	Si	P
Ga	Ge	As

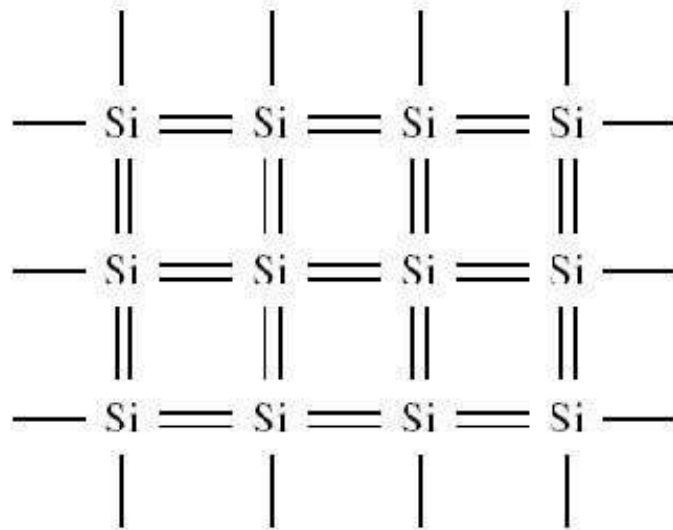
# Elemental/Compound Semiconductor

- Silicon (Si) and Germanium (Ge) are in group IV, and are **elemental semiconductors**
- Gallium arsenide (GaAs) is a group III-V **compound semiconductor**

# Silicon Crystal

- → At 0°K, each electron is in its lowest possible energy state, and each covalent bonding position is filled.
- → If a small electric field is applied, the electrons will not move → silicon is an **insulator**

# Silicon Atom Diagram at 0°K



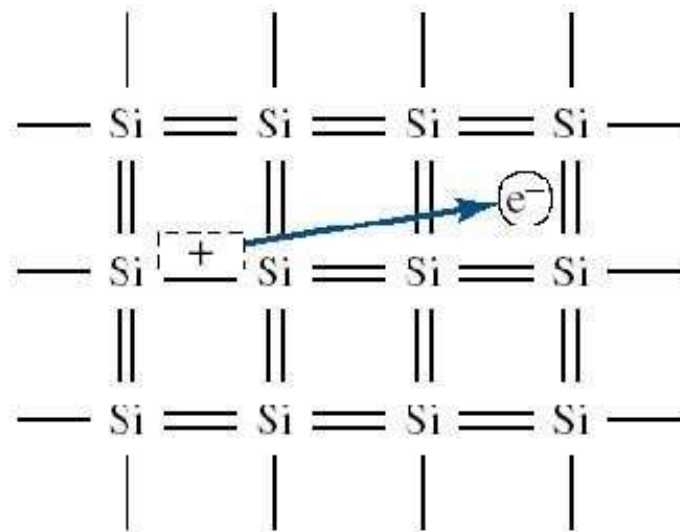
Two-dimensional  
representation of the silicon  
crystal at  $T = 0^\circ\text{K}$



# Intrinsic Silicon

- → If the temperature increases, the valence electrons will gain some thermal energy, and breaks free from the covalent bond → It leaves a positively charged hole
- → In order to break from the covalent bond, a valence electron must gain a minimum energy ***E<sub>g</sub>***:  
**Bandgap energy**

# Silicon Atom Diagram at Ambient Temp



The breaking of  
a covalent bond for  $T > 0^\circ\text{K}$

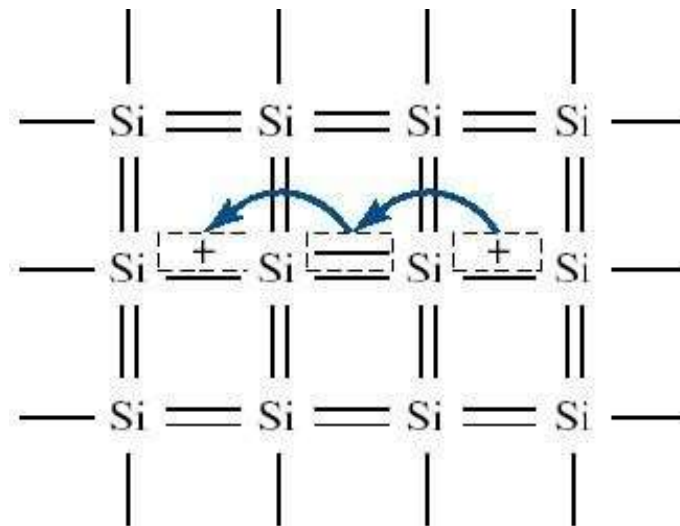
# Insulators/Conductors

- Materials that have large bandgap energies (in the range of 3 to 6 electron-volts (eV)) are **insulators**, because at room temperature, essentially no free electron exists in the material
- Materials that contain very large number of free electrons at room temperature are **conductors**

# Semiconductors

- In a semiconductor, the bandgap energy is in the order of 1 eV. The net flow of free electrons causes a current.
- In a semiconductor, two types of charged particles contribute to the current: the negatively charged electrons and the positively charged holes

# Movement of Holes



A two- dimensional  
representation of  
the silicon crystal showing the  
movement of the positively  
charged hole

# Semiconductor Constants

- The concentration of electrons and holes directly influence the magnitude of the current
- In an intrinsic semiconductor (a single crystal semiconductor) the densities of holes and electrons are equal.

$n_i$ : intrinsic carrier concentration for free electrons (same for holes)

$$n_i = BT^{3/2} e^{\left(\frac{-E_g}{2kT}\right)}$$

B: constant related to specific semiconductor material

$E_g$ : Bandgap energy (eV)

T: Temperature (°K)

K: Boltzman Constant (86 E-06 eV/°K)

# Semiconductor Constants

Semiconductor constants

Material	$E_g$ (eV)	$B$ (cm <sup>-3</sup> °K <sup>-3/2</sup> )
Silicon (Si)	1.1	$5.23 \times 10^{15}$
Gallium arsenide (GaAs)	1.4	$2.10 \times 10^{14}$
Germanium (Ge)	0.66	$1.66 \times 10^{15}$



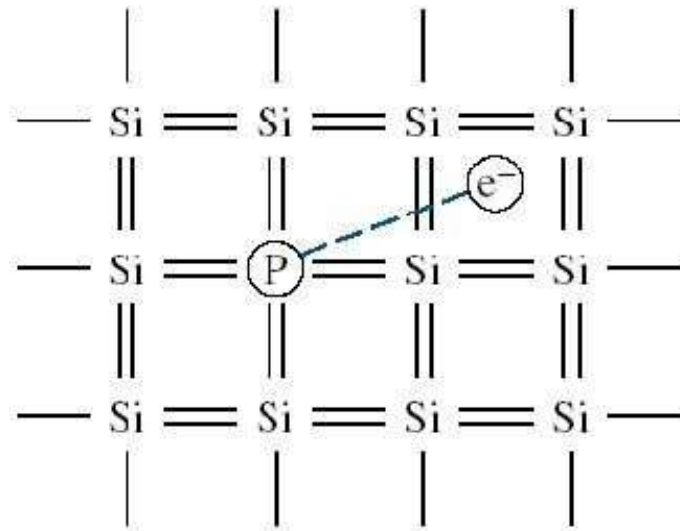
# Extrinsic Semiconductor / Doping

- The electron or hole concentration can be greatly increased by adding controlled amounts of certain impurities
- For silicon, it is desirable to use impurities from the group III and V.
- An N-type semiconductor can be created by adding phosphorus or arsenic

# Extrinsic Semiconductor / Doping

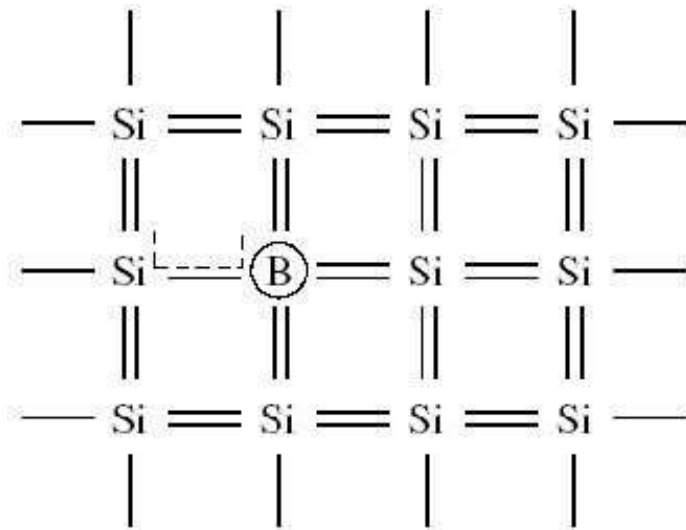
- The phosphorus (group **V**) atom is called **donor impurity** because it donates an electron that is free to move
- The boron (group **III**) has accepted a valence electron (or donated a hole), it is therefore called **acceptor impurity**

# N-Type Semiconductor



Two-dimensional  
representation of a silicon  
lattice doped with a  
phosphorus atom

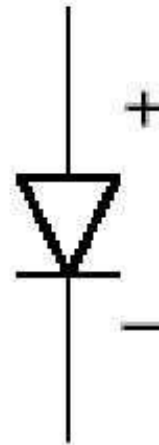
# P-Type Semiconductor



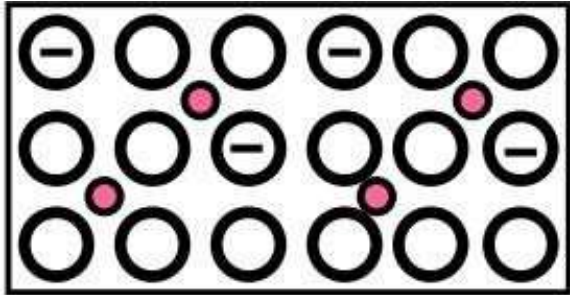
Two-dimensional  
representation of a silicon  
lattice doped with a boron  
atom

# *Semiconductor p-n junction diodes*

## **Semiconductor p-n junction diodes**



# p-n junction formation

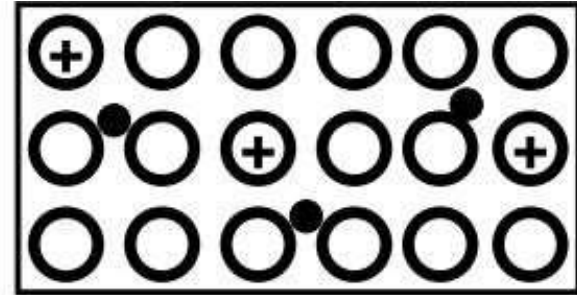


## p-type material

Semiconductor material doped with **acceptors**.

Material has high hole concentration

Concentration of free electrons in p-type material is very low.



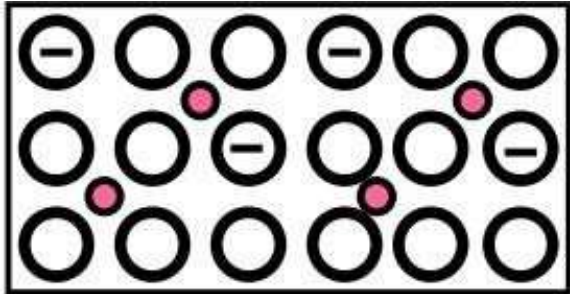
## n-type material

Semiconductor material doped with **donors**.

Material has high concentration of free electrons.

Concentration of holes in n-type material is very low.

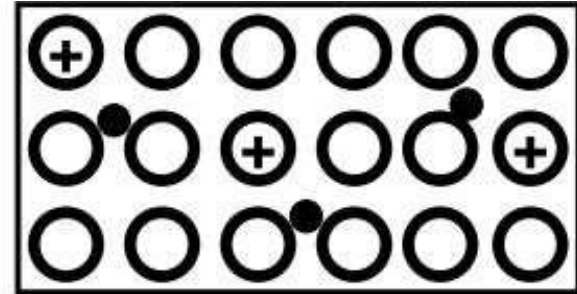
# p-n junction formation



## p-type material

Contains  
NEGATIVELY  
charged acceptors  
(immovable) and  
POSITIVELY charged  
holes (free).

Total charge = 0

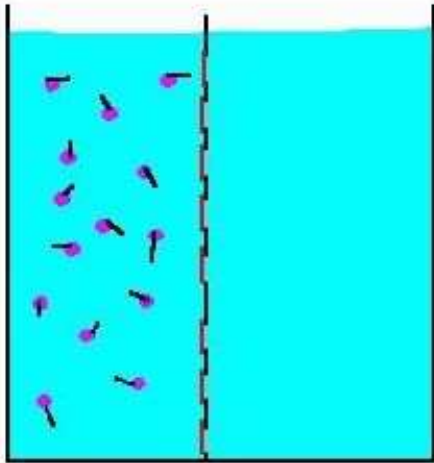


## n-type material

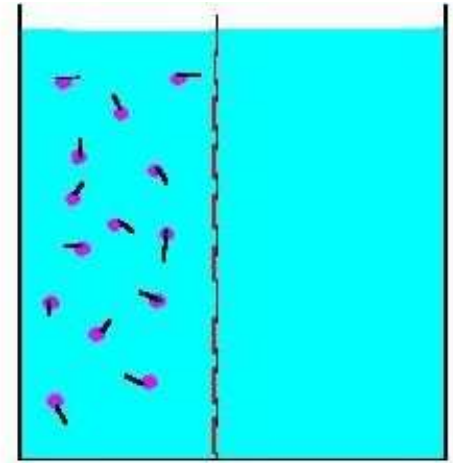
Contains POSITIVELY  
charged donors  
(immovable) and  
NEGATIVELY  
charged free electrons.

Total charge = 0

# Diffusion



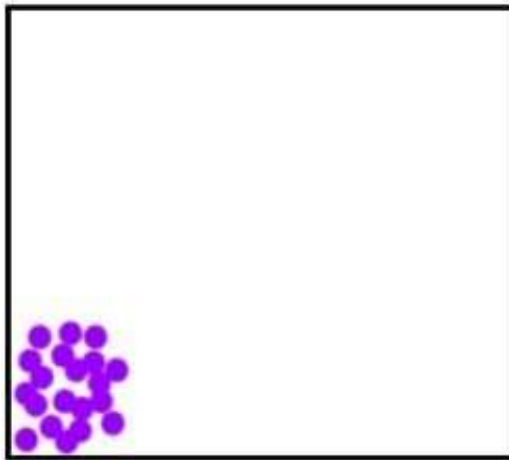
A substance, the purple dots, in solution. A membrane prevents movement of the water and the molecules from crossing from one side of the beaker to the other.



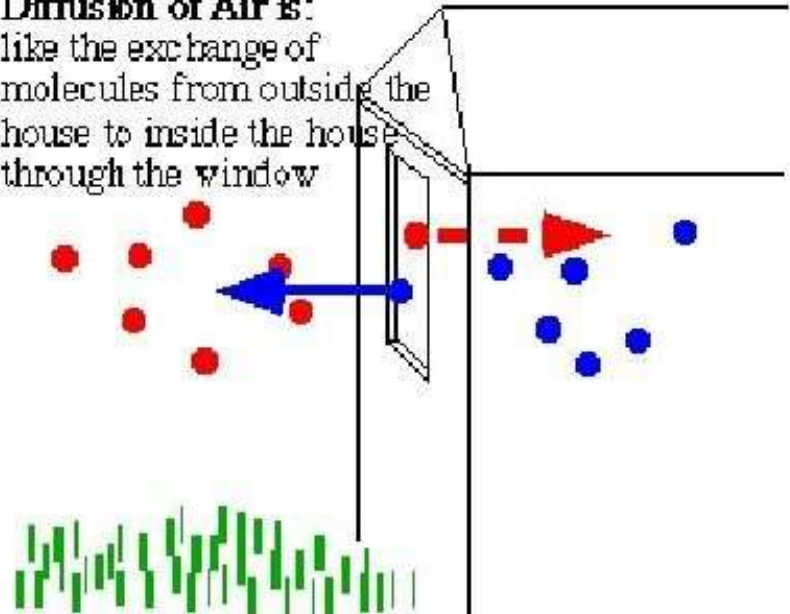
Now that the gates have been opened, the random movements of the molecules have caused, overtime, the number of molecules to be equal on the two sides of the barrier.



# Diffusion



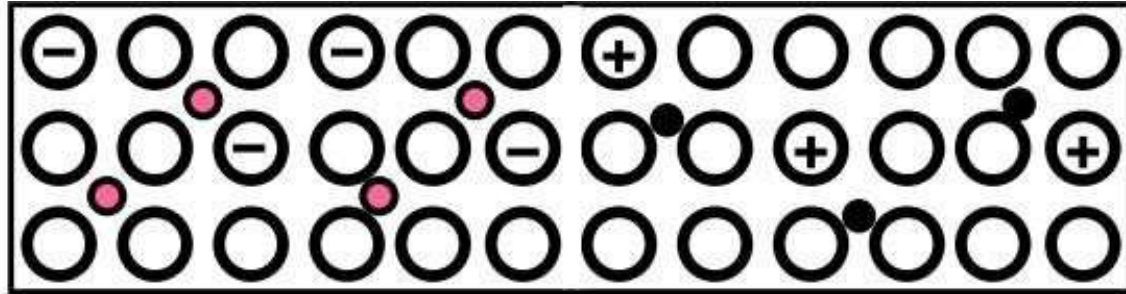
Diffusion of Air is:  
like the exchange of  
molecules from outside the  
house to inside the house  
through the window



**As a result of diffusion, the molecules or other free particles distribute uniformly over the entire volume**

# p- n junction formation

What happens if n- and p-type materials are in close contact?



Being free particles, **electrons** start diffusing from n-type material into p-material

Being free particles, **holes**, too, start diffusing from p-type material into n-material

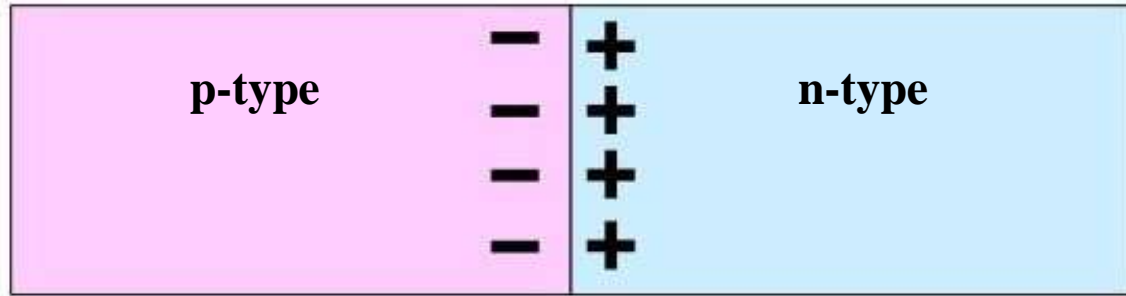
Have they been NEUTRAL particles, eventually all the free electrons and holes had uniformly distributed over the entire compound crystal.

However, every electrons transfers a negative charge ( $-q$ ) onto the p-side and also leaves an uncompensated ( $+q$ ) charge of the donor on the n-side.

Every hole creates one positive charge ( $q$ ) on the n-side and ( $-q$ ) on the p-side

# p- n junction formation

What happens if n- and p-type materials are in close contact?



Electrons and holes remain staying close to the p-n junction because negative and positive charges attract each other.

Negative charge stops electrons from further diffusion

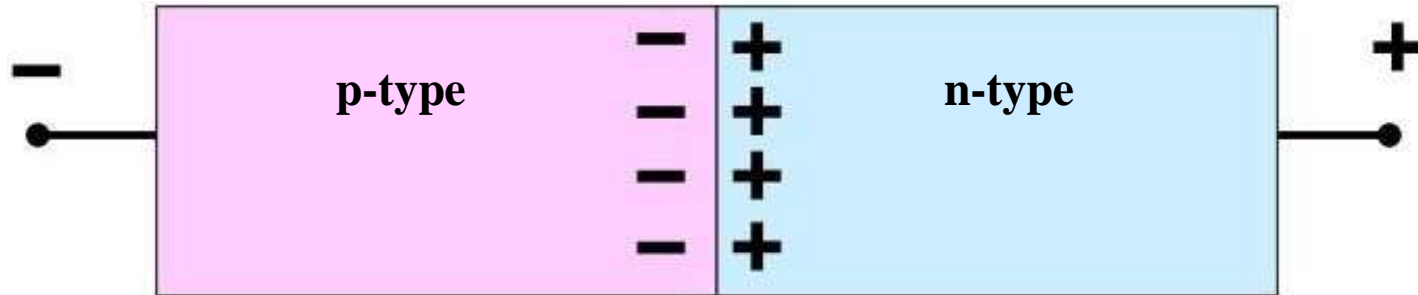
Positive charge stops holes from further diffusion

**The diffusion forms a dipole charge layer at the p-n junction interface.**

**There is a “built-in” VOLTAGE at the p-n junction interface that prevents penetration of electrons into the p-side and holes into the n-side.**

# p- n junction current - voltage characteristics

What happens when the voltage is applied to a p-n junction?



The polarity shown, attracts holes to the left and electrons to the right.

According to the **current continuity law**, the current can **only** flow if all the charged particles move forming a closed loop

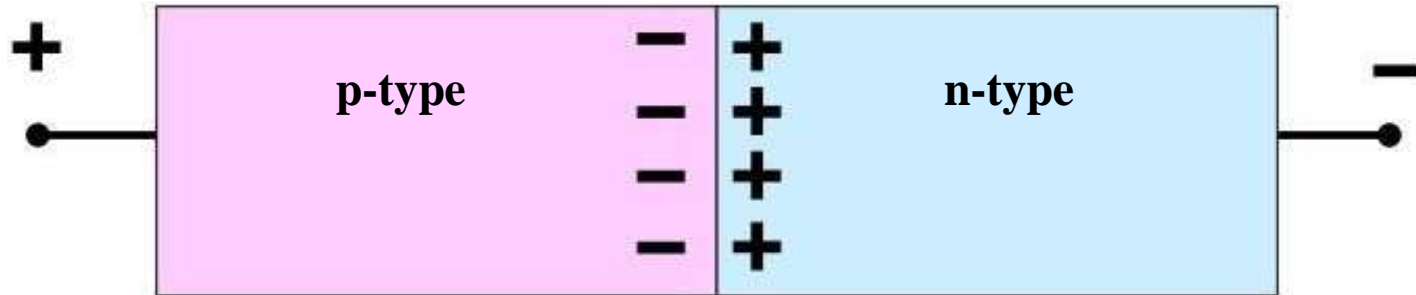
However, there are very few holes in n-type material and there are very few electrons in the p-type material.

There are very few carriers available to support the current through the junction plane

**For the voltage polarity shown, the current is nearly zero**

## p- n junction current - voltage characteristics

**What happens if voltage of opposite polarity is applied to a p-n junction?**



The polarity shown, attracts electrons to the left and holes to the right.

There are plenty of electrons in the n-type material and plenty of holes in the p-type material.

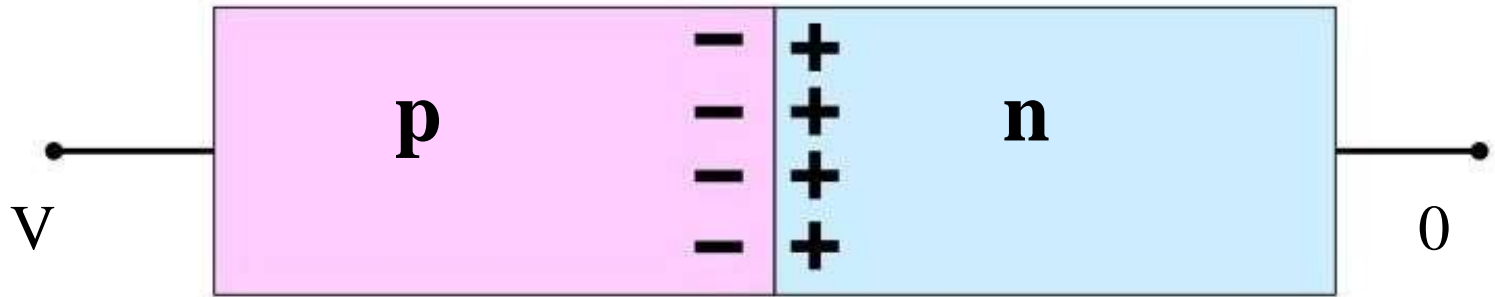
There are a lot of carriers available to cross the junction.

**When the voltage applied is lower than the built-in voltage,  
the current is still nearly zero**

**When the voltage exceeds the built-in voltage, the current can flow through  
the p-n junction**

# Diode current - voltage (I-V) characteristics

Semiconductor diode consists of a p-n junction with two contacts attached to the p- and n- sides



$$I = I_S \exp \left( \frac{qV}{kT} \right) - 1$$

$I_S$  is usually a very small current,  $I_S \approx 10^{-17} \dots 10^{-13} \text{ A}$

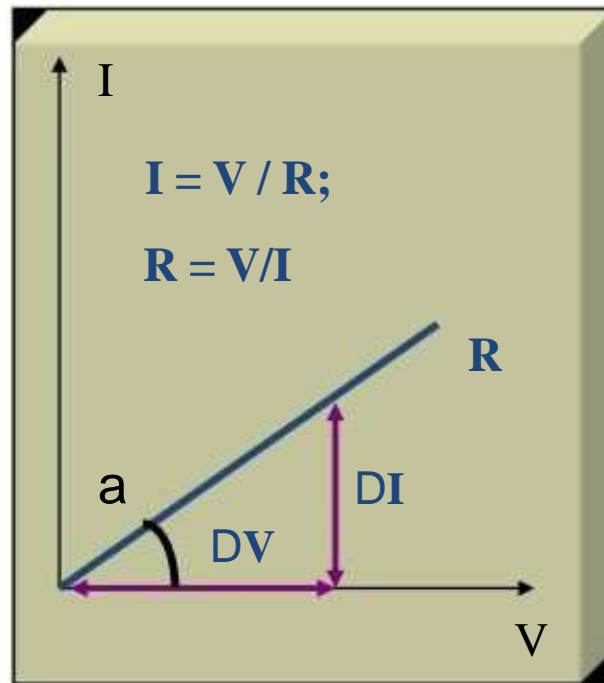
When the voltage  $V$  is negative (“reverse” polarity) the exponential term  $\approx -1$ ;  
The diode current is  $\approx I_S$  ( very small).

When the voltage  $V$  is positive (“forward” polarity) the exponential term increases rapidly with  $V$  and the current is high.

# Graphing the I-V characteristics of electronic components.

The I-V plot represents the dependence of the current  $I$  through the component on the voltage  $V$  across it.

Resistor  $V = I \cdot R; \quad I = \frac{1}{R} \cdot V$



$$\operatorname{tg}(a) = 1/R$$

**The I-V characteristic of the resistor**

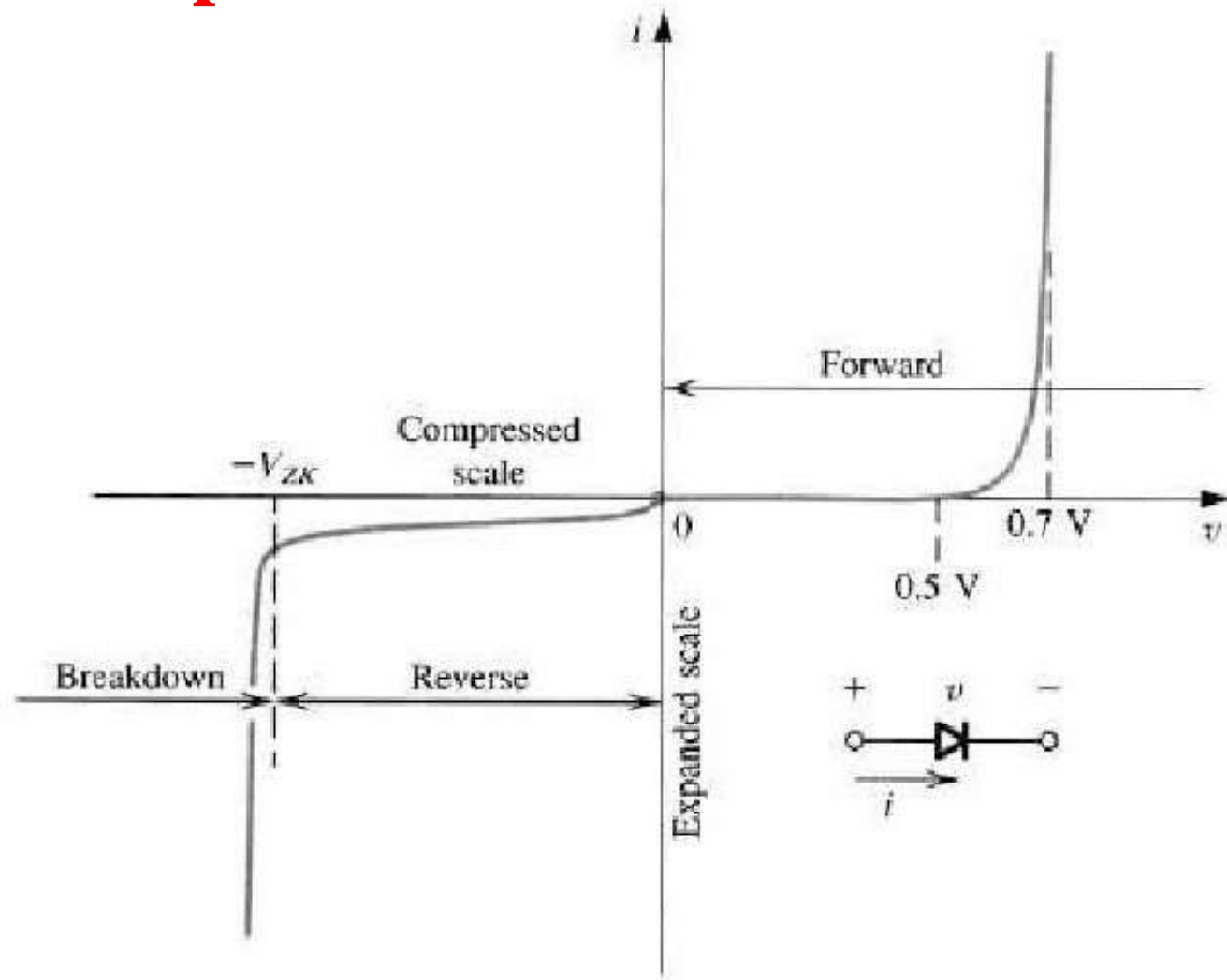
# The I-V characteristic of the diode

$$I = I_S \exp\left(\frac{qV}{kT}\right) - 1$$

$I_S$

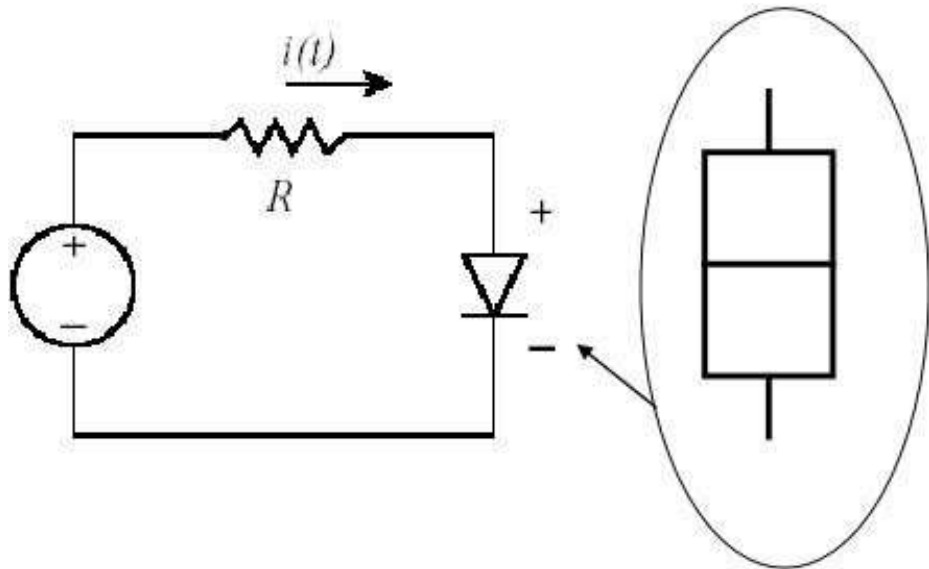


# The experimental I-V characteristic of a Si



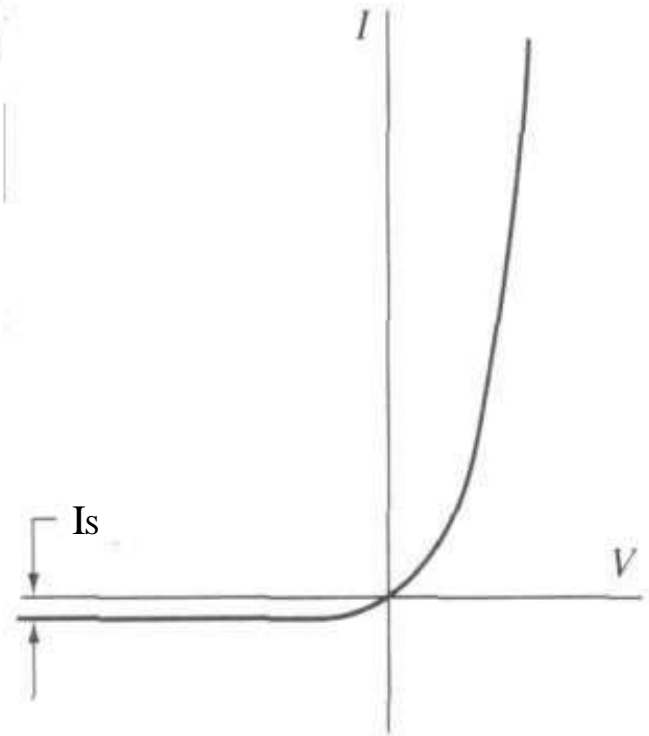
The diode  $i$ - $v$  relationship with some scales expanded and others compressed in order to reveal details.

# p- n diode circuit notation



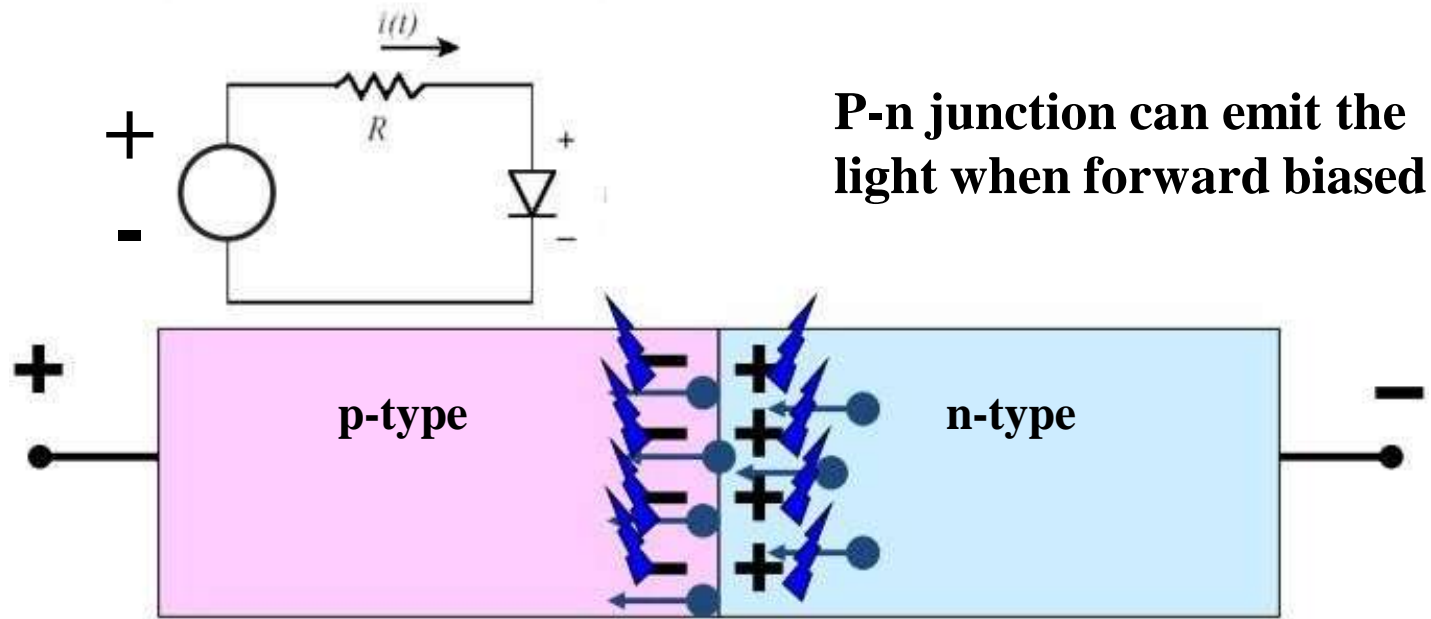
When “plus” is applied to the p-side,  $I \cdot I_s \exp$  the current is high. This voltage polarity is called **FORWARD**.

When “plus” is applied to the n-side, the current is nearly zero. This voltage polarity is called **REVERSE**.



# p- n diode applications

## Light emitters



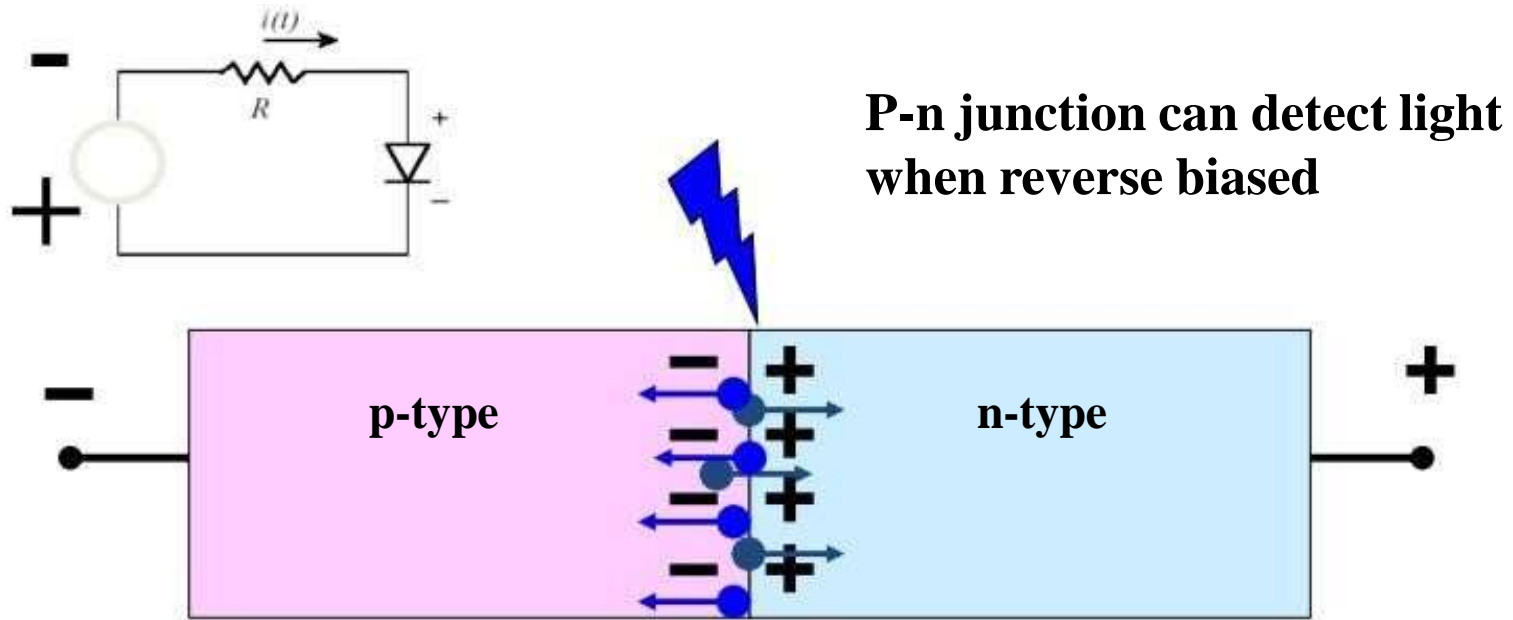
**P-n junction can emit the light when forward biased**

Electrons drift into p-material and find plenty of holes there. They “RECOMBINE” by filling up the “empty” positions.

Holes drift into n-material and find plenty of electrons there. They also “RECOMBINE” by filling up the “empty” positions.

The energy released in the process of “annihilation” produces  
PHOTONS - the particles of light

## p- n diode applications: Photodetectors



When the light illuminates the p-n junction, the photons energy RELEASES free electrons and holes.

They are referred to as PHOTO-ELECTRONS and PHOTO-HOLES

The applied voltage separates the photo-carriers attracting electrons toward “plus” and holes toward “minus”

As long as the light is ON, there is a current flowing through the p-n junction

# NEGATIVE RESISTANCE DEVICE

- It is a device which exhibits a negative incremental resistance over a limited range of V-I characteristic.
- It is of two types :-
  1. Current controllable type : V-I curve is a multi valued function of voltage and single valued function of current .eg:- UJT, p-n-p-n diode
  2. Voltage controllable type : V-I curve is a multi valued function of current and single valued function of voltage. eg:- SCS, Tunnel diode

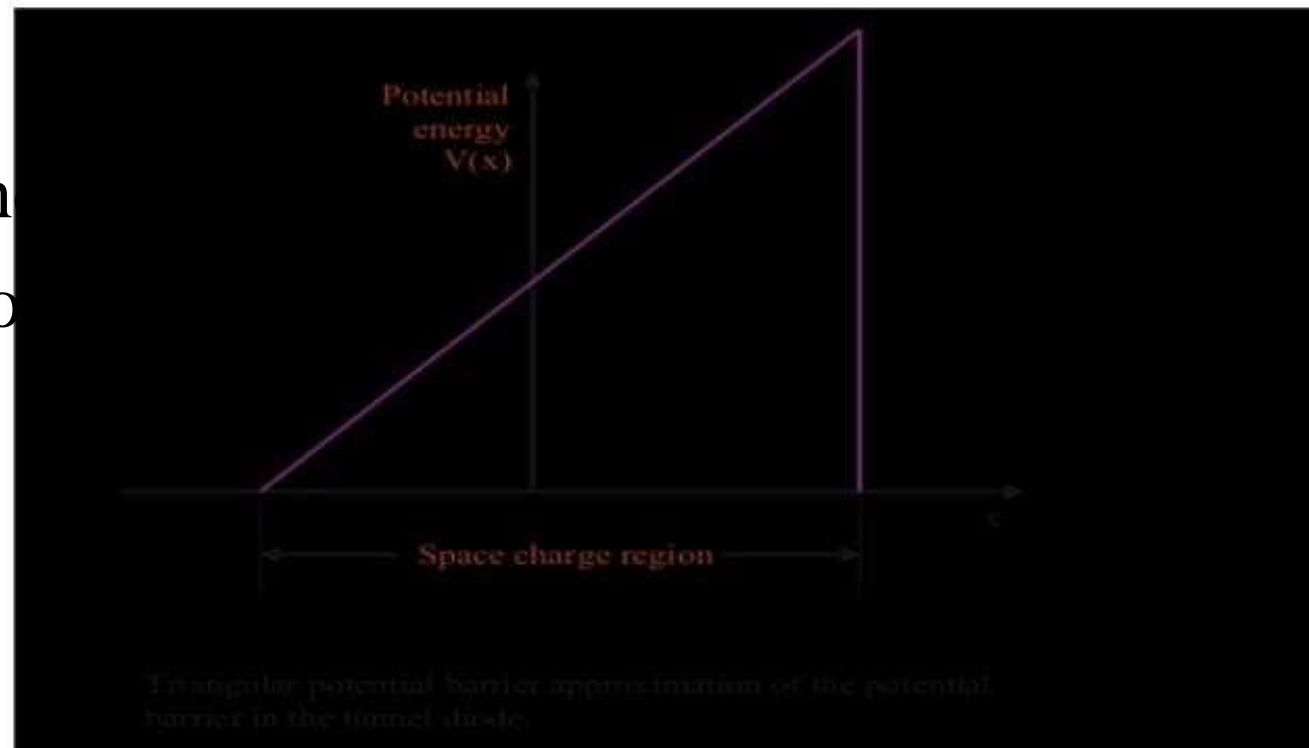
# TUNNEL DIODE (Esaki Diode)

- It was introduced by Leo Esaki in 1958.
- Heavily-doped p-n junction
  - Impurity concentration is 1 part in  $10^3$  as compared to 1 part in  $10^8$  in p-n junction diode
- Width of the depletion layer is very small (about 100 Å).
- It is generally made up of Ge and GaAs.
- It shows tunneling phenomenon.
- Circuit symbol of tunnel diode is :



# WHAT IS TUNNELING

- **Classically**, carrier must have energy at least equal to potential-barrier height to cross the junction .
- But according to **Quantum mechanics** there is finite probability that it can penetrate through the barrier for a thin width.
- This phenomenon called **tunneling** and hence the Esaki Diode is known as **Tunnel Diode**.



# CHARACTERISTIC OF TUNNEL DIODE

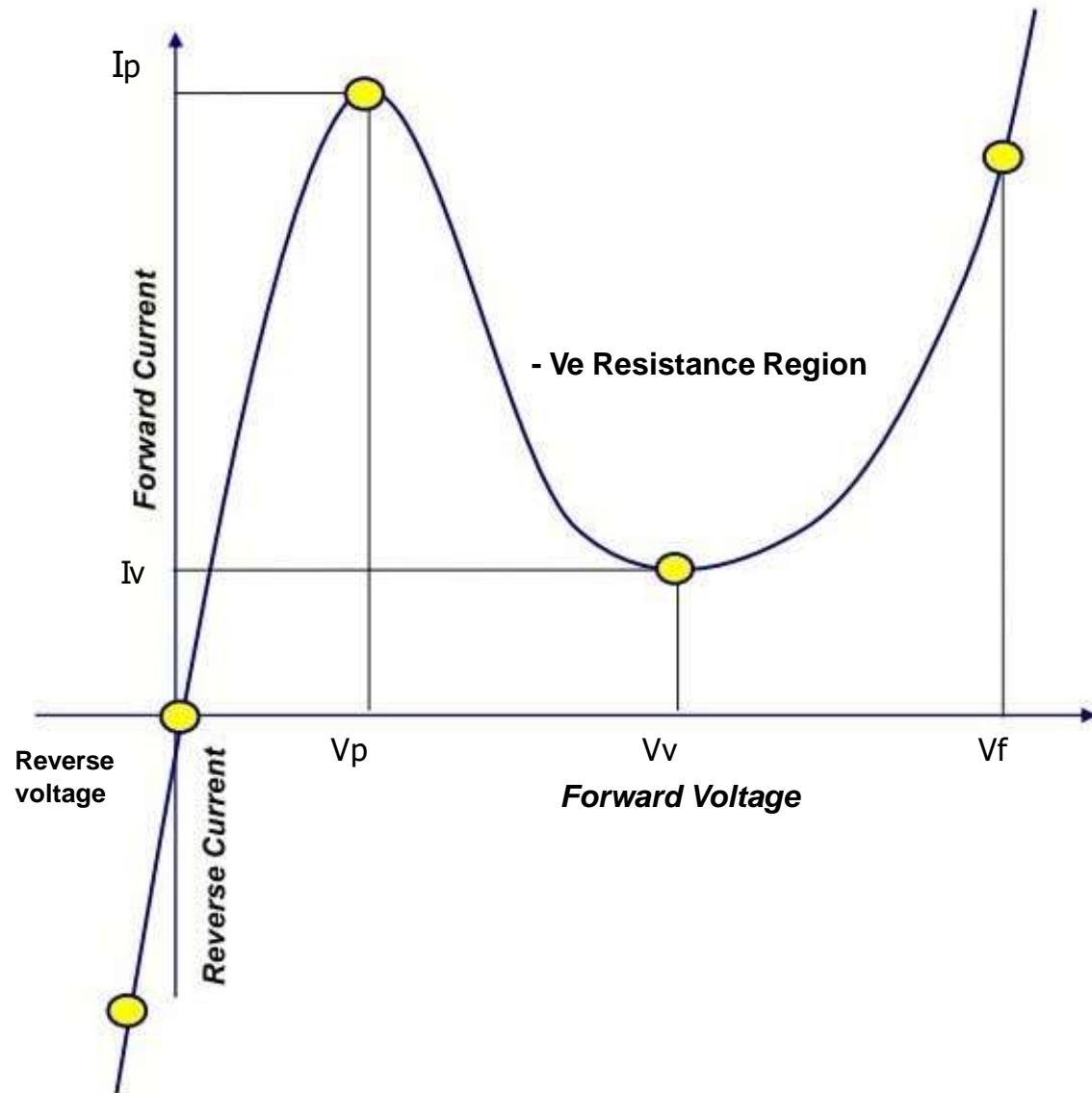
$I_p$ :- Peak Current

$I_v$  :- Valley Current

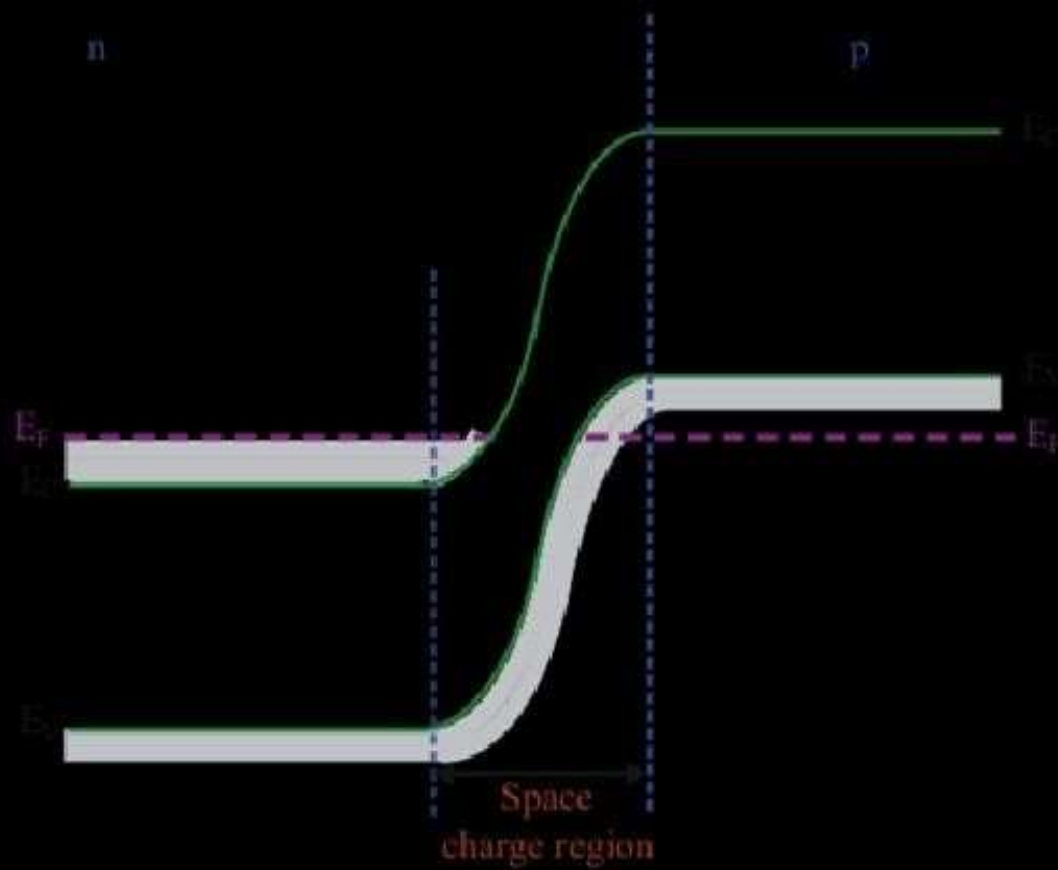
$V_p$ :- Peak Voltage

$V_v$ :- Valley Voltage

$V_f$ :- Peak Forward  
Voltage

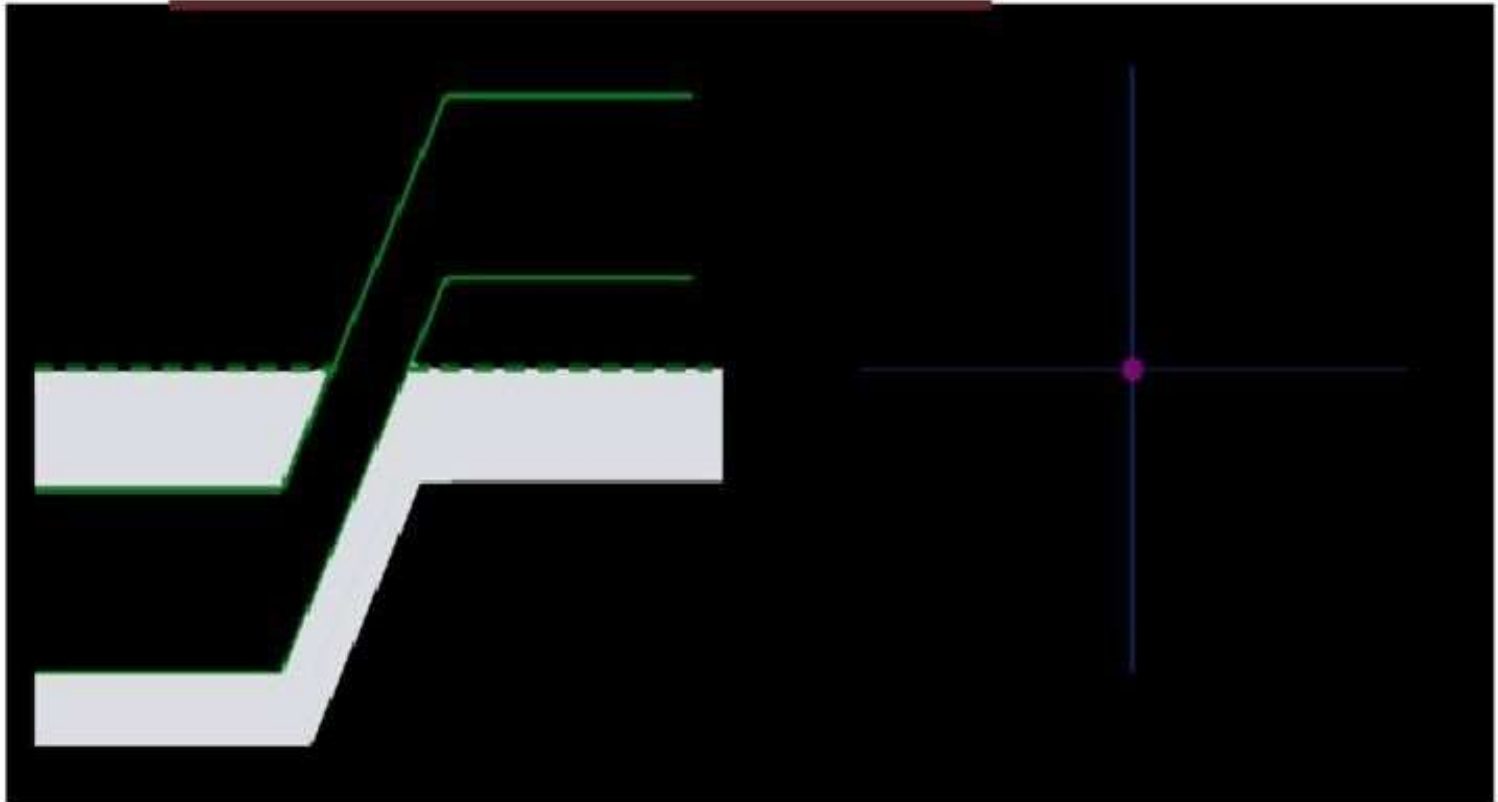






Energy-band diagram of pn junction in thermal equilibrium in which both the n and p region are degenerately doped.

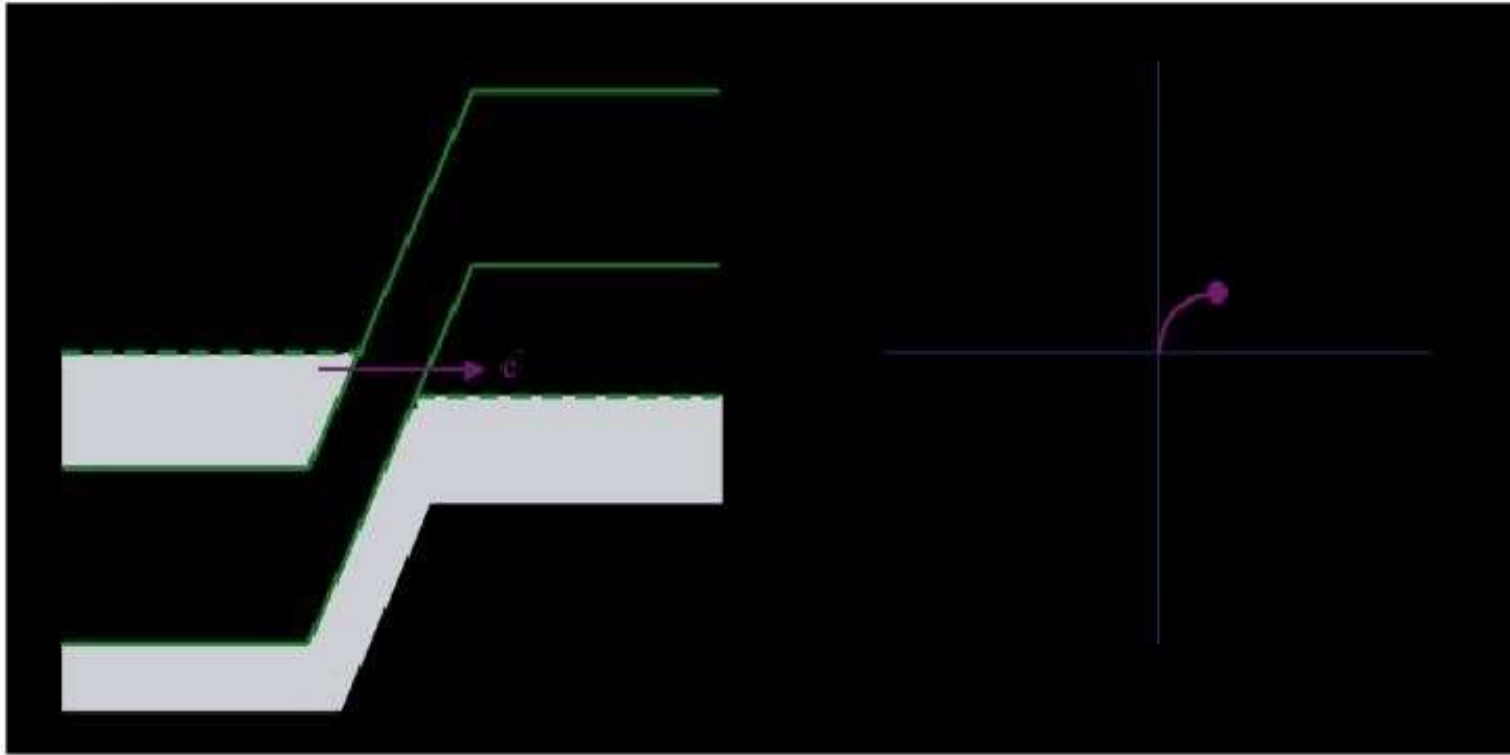
# AT ZERO BIAS



Simplified energy-band diagram and I-V characteristics of the tunnel diode at zero bias.

- Zero current on the I-V diagram;
- All energy states are filled below  $E_F$  on both sides of the junction;

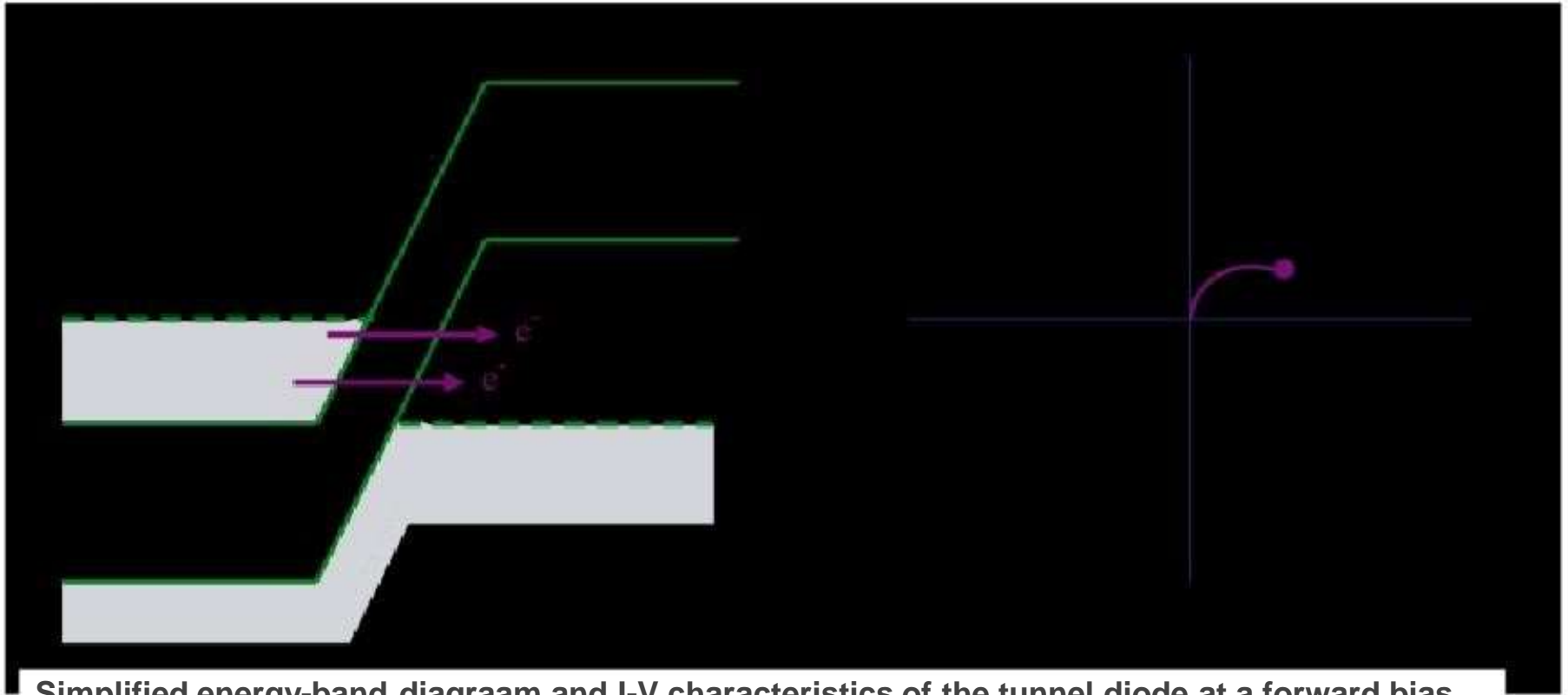
# AT SMALL FORWARD VOLTAGE



Simplified energy-band diagram and I-V characteristics of the tunnel diode at a slight forward bias.

- Electrons in the conduction band of the n region are directly opposite to the empty states in the valence band of the p region.
- So a finite probability that some electrons tunnel directly into the empty states resulting in forward-bias tunneling current.

# AT MAXIMUM TUNNELING CURENT



Simplified energy-band diagram and I-V characteristics of the tunnel diode at a forward bias producing maximum tunneling current.

- The maximum number of electrons in the n region are opposite to the maximum number of empty states in the p region.
- Hence tunneling current is maximum.

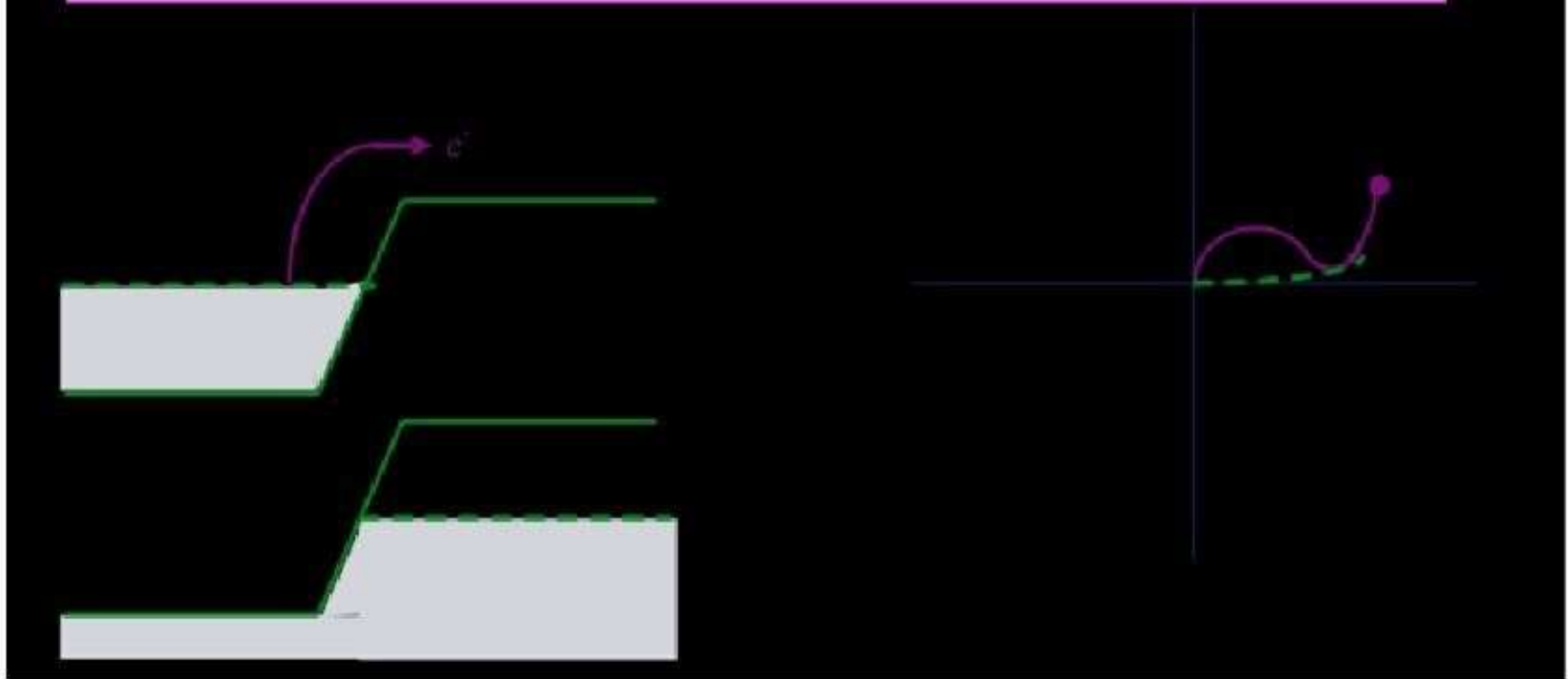
# AT DECREASING CURRENT REGION



Simplified energy-band diagram and I-V characteristics of the tunnel diode at a higher forward bias producing less tunneling current.

- The forward-bias voltage increases so the number of electrons on the n side, directly opposite empty states on the p side decreases.
- Hence the tunneling current decreases.

# AT HIGHER FORWARD VOLTAGE



Simplified energy-band diagram and I-V characteristics of the tunnel diode at a forward bias for which the diffusion current dominates.

- No electrons on the n side are directly opposite to the empty states on the p side.
- The tunneling current is zero.
- The normal ideal diffusion current exists in the device.

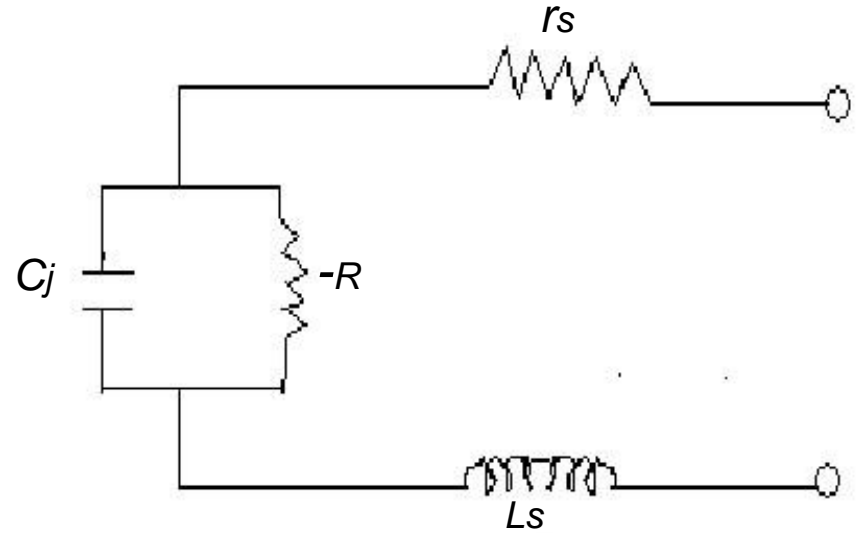
# AT REVERSE BIAS VOLTAGE



- Electrons in the valence band on the p side are directly opposite to empty states in the conduction band on the n side.
- Electrons tunnel directly from the p region into the n region.
- The reverse-bias current increases monotonically and rapidly with reverse-bias voltage.

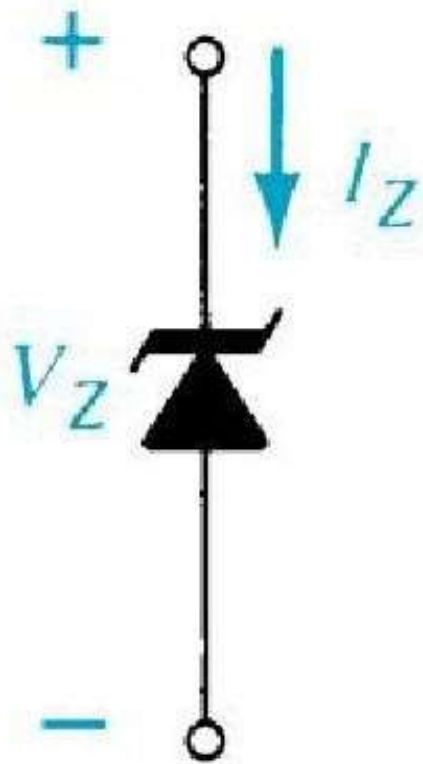
# TUNNEL DIODE EQUIVALENT CIRCUIT

- This is the equivalent circuit of tunnel diode when biased in negative resistance region.
- At higher frequencies the series  $R$  and  $L$  can be ignored.
- Hence equivalent circuit can be reduced to parallel combination of junction capacitance and negative resistance.





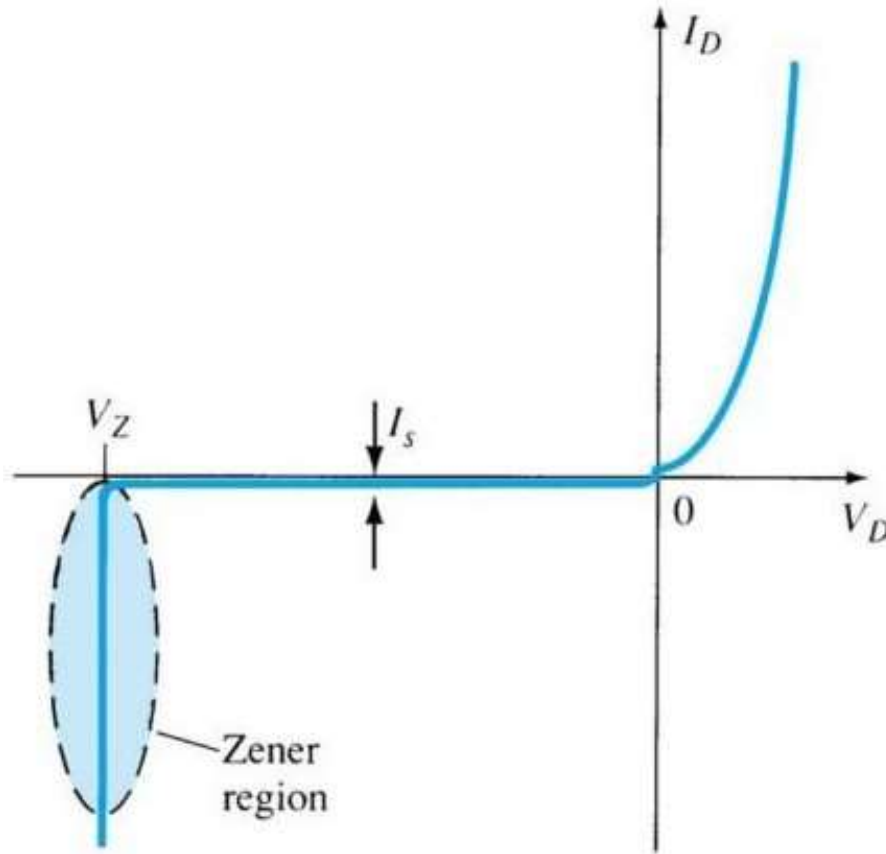
# Zener Diode



(a)

- A Zener is a diode operated in reverse bias at the Peak Inverse Voltage (PIV) called the Zener Voltage ( $V_Z$ ).
- Common Zener Voltages: 1.8V to 200V

# Zener Region



The diode is in the reverse bias condition.

At some point the reverse bias voltage is so large the diode breaks down.

The reverse current increases dramatically.

This maximum voltage is called ***avalanche breakdown voltage*** and the current is called ***avalanche current***.

# Resistance Levels

Semiconductors act differently to DC and AC currents.  
There are 3 types of resistances.

- DC or Static Resistance
- AC or Dynamic Resistance
- Average AC Resistance

- DC or Static Resistance

- The resistance of a diode at a particular operating point is called the dc or static resistance diode. It can be determined using equation (1.1):

$$R_D = V_D / I_D$$

(1.1)

## Example : DC or Static Resistance - refer Figure 1.1

Ideal diode			Si diode		
$I_D(\text{A})$	$V_D(\text{V})$	$R_D(\cdot)$	$I_D(\text{A})$	$V_D(\text{V})$	$R_D(\cdot)$
20m	0	0	20m	0.8	40
2m	0	0	2m	0.5	250

dc resistance of forward-bias region decrease when higher currents and voltage.

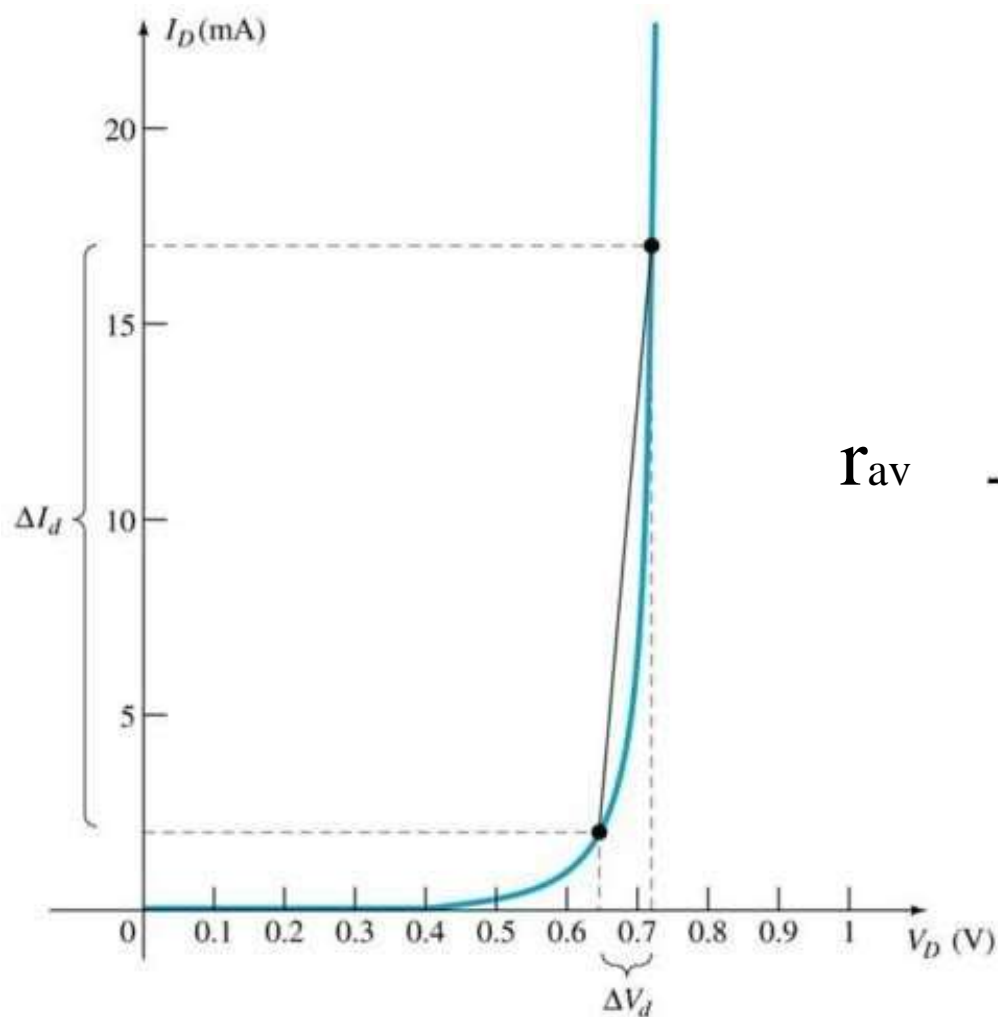
Ideal diode			Si diode		
$I_D(A)$	$V_D(V)$	$R_D(\cdot)$	$I_D(A)$	$V_D(V)$	$R_D(\cdot)$
0	-10	$\cdot$	-2 $\cdot$	-10	5M

- dc resistance of reverse-bias region, its open-circuit equivalent.

- AC or Dynamic Resistance
- Static resistance is using dc input. If the input is sinusoidal the scenario will be change.
- The varying input will move instantaneous operating point UP and DOWN of a region.
- Thus the specific changes in current and voltage is obtained. It can be determined using equation (1.2)

$r_d = \Delta V_D / \Delta I_D$	(1.2)
---------------------------------	-------

- Average AC Resistance



$$r_{av} = \frac{V_d}{I_d} \text{ (point to point)}$$

AC resistance can be determined by picking 2 points on the characteristic curve developed for a particular circuit.



# **RECTIFIERS, FILTERS AND REGULATORS**

# Introduction

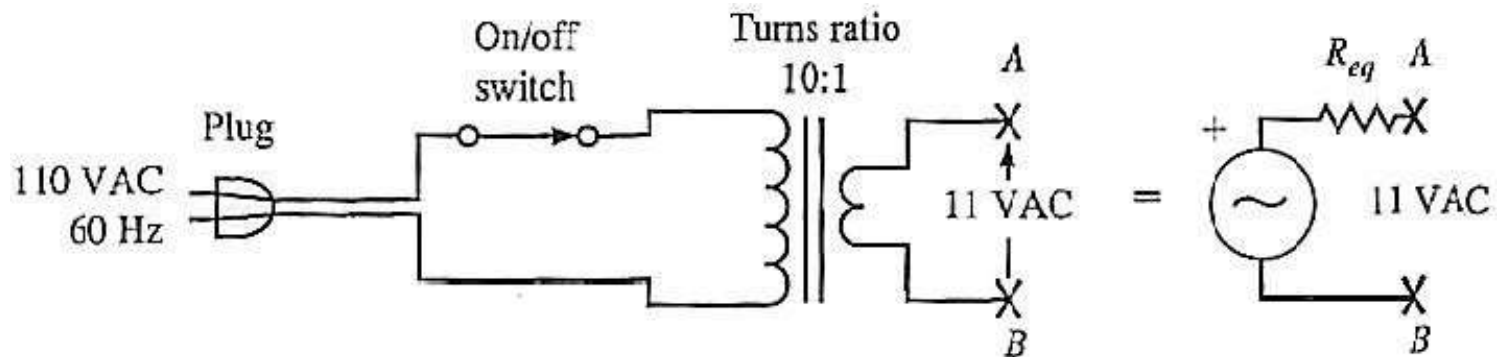
A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which is in only one direction, a process known as rectification.

# Power Supply Circuits

- To achieve its purpose a power supply must:
  - Step down the voltage supplied;
  - Convert ac to dc by rectifying the ac.
- A transformer is used to step down the magnitude of the voltages from the wall receptacle.

# Transformer

- A transformer consists of two coils of wire on a common iron core. The voltages on these two coils are related by the *turns ratio*, which is the ratio of the number of turns of wire in the secondary coil to that in the primary coil.



# RMS Values

- Note that the 110-120 volts and 220-240 volts are RMS values.
- The actual amplitude of that sinusoidal signal is a factor of  $\sqrt{2}$  larger.

# Types of Rectifiers



Half wave Rectifier



Full wave Rectifier



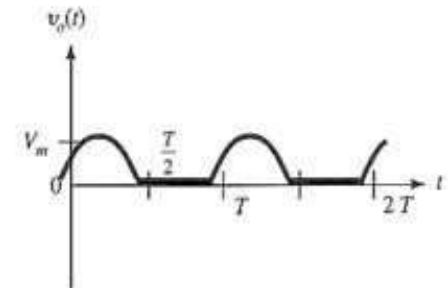
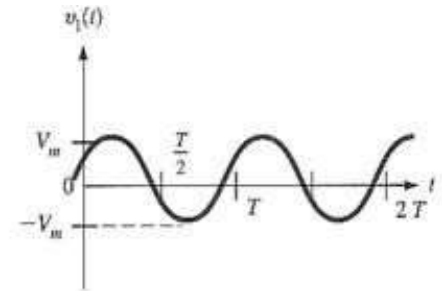
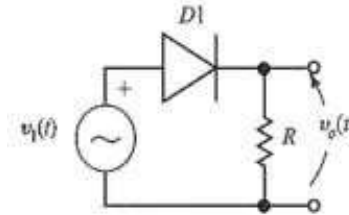
Bridge Rectifier

# Half wave rectifier

- In half wave rectification, either the positive or negative half of the AC wave is passed, while the other half is blocked.
- Because only one half of the input waveform reaches the output, it is very inefficient if used for power transfer.

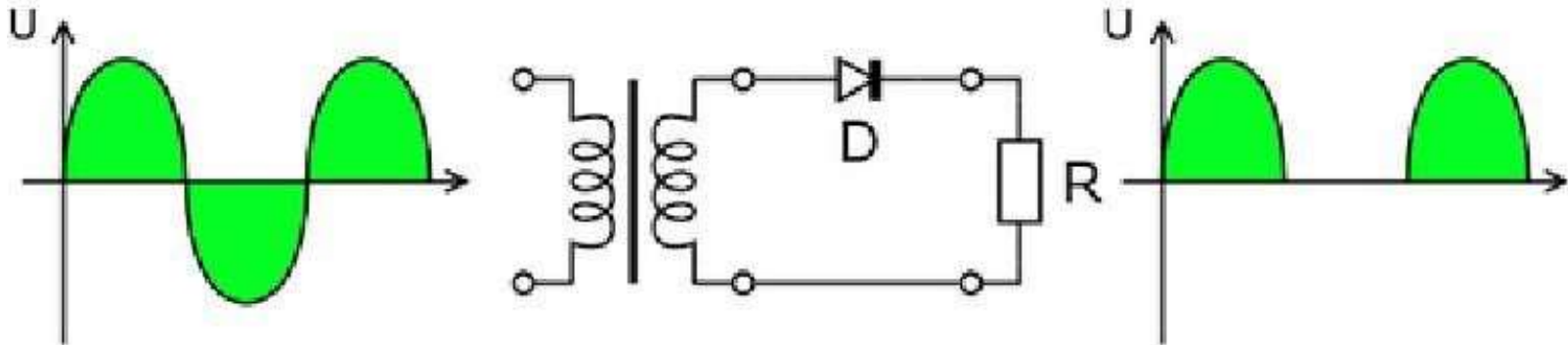
# Half-wave Rectification

- Simplest process used to convert ac to dc.
- A diode is used to clip the input signal excursions of one polarity to zero.





# Half wave rectification



# Output dc voltage calculation

- The output DC voltage of a half wave rectifier can be calculated with the following two ideal equations

$$V_{avg} = \frac{V_{peak}}{2}$$

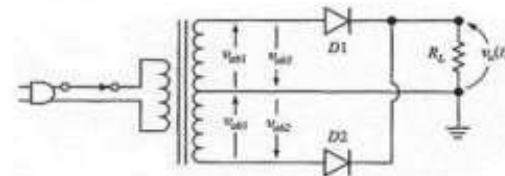
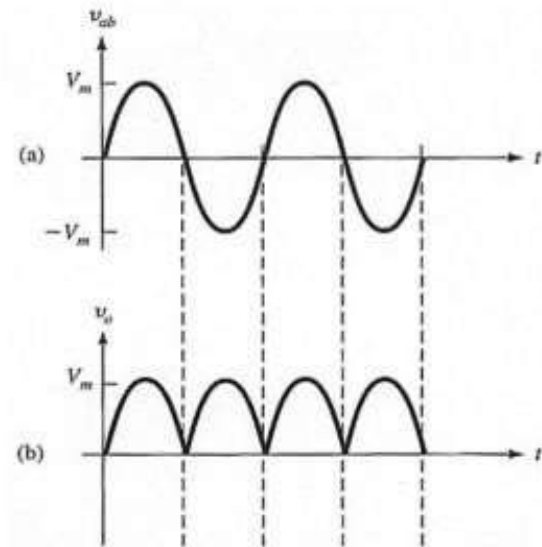
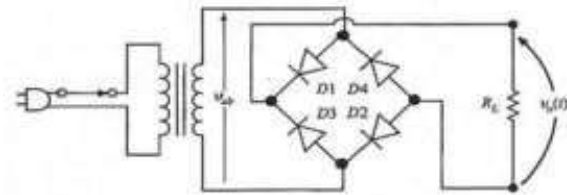
$$V_{dc} = \frac{V_{peak}}{\pi}$$

# Full wave rectifier

- A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output.
- Full-wave rectification converts both polarities of the input waveform to DC (direct current), and is more efficient.0

# Full-wave Rectification

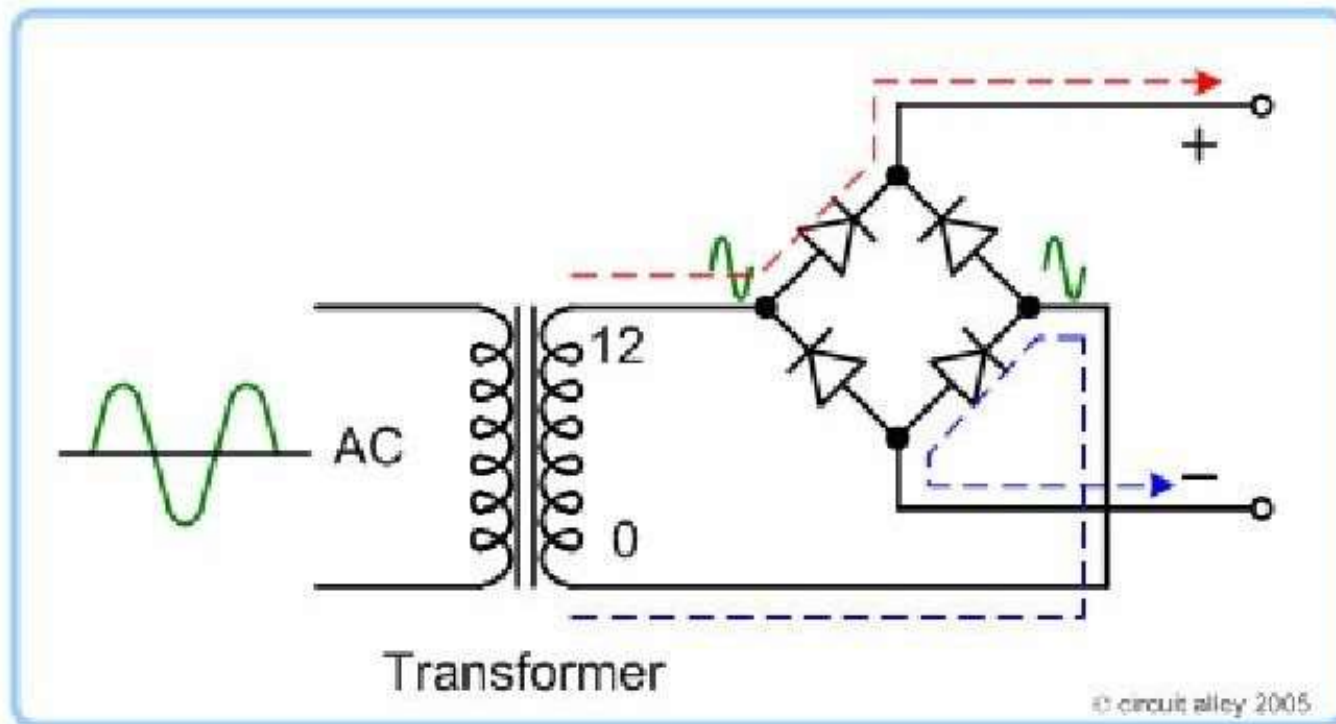
- The output of a full-wave rectifier is driven by both the positive and negative cycles of the sinusoidal input, unlike the half-wave rectifier which uses only one cycle.



# Full wave rectifier

- A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output.
- Full-wave rectification converts both polarities of the input waveform to DC (direct current), and is more efficient.0

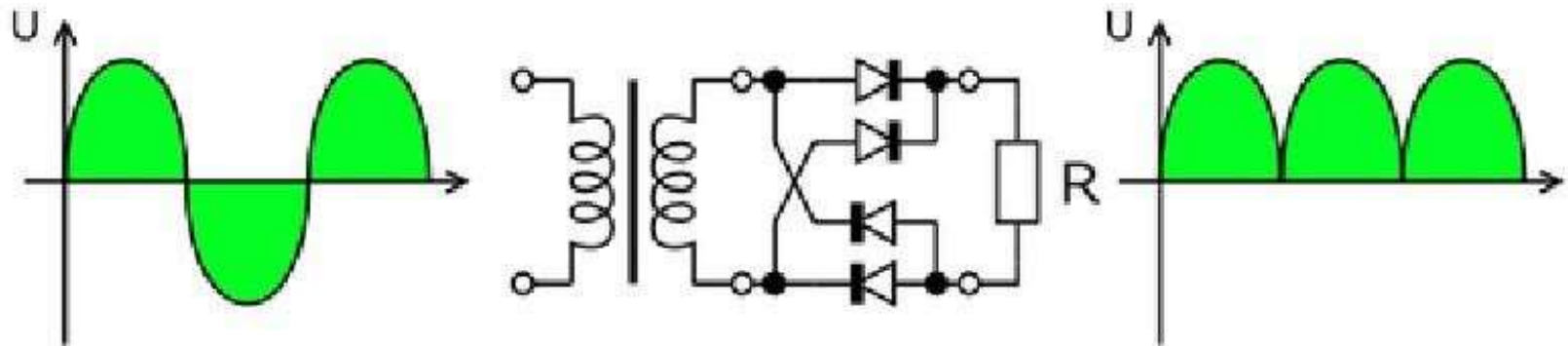
# Full wave rectifier working animation



# Full wave rectification

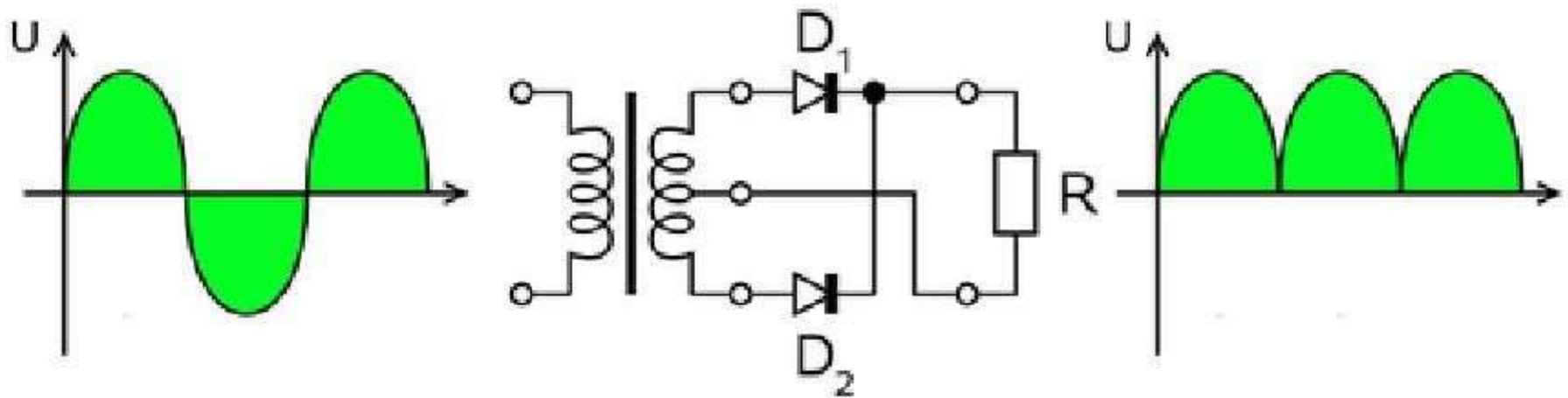
- In a circuit with a non - center tapped transformer, four diodes are required instead of the one needed for half-wave rectification.
- For single-phase AC, if the transformer is center-tapped, then two diodes back-to-back(i.e. anodes-to-anode or cathode-to-cathode) can form a full-wave rectifier.

## Full wave rectifier using 4 diodes





## Full wave rectifier using transformer and 2 diodes

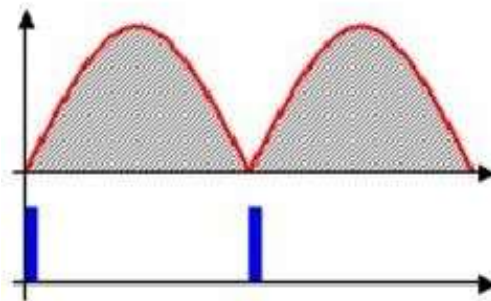


The average and root-mean-square output voltages of an ideal single phase full wave rectifier can be calculated as:

$$V_{dc} = V_{av} = \frac{2V_p}{\pi}$$

$$V_{rms} = \frac{V_p}{\sqrt{2}}$$

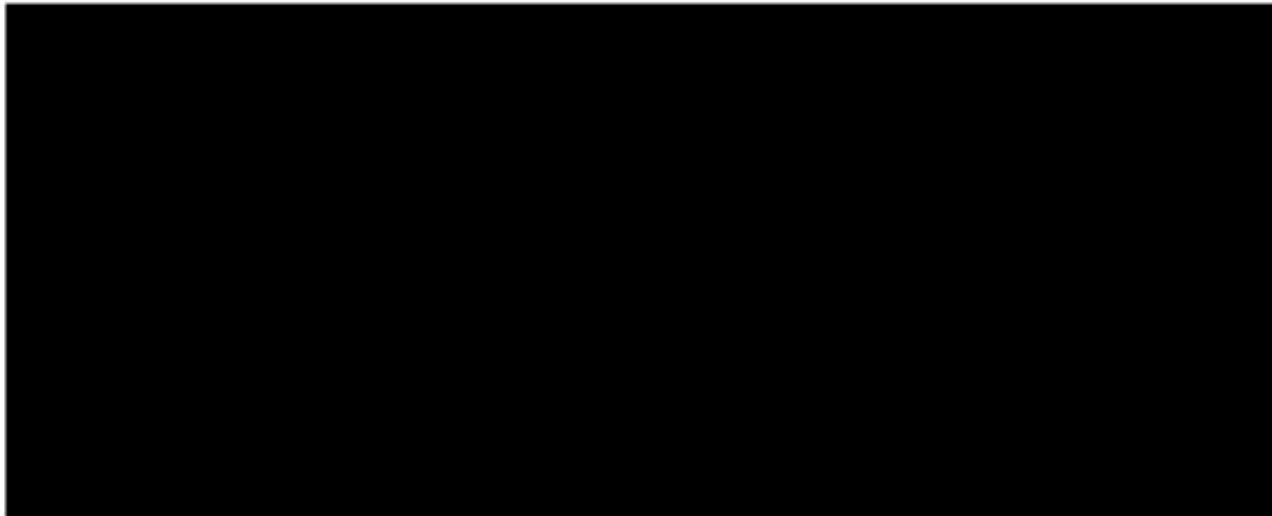
# Output voltage of the full wave rectifier Animation



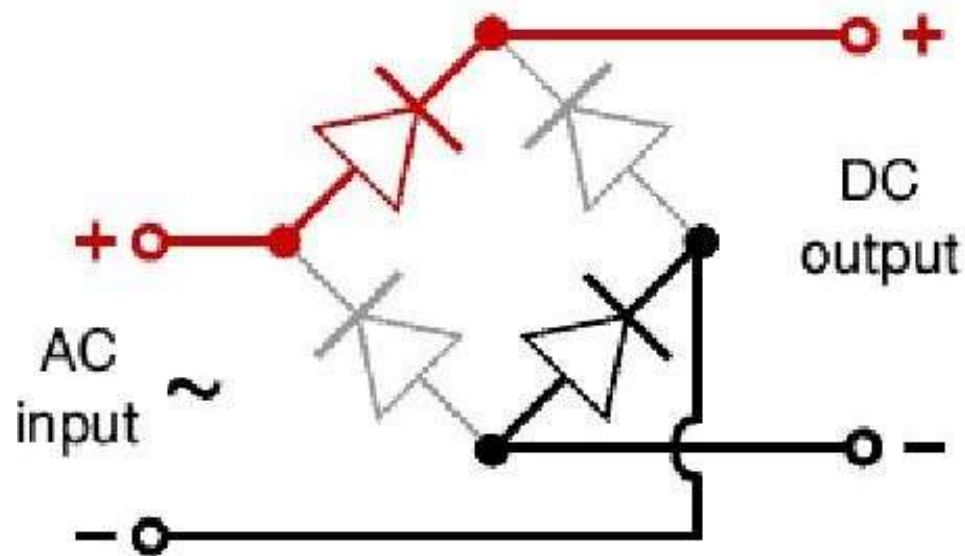
# Bridge rectifier

- A bridge rectifier makes use of four diodes in a bridge arrangement to achieve full-wave rectification.

# Bridge rectifier circuit

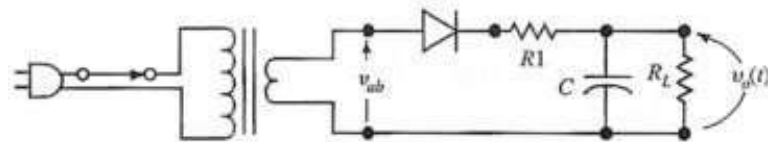
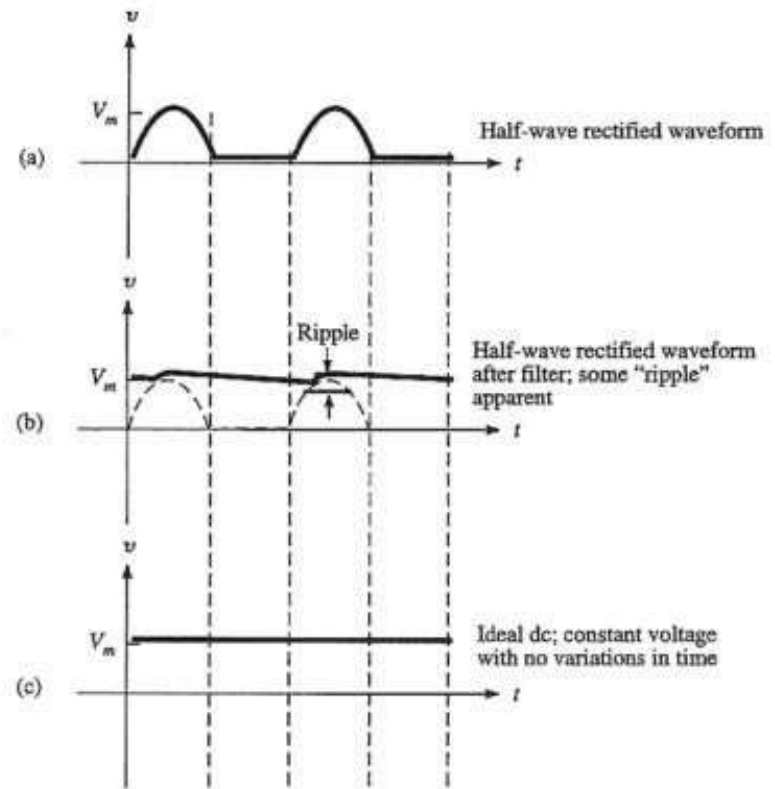


# Bridge rectifier working animation

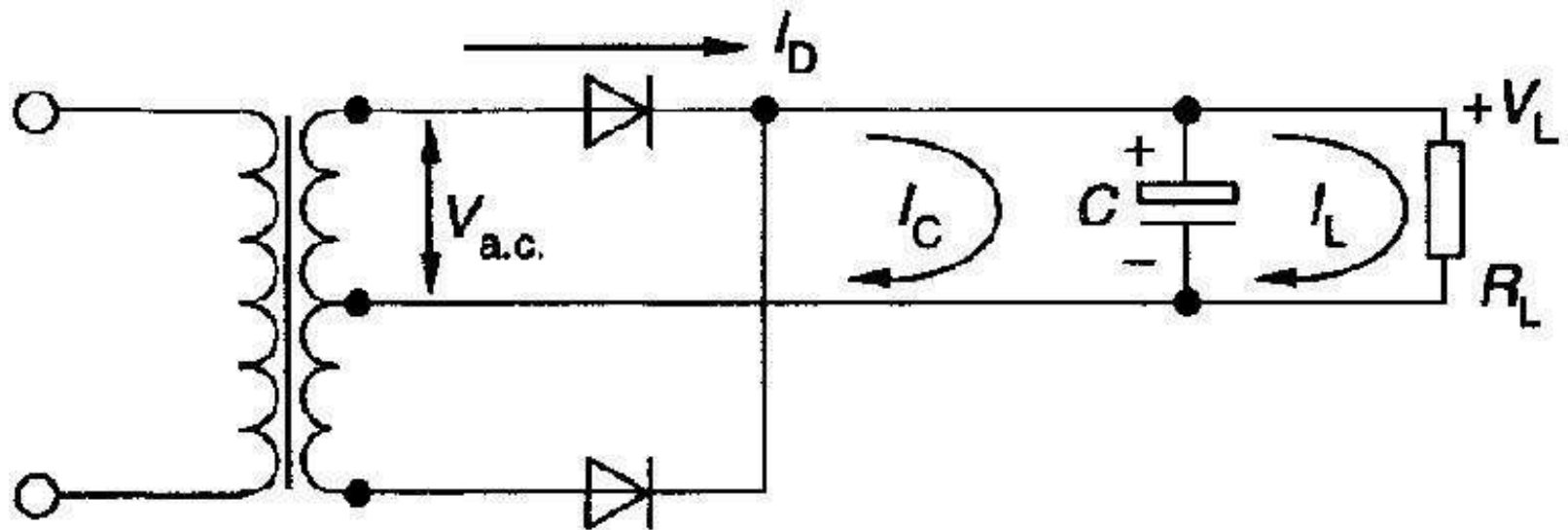


# Filtering

- Process used to smooth out the output of the rectifier circuit.
- One of the most common filter is the RC network.

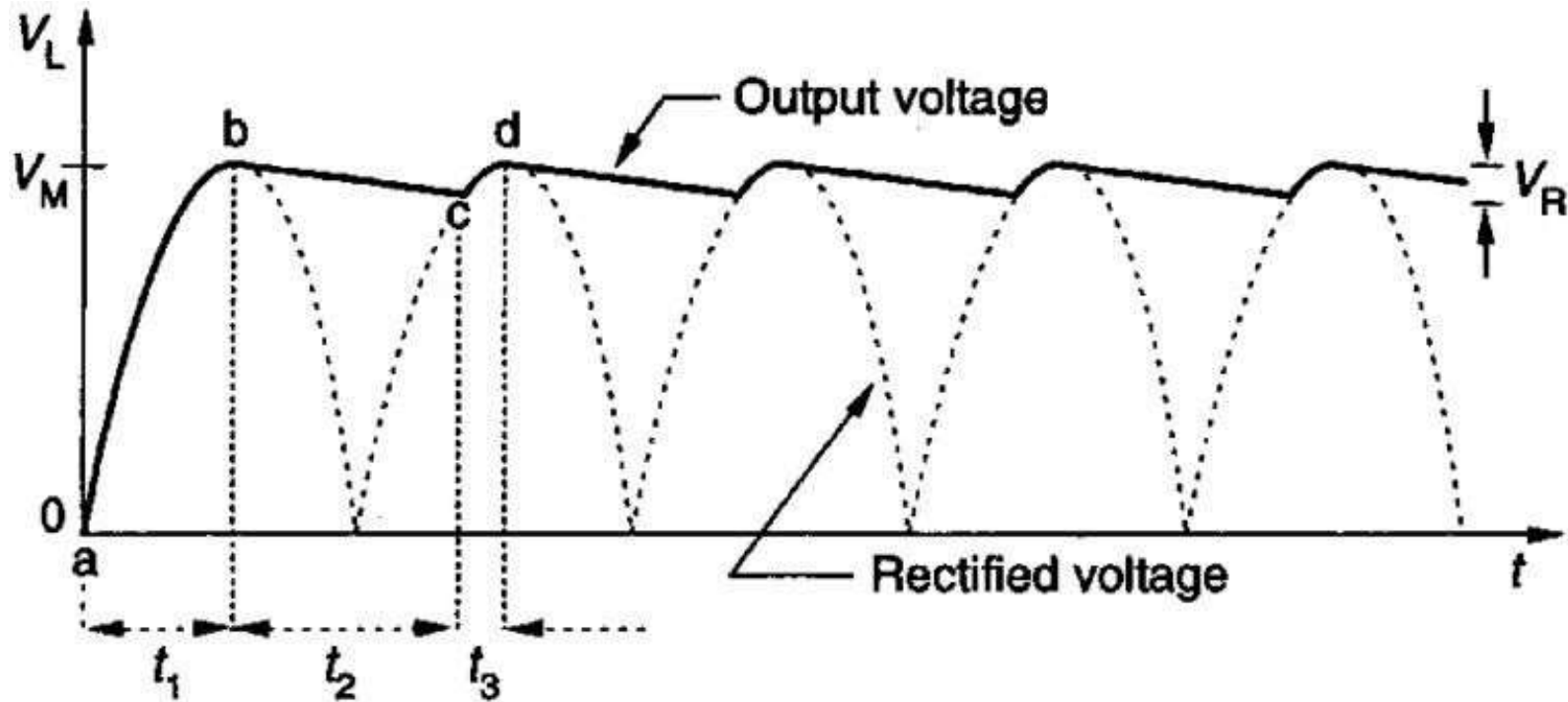


# Full-wave centre-tap rectifier and capacitor filter with load connected

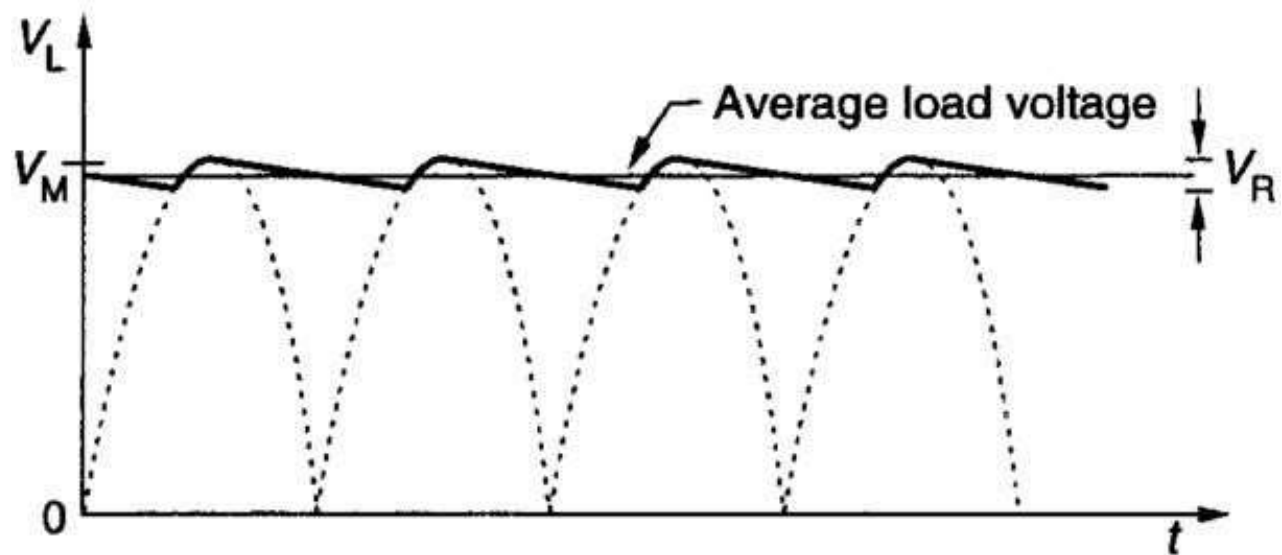




# Capacitor filter output waveforms with load connected

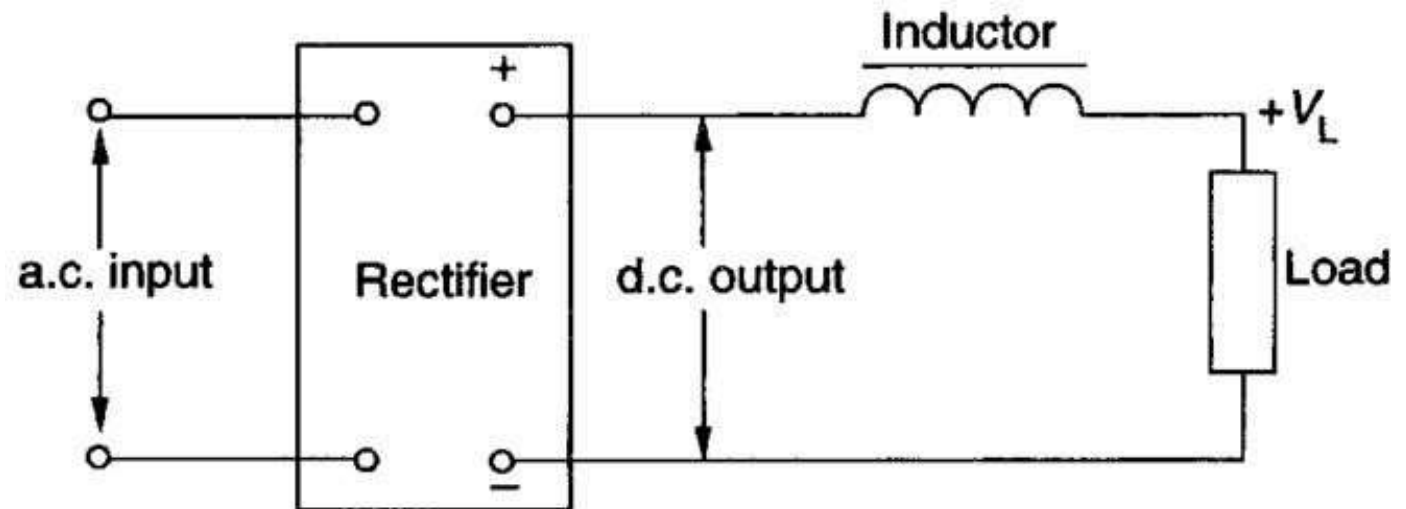


# Effect of load on the output of a capacitor filter circuit

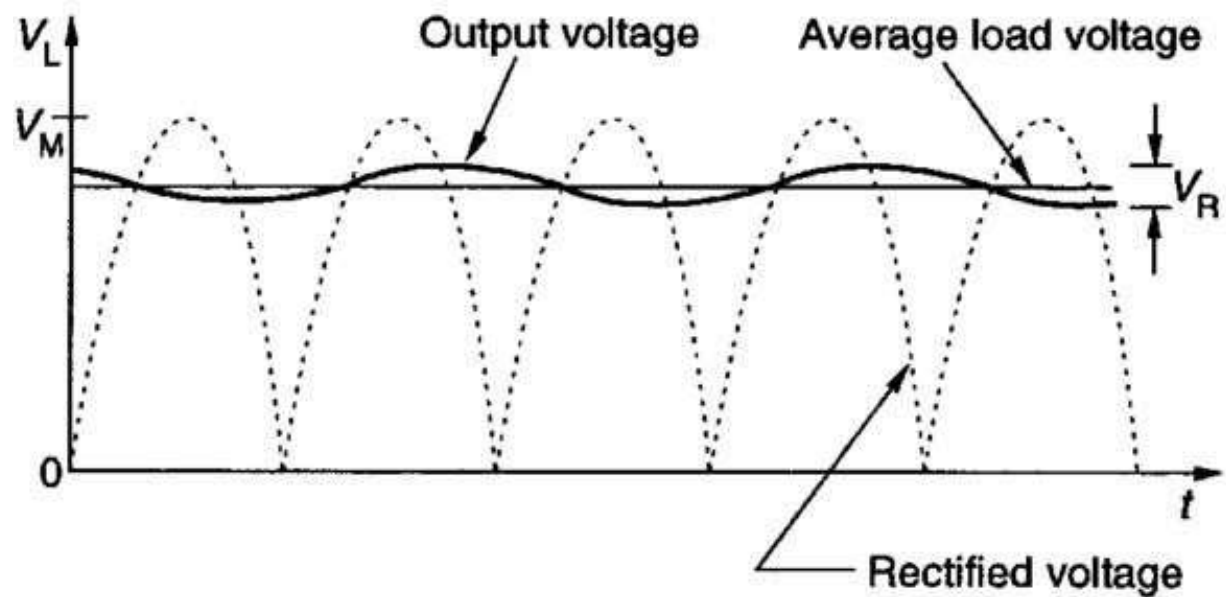


(a) Capacitor filter on light load

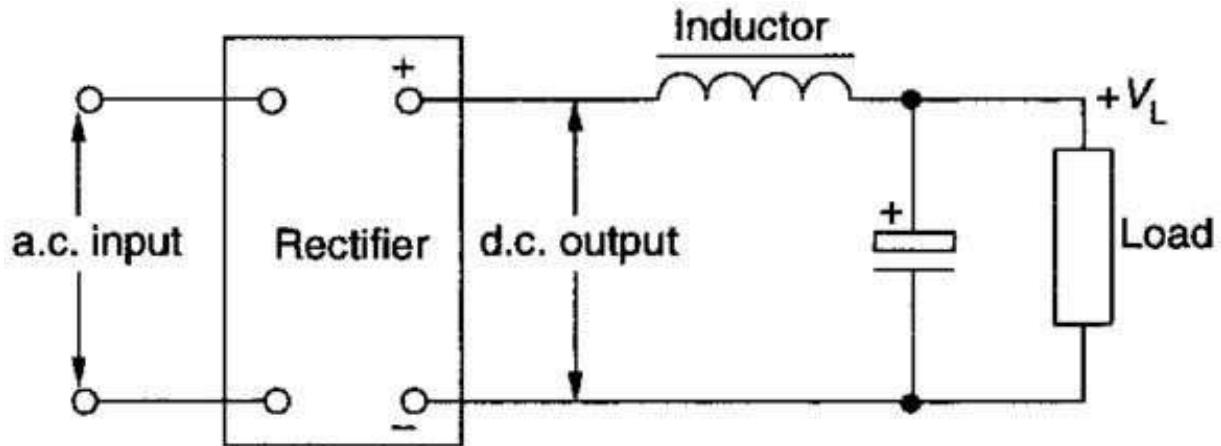
# Inductor filter



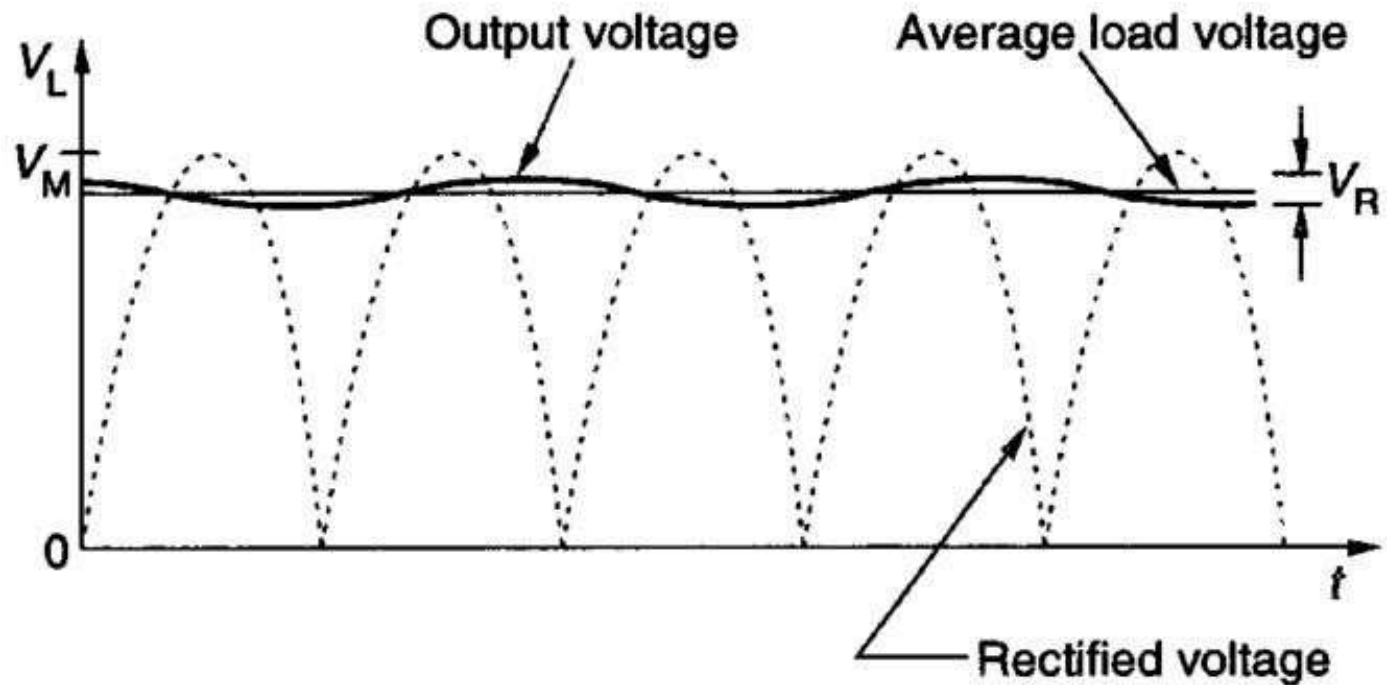
# Inductor filter output voltage waveforms



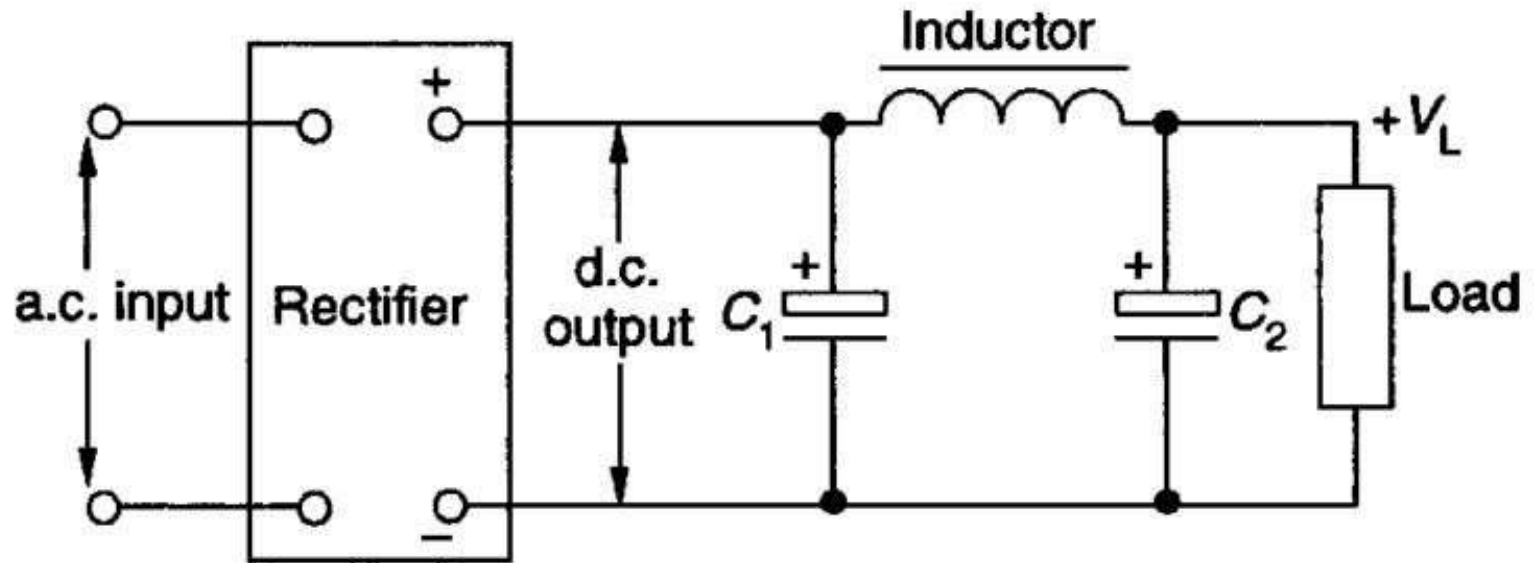
# Choke input filter (L-section filter)



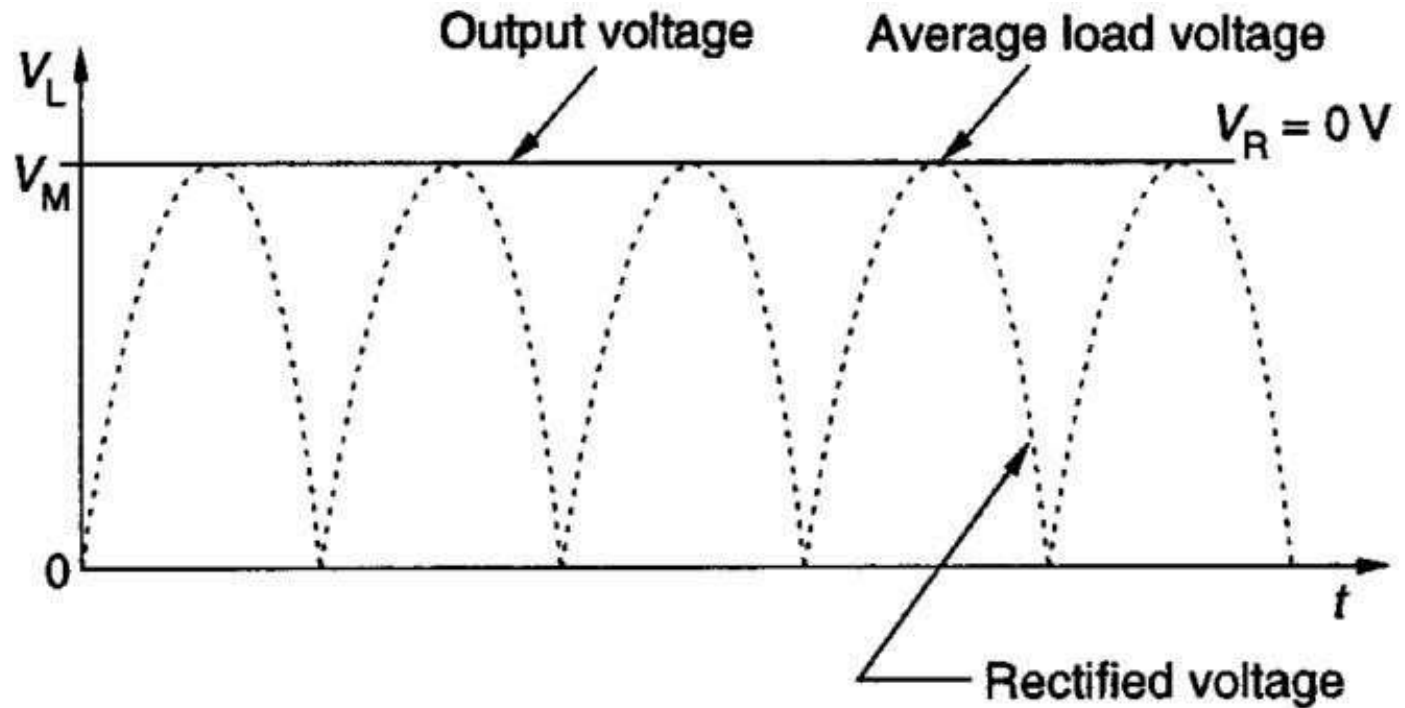
# Choke input filter load voltage waveforms



# $\pi$ -type filter

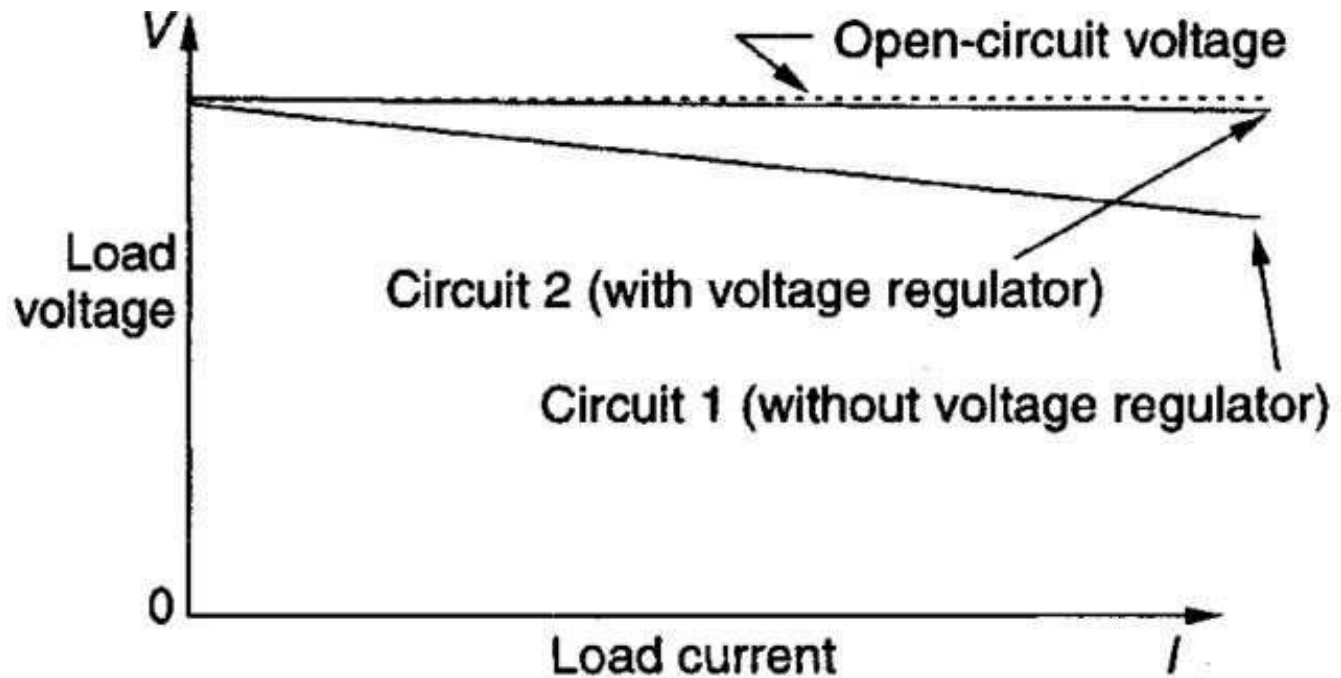


# $\pi$ -type filter output voltage waveforms



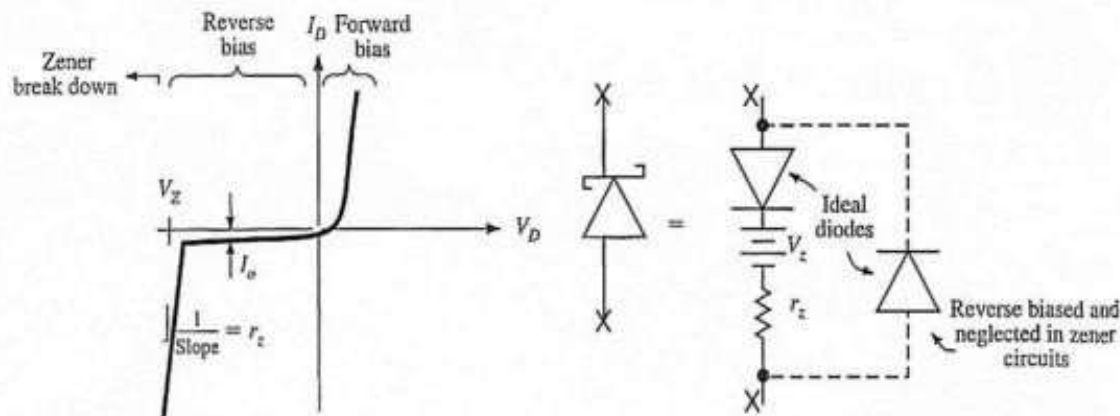


# Load characteristics for circuits with and without voltage regulators

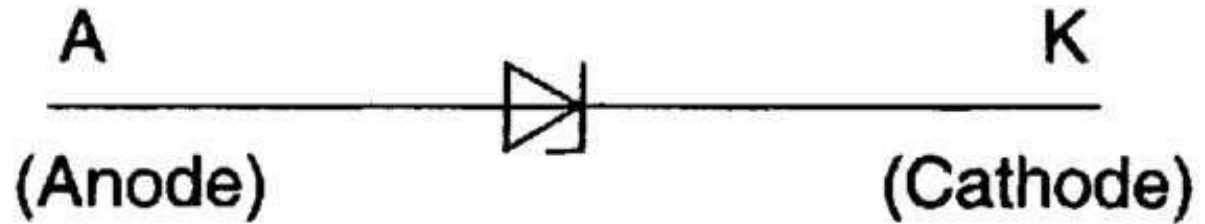


# Zener Diode

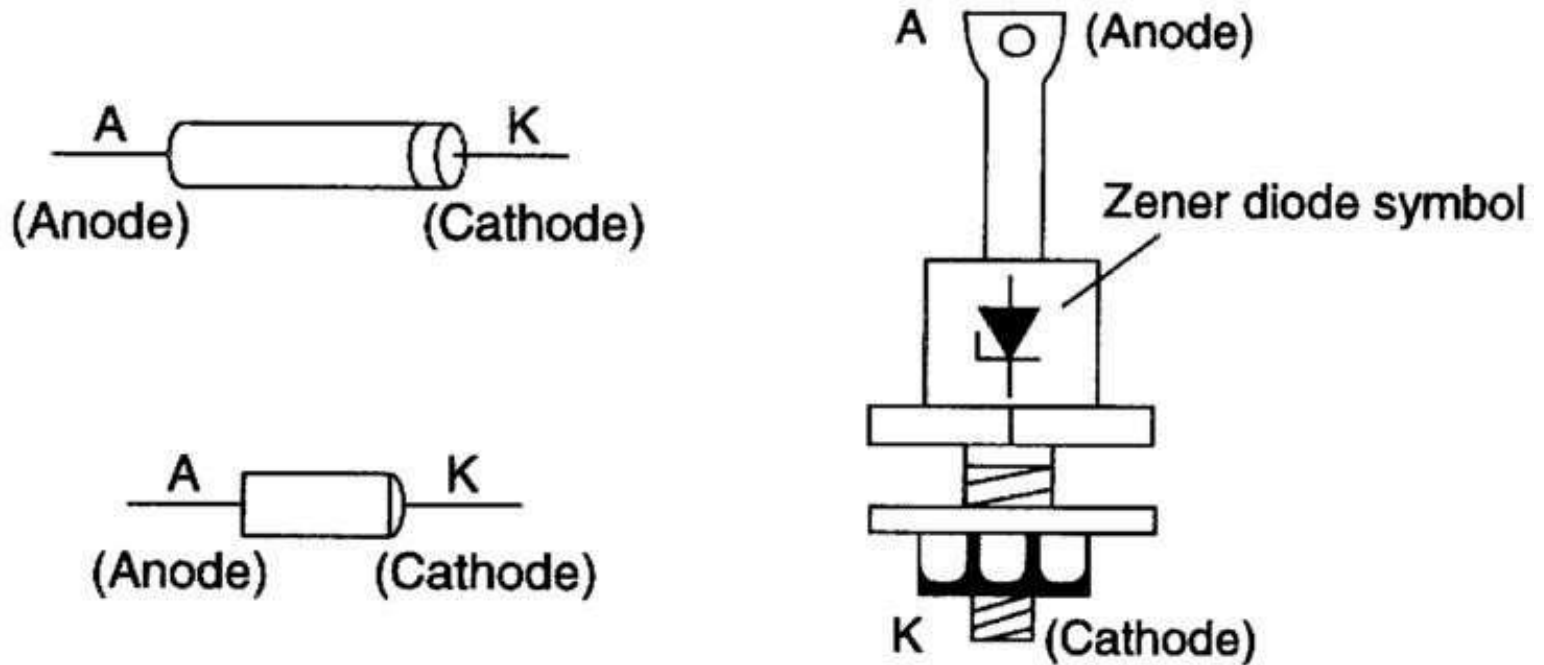
- Analyzing a diode operating in the reverse bias region will show that the current through it remains essentially constant until the *breakdown voltage*, also called the *avalanche* or *zener breakdown voltage*, is reached. At this point the current will increase very rapidly for a small voltage change.



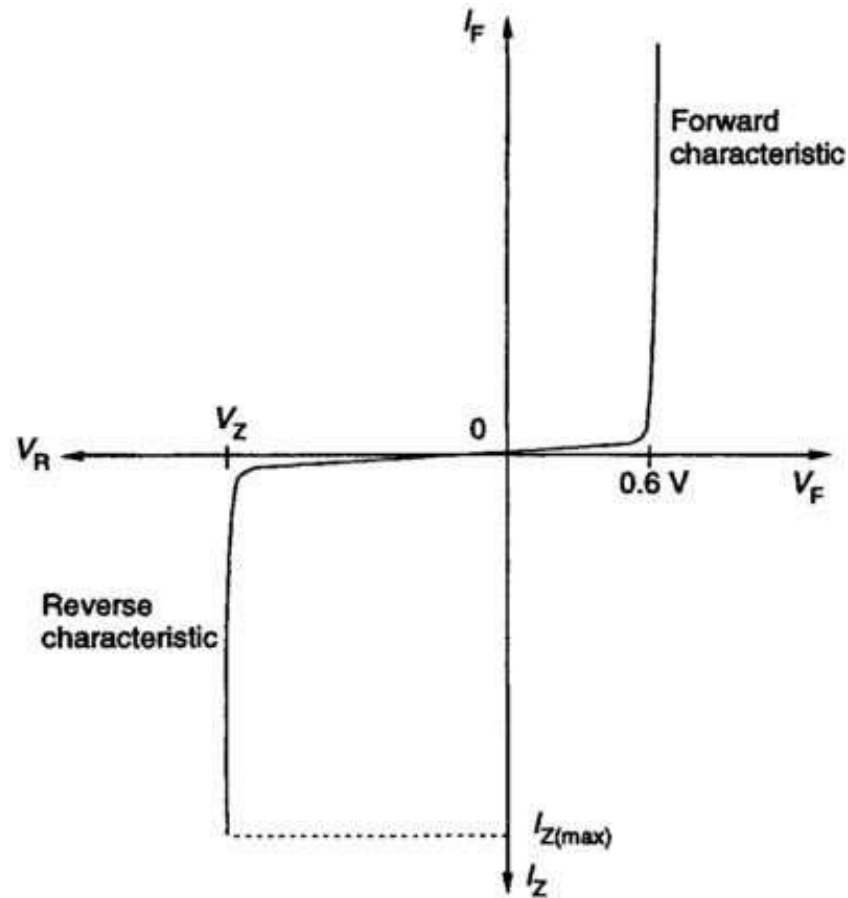
# Zener diode symbol



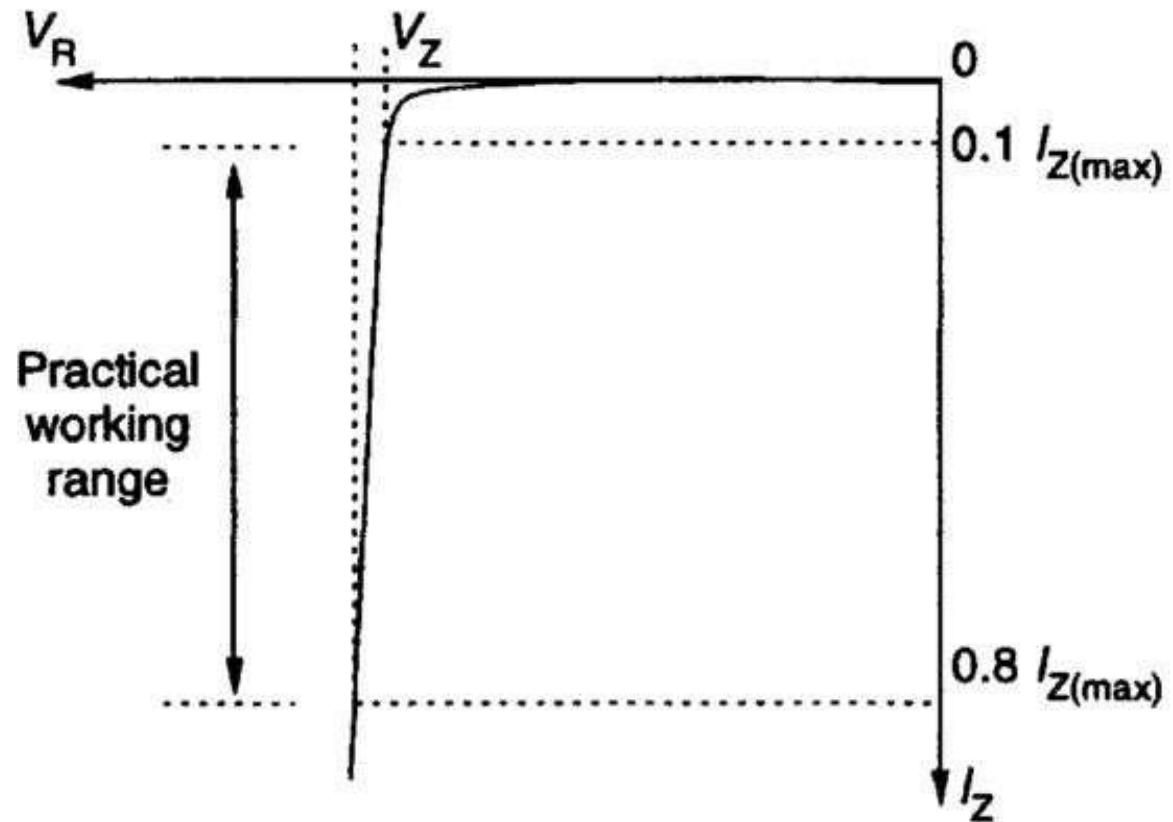
# Zener diode terminal identification



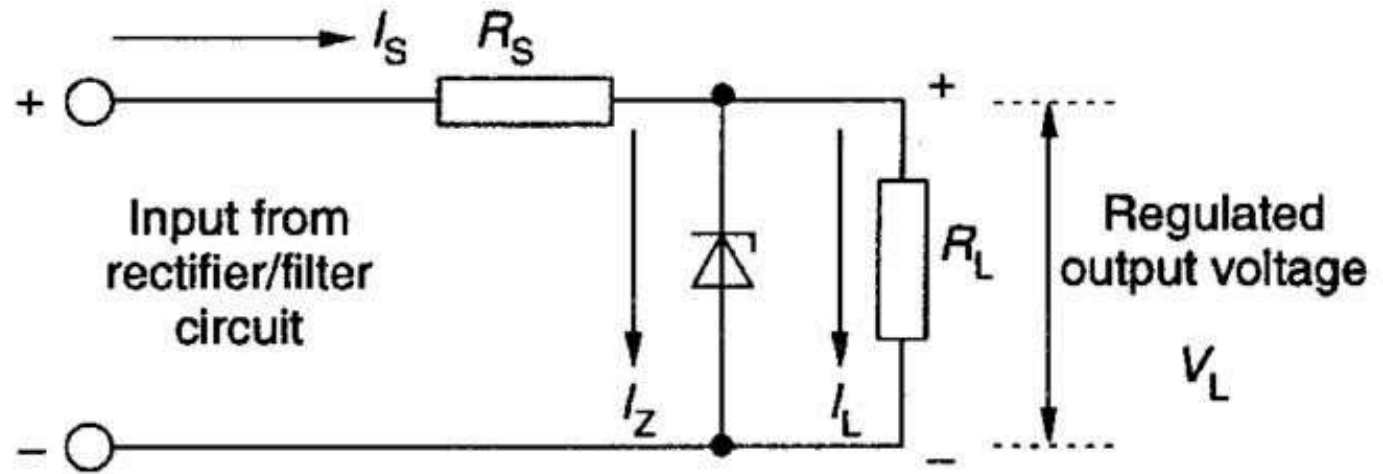
# Zener diode V-I characteristics



# Zener diode reverse-characteristic working range of currents



# Zener diode shunt regulator

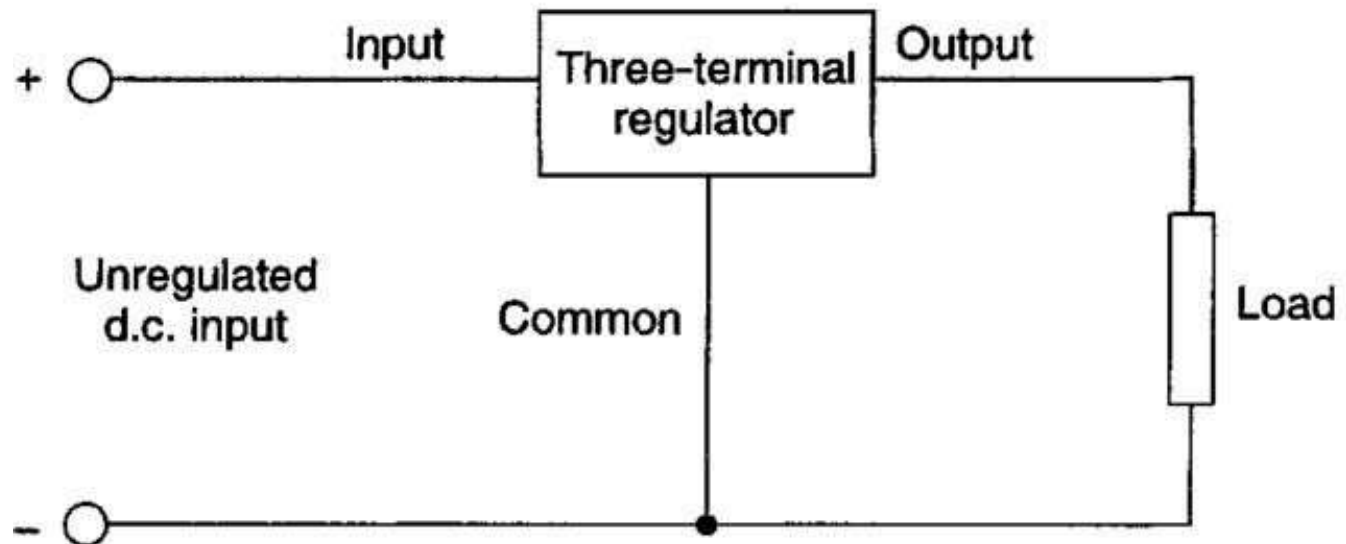


# Voltage Regulation

- This characteristic of the zener diode is very useful for voltage regulation circuits. The zener diode provides an effective way to clamp or limit the voltage at a relatively constant value thus creating a voltage regulation capability.



# Three-terminal integrated circuit regulator—basic circuit



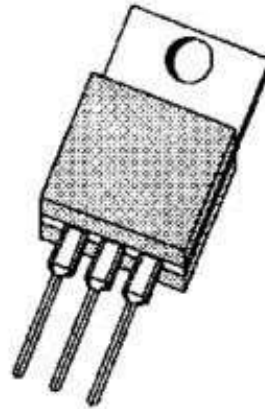
# Three-terminal regulator case styles



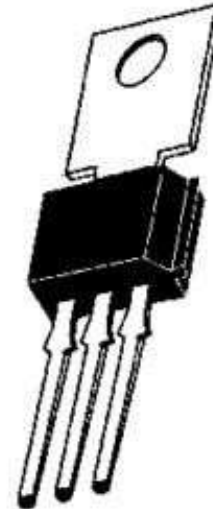
(a) TO-92



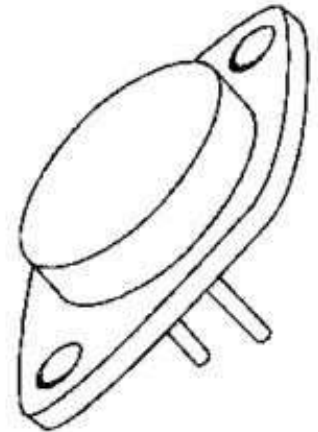
(b) TO-39



(c) TO-202

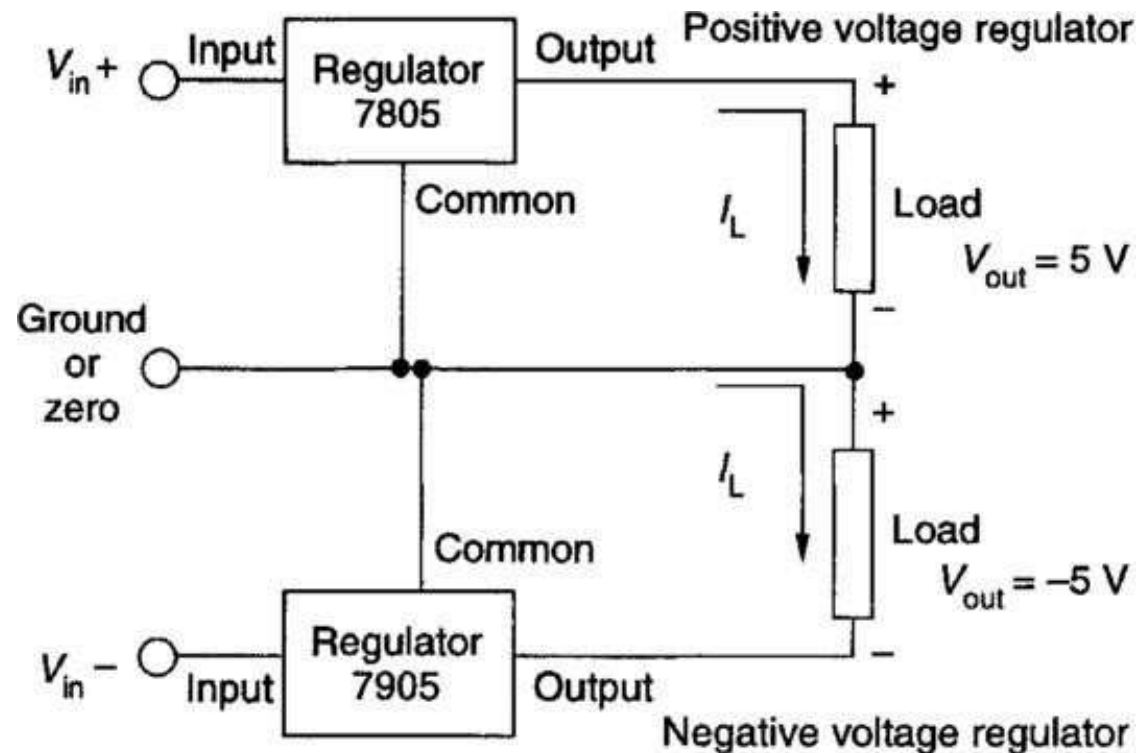


(d) TO-220



(e) TO-3

# Three-terminal regulator connections—positive and negative regulators



## Unit-2

# TRANSISTOR CHARACTERISTICS

# Introduction

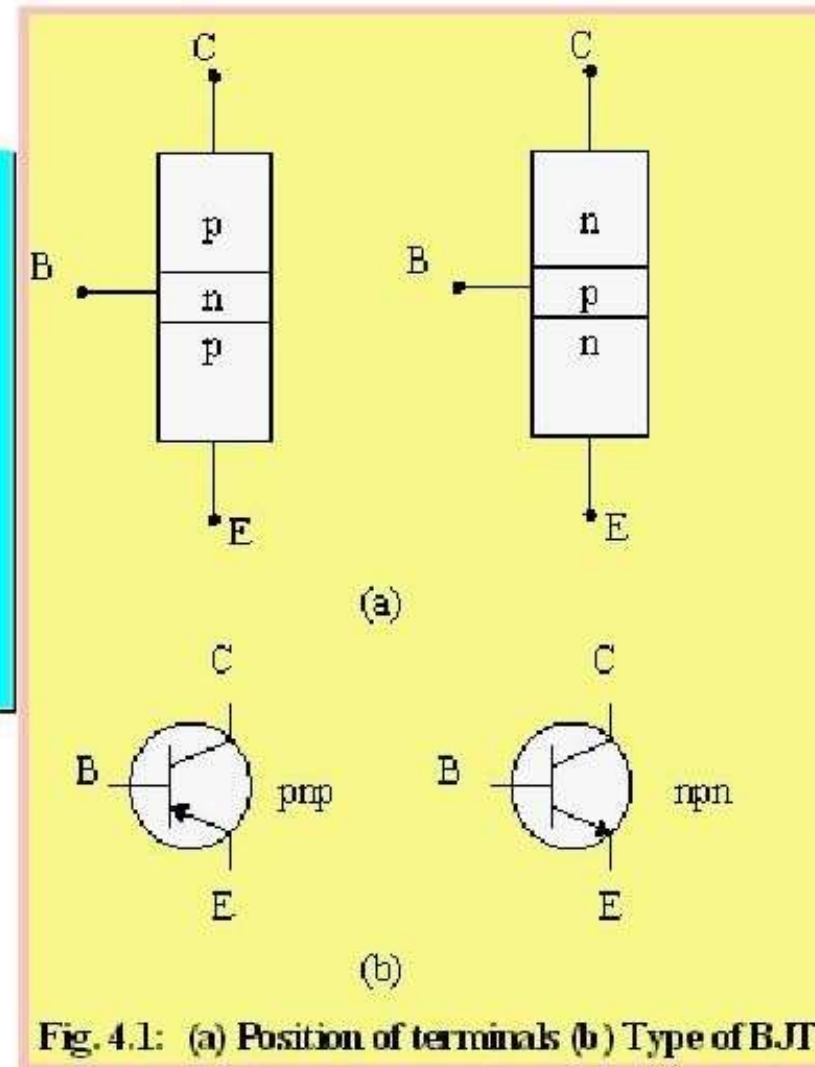
- The basic of electronic system nowadays is semiconductor device.
- The famous and commonly use of this device is BJTs (Bipolar Junction Transistors).
- It can be use as amplifier and logic switches.
- BJT consists of three terminal:
  - collector : C
  - base : B
  - emitter : E
- Two types of BJT : pnp and npn

# Transistor Construction

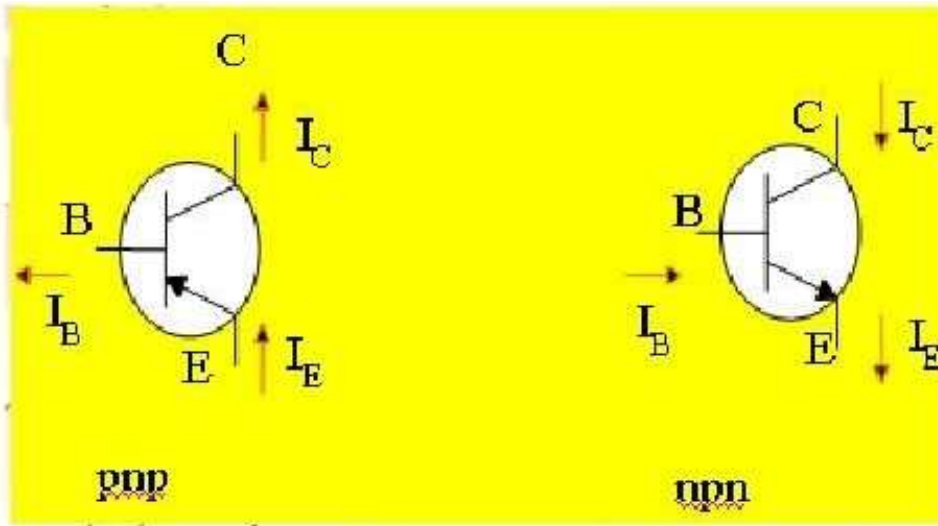
- 3 layer semiconductor device consisting:
  - 2 n- and 1 p-type layers of material • npn transistor
  - 2 p- and 1 n-type layers of material • pnp transistor
- The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material
- A single pn junction has two different types of bias:
  - forward bias
  - reverse bias
- Thus, a two-pn-junction device has four types of bias.

# Position of the terminals and symbol of BJT.

- Base is located at the middle and more thin from the level of collector and emitter
- The emitter and collector terminals are made of the same type of semiconductor material, while the base of the other type of material



# Transistor currents



$I_C$  = the collector current

$I_B$  = the base current

$I_E$  = the emitter current

-The arrow is always drawn on the emitter

-The arrow always point toward the n-type

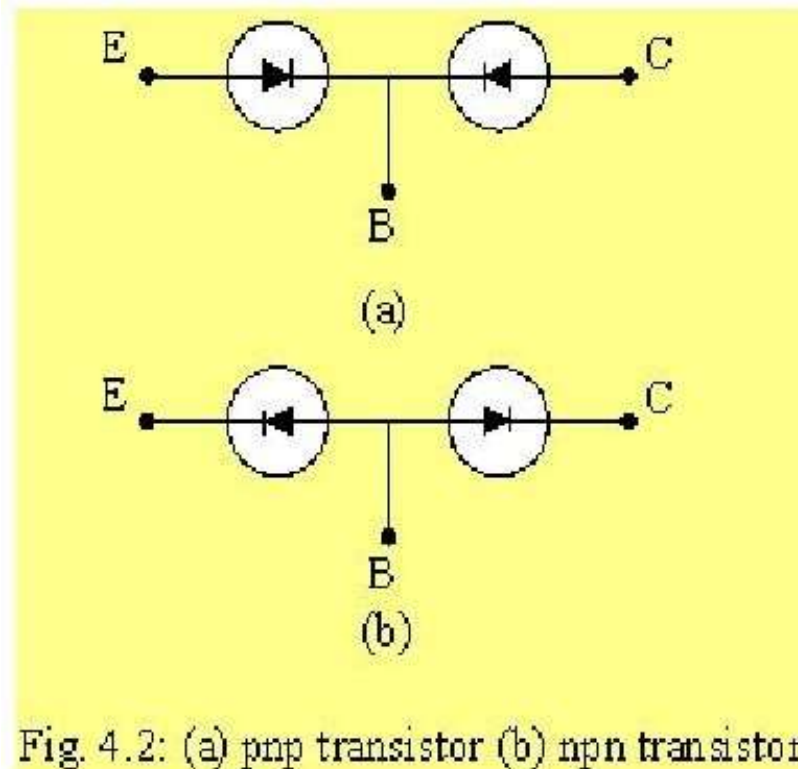
-The arrow indicates the direction of the emitter current:

pnp:  $E \rightarrow B$

npn:  $B \rightarrow E$

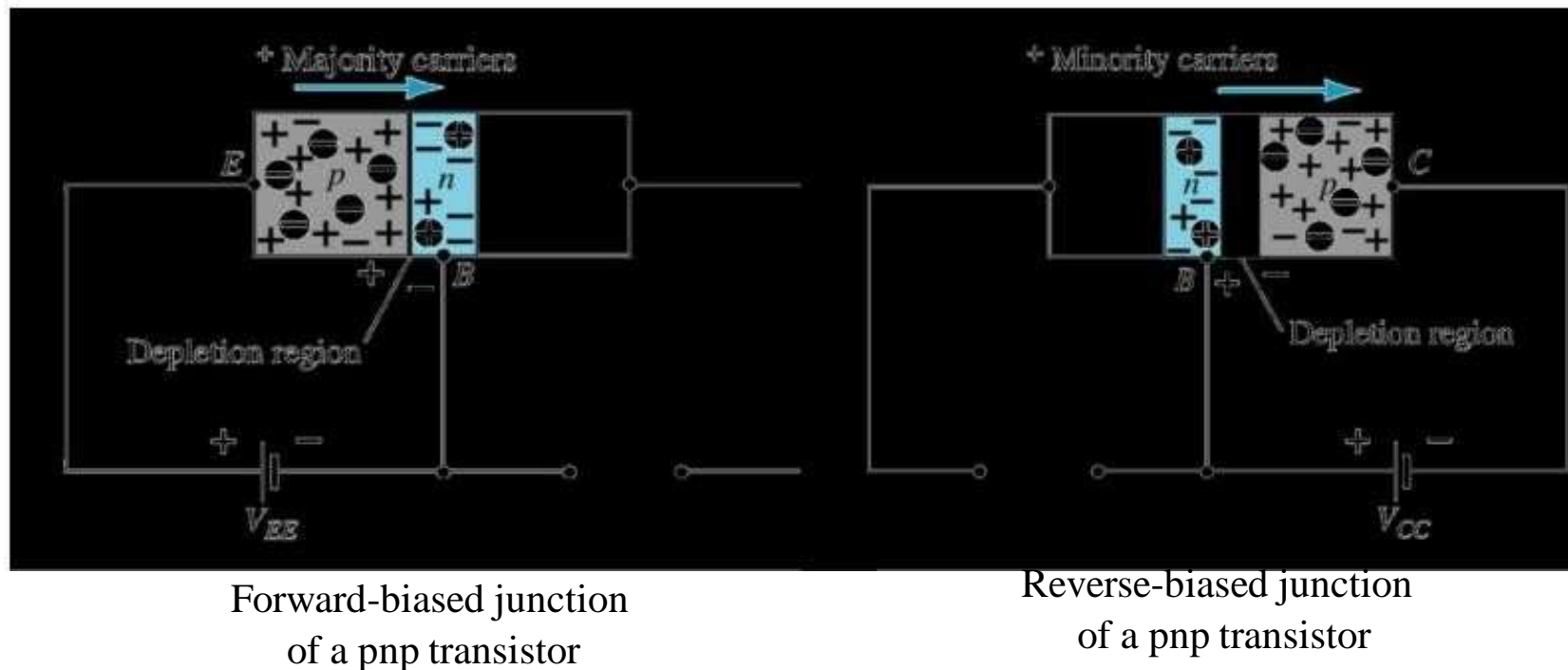


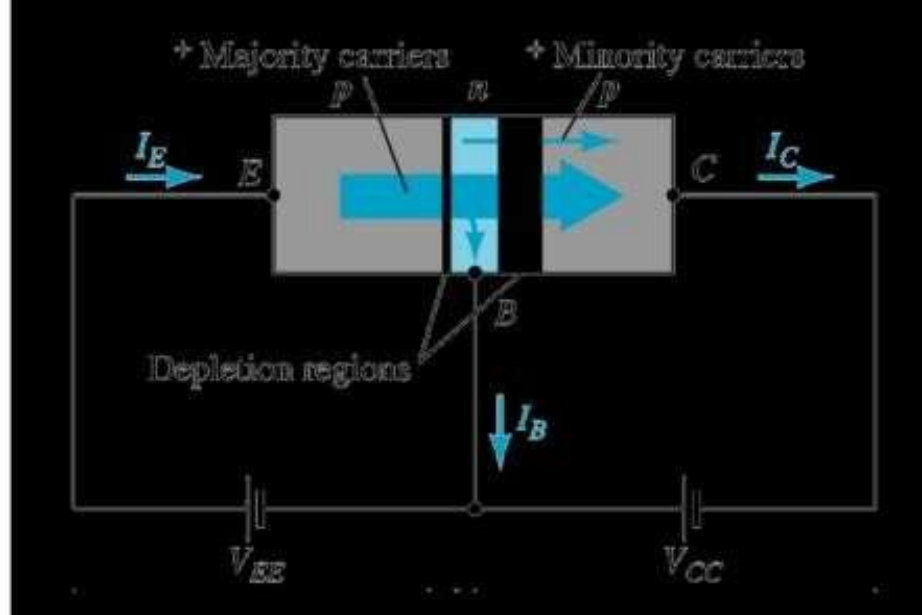
- By imaging the analogy of diode, transistor can be construct like two diodes that connetecd together.
- It can be conclude that the work of transistor is base on work of diode.



# Transistor Operation

- The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.
- One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.





- Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.
- Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.
- A very small number of carriers (+) will through n-type material to the base terminal. Resulting  $I_B$  is typically in order of microamperes.
- The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal.

- Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material.
- Applying KCL to the transistor :

$$I_E = I_C + I_B$$

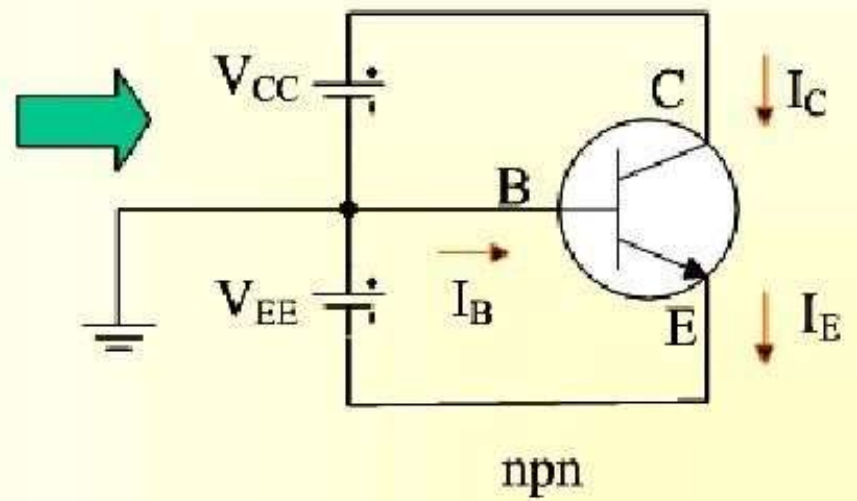
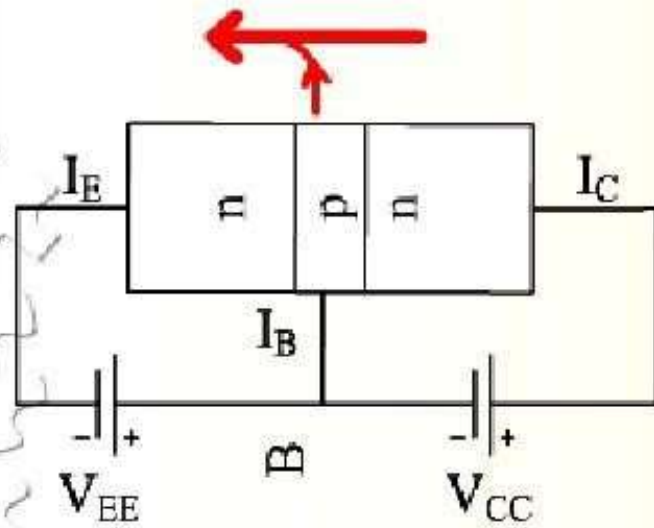
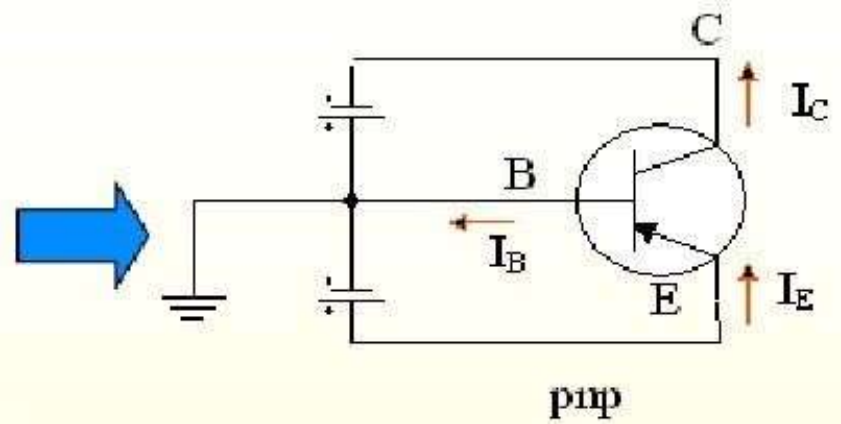
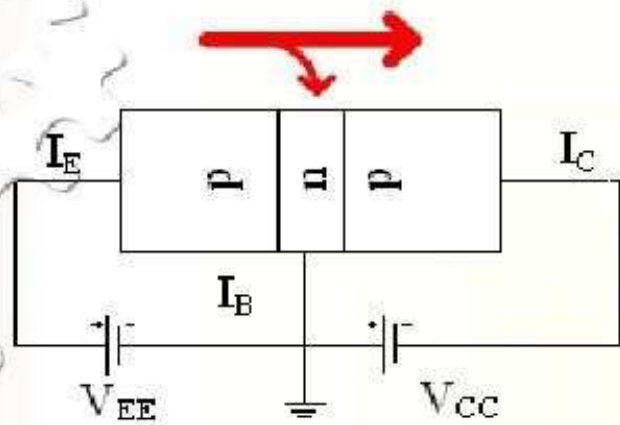
- The comprises of two components - the majority and minority carriers

$$I_C = I_{C_{majority}} + I_{C_{Ominority}}$$

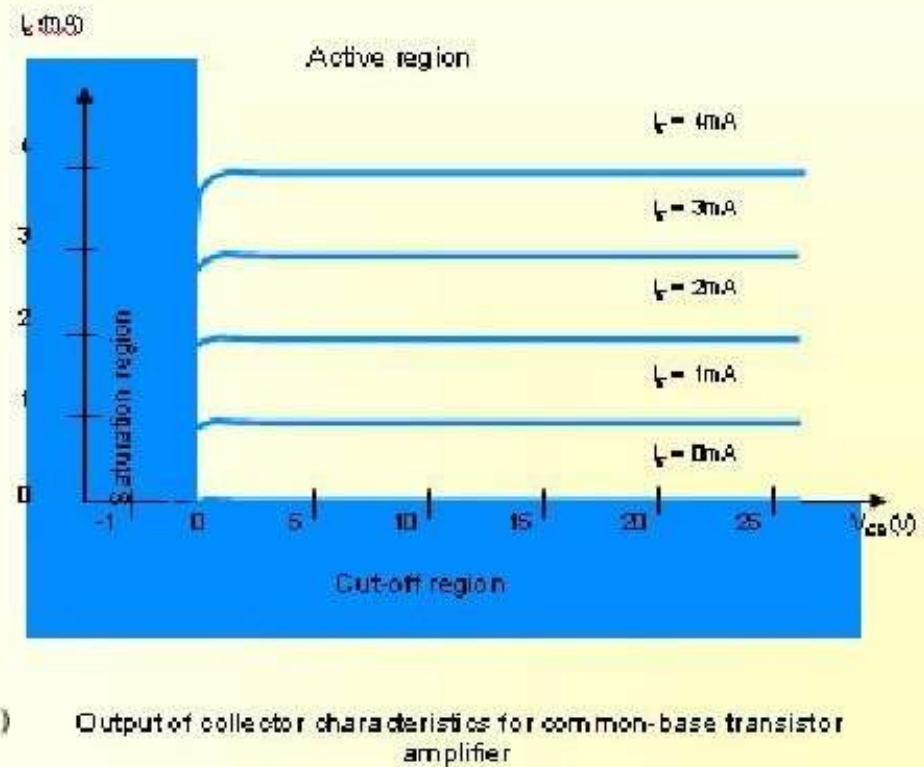
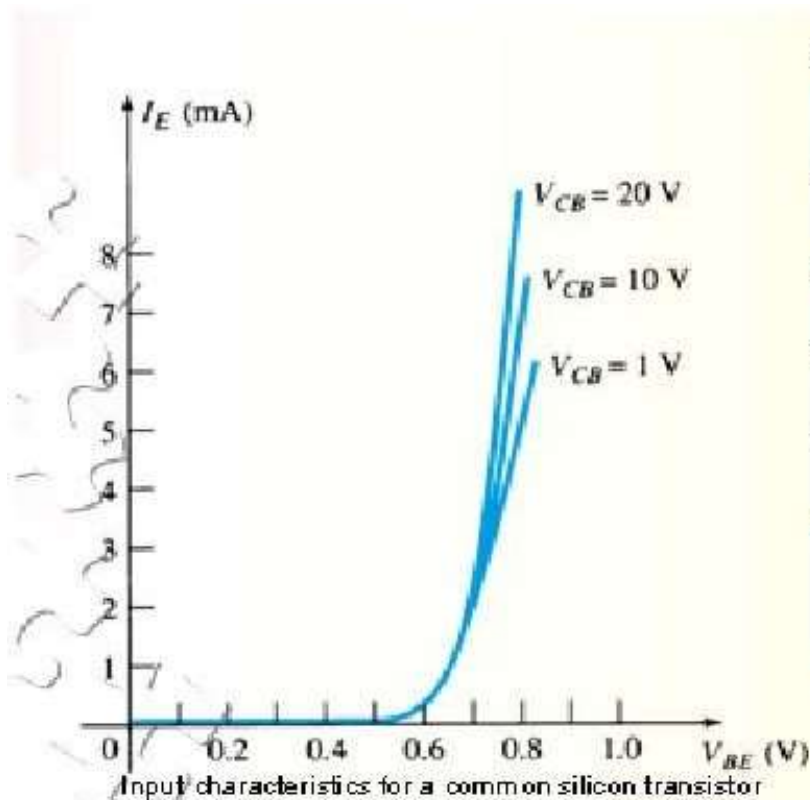
- $I_{CO}$  -  $I_C$  current with emitter terminal open and is called leakage current.

# Common-Base Configuration

- Common-base terminology is derived from the fact that the :-  
base is common to both input and output of the  
configuration.
  - base is usually the terminal closest to or at  
ground potential.
- All current directions will refer to **conventional** (hole) flow and  
the arrows in all electronic symbols have a direction defined by  
this convention.
- Note that the applied **biasing** (voltage sources) are such as to  
establish current in the direction indicated for each branch.



- To describe the behavior of common-base amplifiers requires two set of characteristics:
  - Input or driving point characteristics.
  - Output or collector characteristics
- The output characteristics has 3 basic regions:
  - Active region -defined by the biasing arrangements
  - Cutoff region - region where the collector current is 0A
  - Saturation region- region of the characteristics to the left of  $V_{CB} = 0V$



Active region	Saturation region	Cut-off region
<ul style="list-style-type: none"> <li>• <math>I_E</math> increased, <math>I_C</math> increased</li> <li>• BE junction forward bias and CB junction reverse bias</li> <li>• Refer to the graf, <math>I_C \approx I_E</math></li> <li>• <math>I_C</math> not depends on <math>V_{CB}</math></li> <li>• Suitable region for the transistor working as amplifier</li> </ul>	<ul style="list-style-type: none"> <li>• BE and CB junction is forward bias</li> <li>• Small changes in <math>V_{CB}</math> will cause big different to <math>I_C</math></li> <li>• The allocation for this region is to the left of <math>V_{CB} = 0 \text{ V}</math>.</li> </ul>	<ul style="list-style-type: none"> <li>• Region below the line of <math>I_E = 0 \text{ A}</math></li> <li>• BE and CB is reverse bias</li> <li>• no current flow at collector, only leakage current</li> </ul>

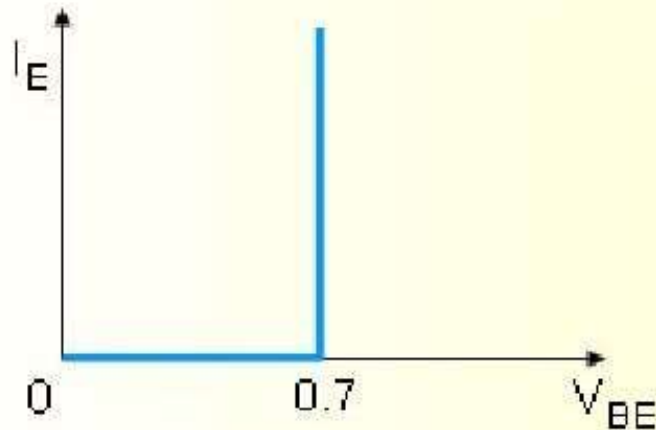


- The curves (output characteristics) clearly indicate that a first approximation to the relationship between  $I_E$  and  $I_C$  in the active region is given by

$$I_C \approx I_E$$

- Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to be

$$V_{BE} = 0.7V$$



- In the dc mode the level of  $I_C$  and  $I_E$  due to the majority carriers are related by a quantity called alpha

$$a = \frac{I_C}{I_E}$$

$$I_C = aI_E + I_{CBO}$$

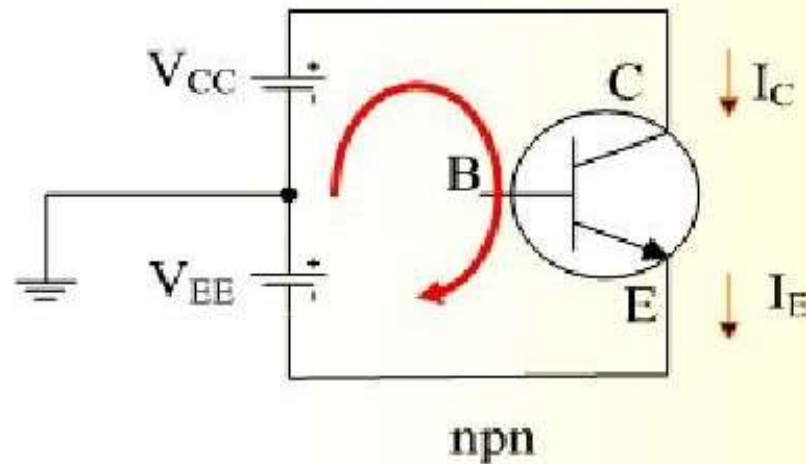
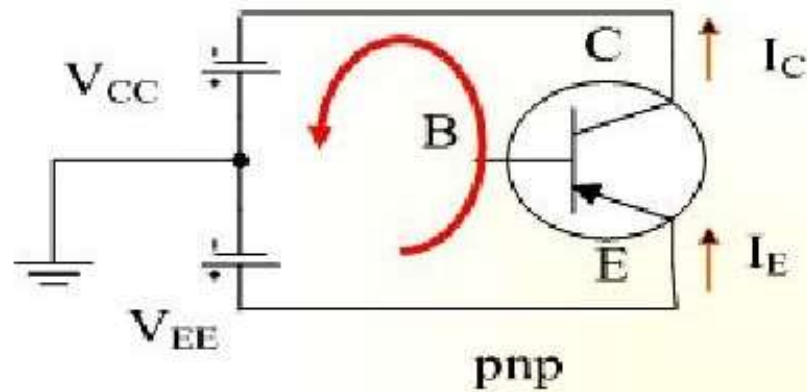
- It can then be summarize to  $I_C = aI_E$  (ignore  $I_{CBO}$  due to small value)
- For ac situations where the point of operation moves on the characteristics curve, an ac alpha defined by

$$a = \frac{D I_C}{D I_E}$$

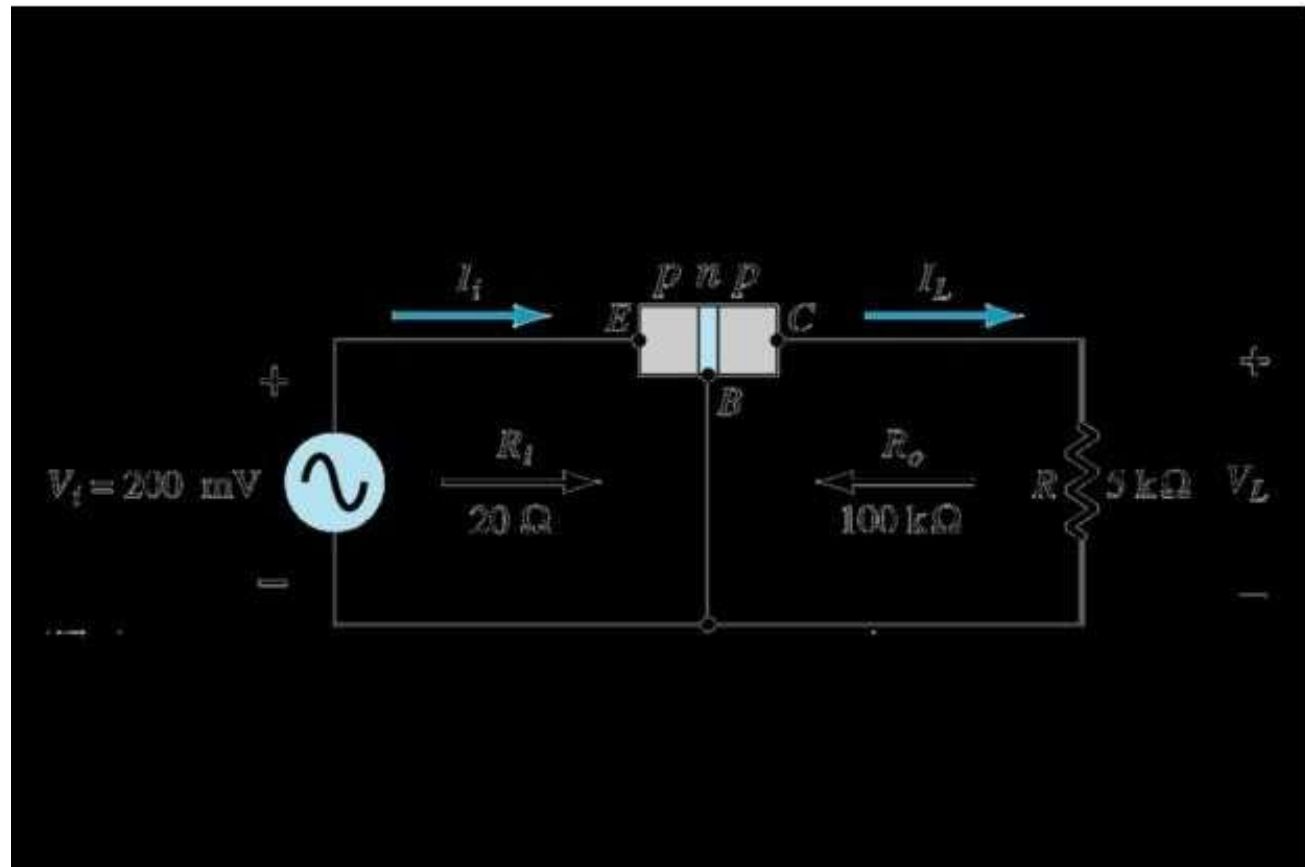
- Alpha a **common base current gain factor** it shows the efficiency by calculating the current percent from current flow from emitter to collector. The value of  $a$  is typical from 0.9 ~ 0.998.

# Biasing

- Proper biasing CB configuration in active region by approximation  $I_C \approx I_E$  ( $I_B \approx 0 \mu A$ )



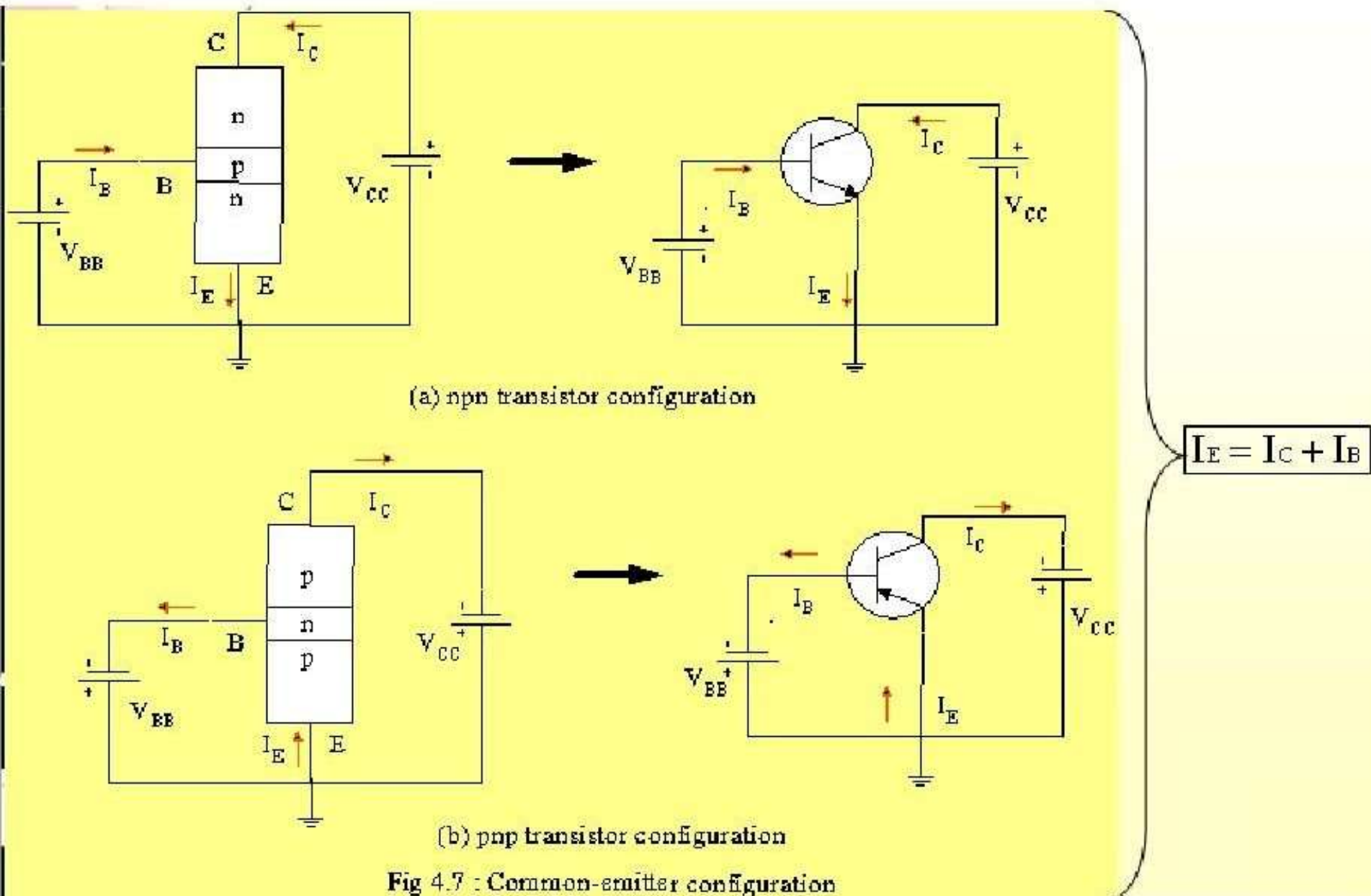
# Transistor as an amplifier

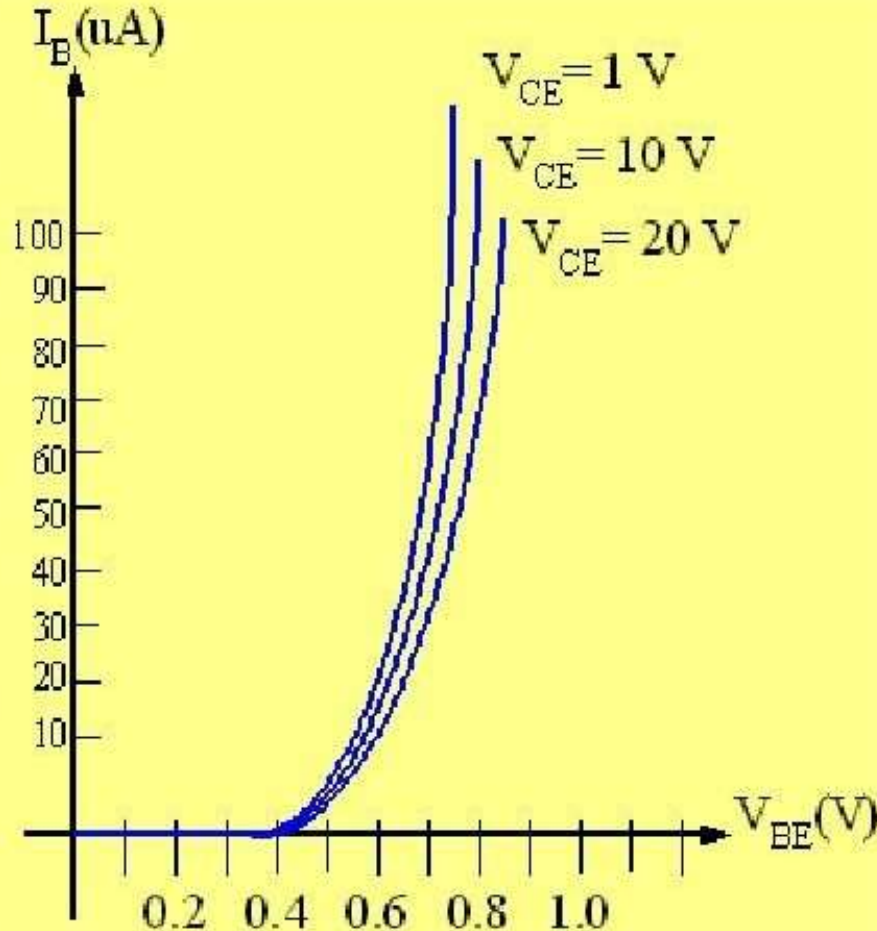


# Common-Emitter Configuration

- It is called common-emitter configuration since :
  - emitter is common or reference to both input and output terminals.
  - emitter is usually the terminal closest to or at ground potential.
- Almost amplifier design is using connection of CE **due to the high gain for current and voltage**
- Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters.

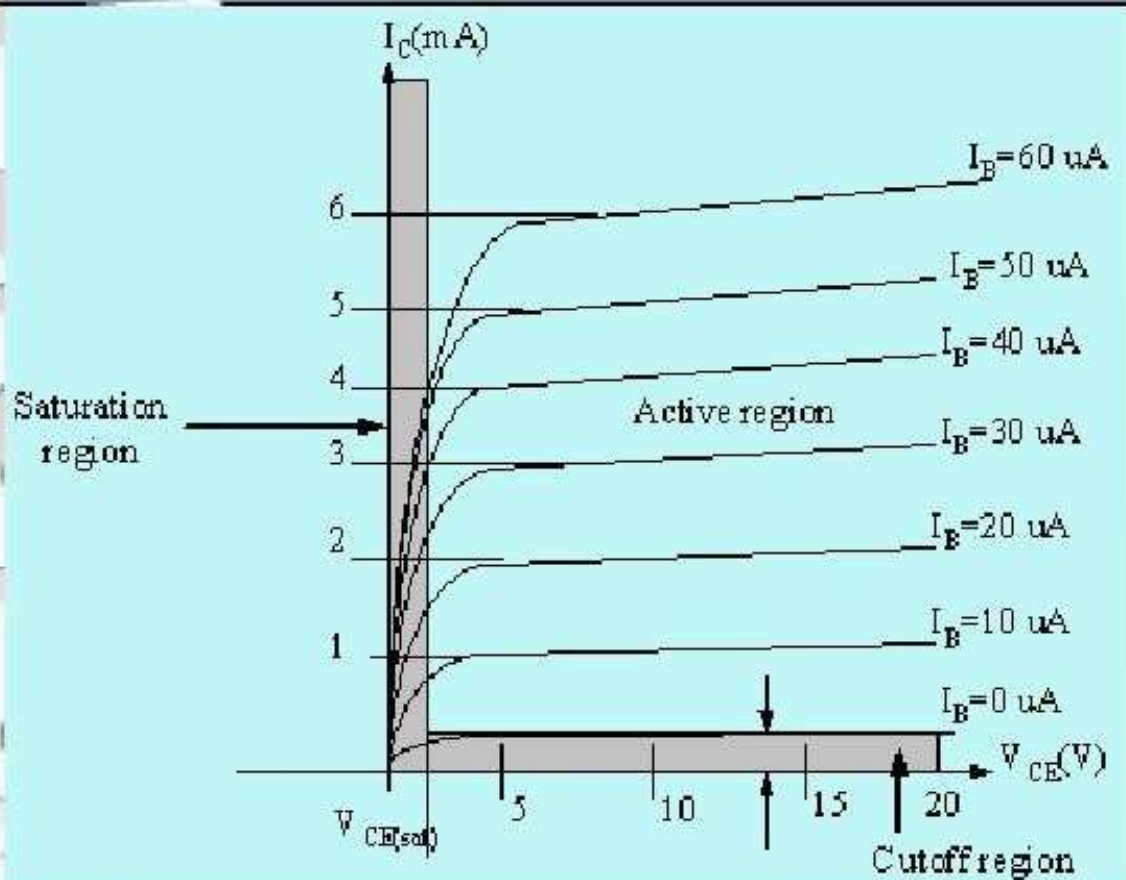
## Proper Biasing common-emitter configuration in active region





- $I_B$  is microamperes compared to milliamperes of  $I_C$ .
- $I_B$  will flow when  $V_{BE} > 0.7$  V for silicon and 0.3 V for germanium
- Before this value  $I_B$  is very small and no  $I_B$ .
- Base-emitter junction is forward bias
- Increasing  $V_{CE}$  will reduce  $I_B$  for different values.

Input characteristics for a  
common emitter NPN transistor

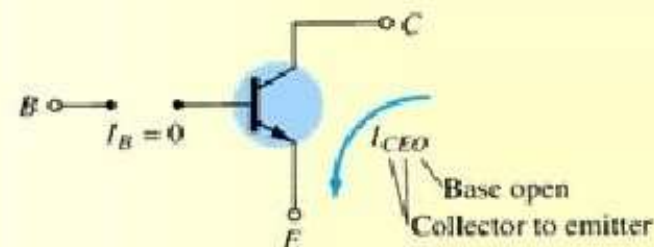
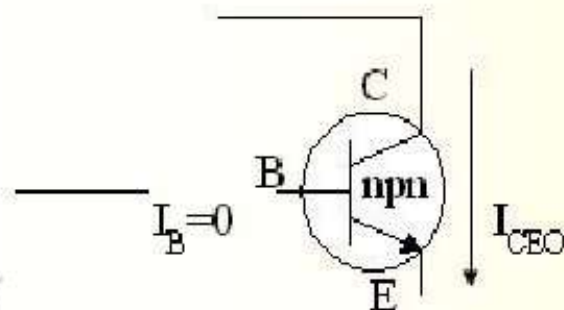


Output characteristics for a common-emitter npn transistor

- For small  $V_{CE}$  ( $V_{CE} < V_{CE(sat)}$ ,  $I_C$  increase linearly with increasing of  $V_{CE}$
- $V_{CE} > V_{CE(sat)}$   $I_C$  not totally depends on  $V_{CE}$  • constant  $I_C$
- $I_B(\mu A)$  is very small compare to  $I_C$  (mA). Small increase in  $I_B$  cause big increase in  $I_C$
- $I_B = 0 A$  •  $I_{CEO}$  occur.
- Noticing the value when  $I_C = 0 A$ . There is still some value of current flows.



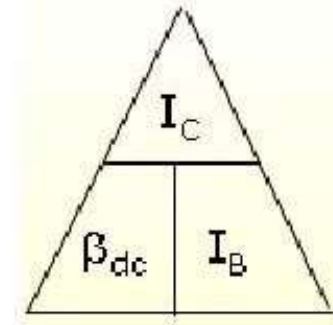
Active region	Saturation region	Cut-off region
<ul style="list-style-type: none"> <li>• B-E junction is forward bias</li> <li>• C-B junction is reverse bias</li> <li>• can be employed for voltage, current and power amplification</li> </ul>	<ul style="list-style-type: none"> <li>• B-E and C-B junction is forward bias, thus the values of <math>I_B</math> and <math>I_C</math> is too big.</li> <li>• The value of <math>V_{CE}</math> is so small.</li> <li>• Suitable region when the transistor as a logic switch.</li> <li>• NOT and avoid this region when the transistor as an amplifier.</li> </ul>	<ul style="list-style-type: none"> <li>• region below <math>I_B=0\mu A</math> is to be avoided if an undistorted o/p signal is required</li> <li>• B-E junction and C-B junction is reverse bias</li> <li>• <math>I_B=0</math>, <math>I_C</math> not zero, during this condition <math>I_C=I_{CEO}</math> where is this current flow when B-E is reverse bias.</li> </ul>



# Beta ( $\beta$ ) or amplification factor

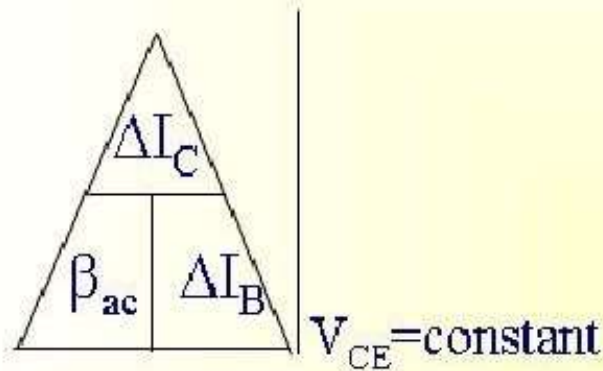
- The ratio of dc collector current ( $I_C$ ) to the dc base current ( $I_B$ ) is dc beta ( $\beta_{dc}$ ) which is dc current gain where  $I_C$  and  $I_B$  are determined at a particular operating point, Q-point (quiescent point).
- It's define by the following equation:

$$30 < \beta_{dc} < 300 \quad \text{for 2N3904}$$



- On data sheet,  $\beta_{dc}$  and  $\beta_{ac}$  are derived from ac hybrid equivalent cct.  $\beta_{dc}$  are derived from forward-current amplification and common-emitter configuration respectively.

- For ac conditions an ac beta has been defined as the changes of collector current ( $I_C$ ) compared to the changes of base current ( $I_B$ ) where  $I_C$  and  $I_B$  are determined at operating point.
- On data sheet,  $E_{ac}=hfe$
- It can defined by the following equation:



# Example

From output characteristics of common emitter configuration, find  $E_{ac}$  and  $E_{dc}$  with an Operating point at  $I_B = 25 \mu A$  and  $V_{CE} = 7.5V$ .

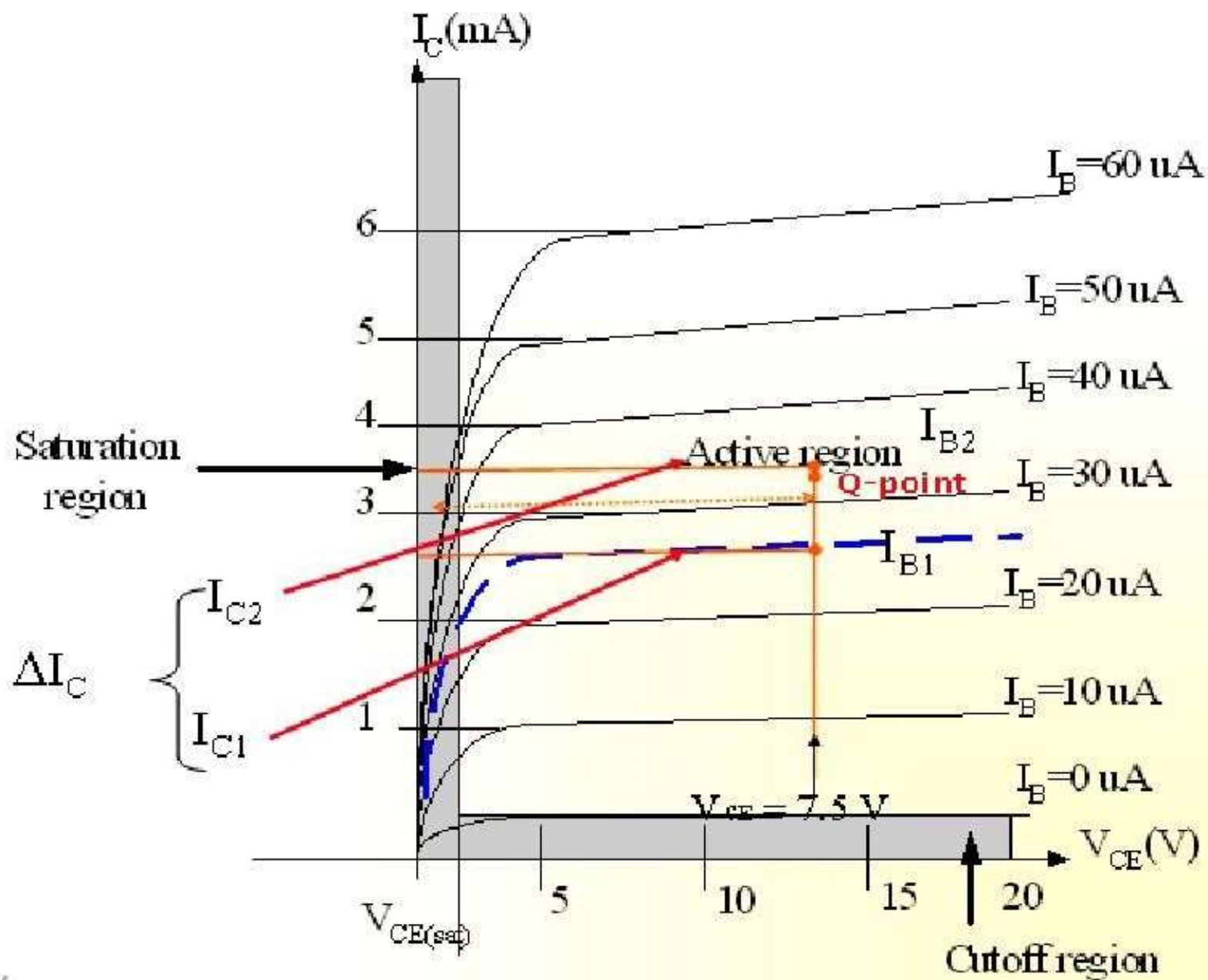
# Solution:

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \Big|_{V_{CE} = \text{constant}}$$

$$= \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} = \frac{3.2 \text{ m} - 2.2 \text{ m}}{30 \mu - 20 \mu}$$

$$= \frac{1 \text{ m}}{10 \mu} = 100$$

$$\begin{aligned} \beta_{dc} &= \frac{I_C}{I_B} \\ &= \frac{2.7 \text{ m}}{25 \mu} \\ &= \underline{\underline{108}} \end{aligned}$$



# Relationship analysis between $\alpha$ and $\beta$

CASE 1

$$I_E = I_C + I_B \quad (1)$$

substitute equ.  $I_C = \beta I_B$  into (1) we get

$$\underline{\underline{I_E = (\beta + 1)I_B}}$$

CASE 2

$$\text{known : } \alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha} \quad (2)$$

$$\text{known : } \beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta} \quad (3)$$

substitute (2) and (3) into (1) we get,

$$\underline{\underline{\alpha = \frac{\beta}{\beta + 1}}}$$

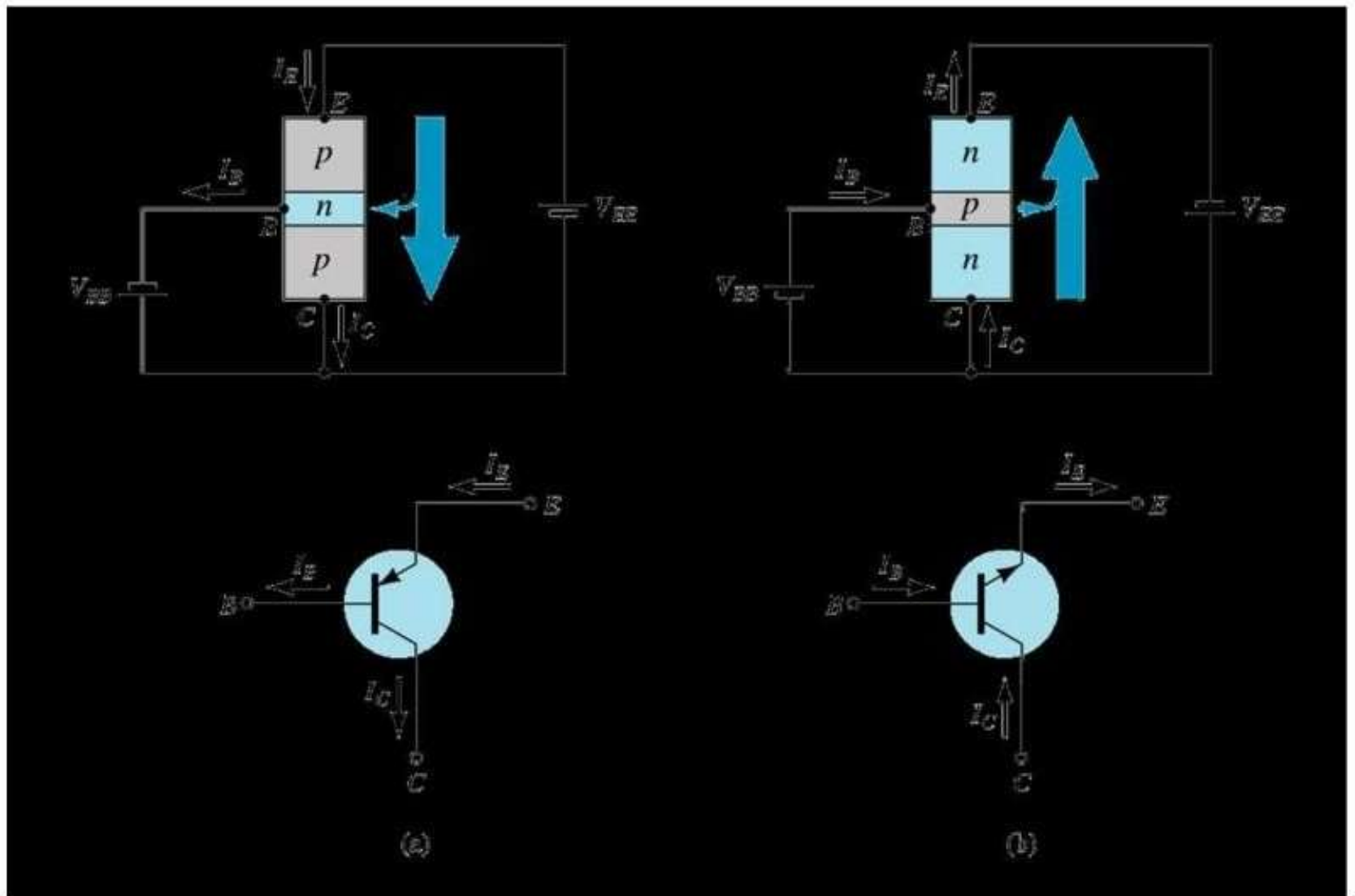
and

$$\underline{\underline{\beta = \frac{\alpha}{1 - \alpha}}}$$

# Common - Collector Configuration

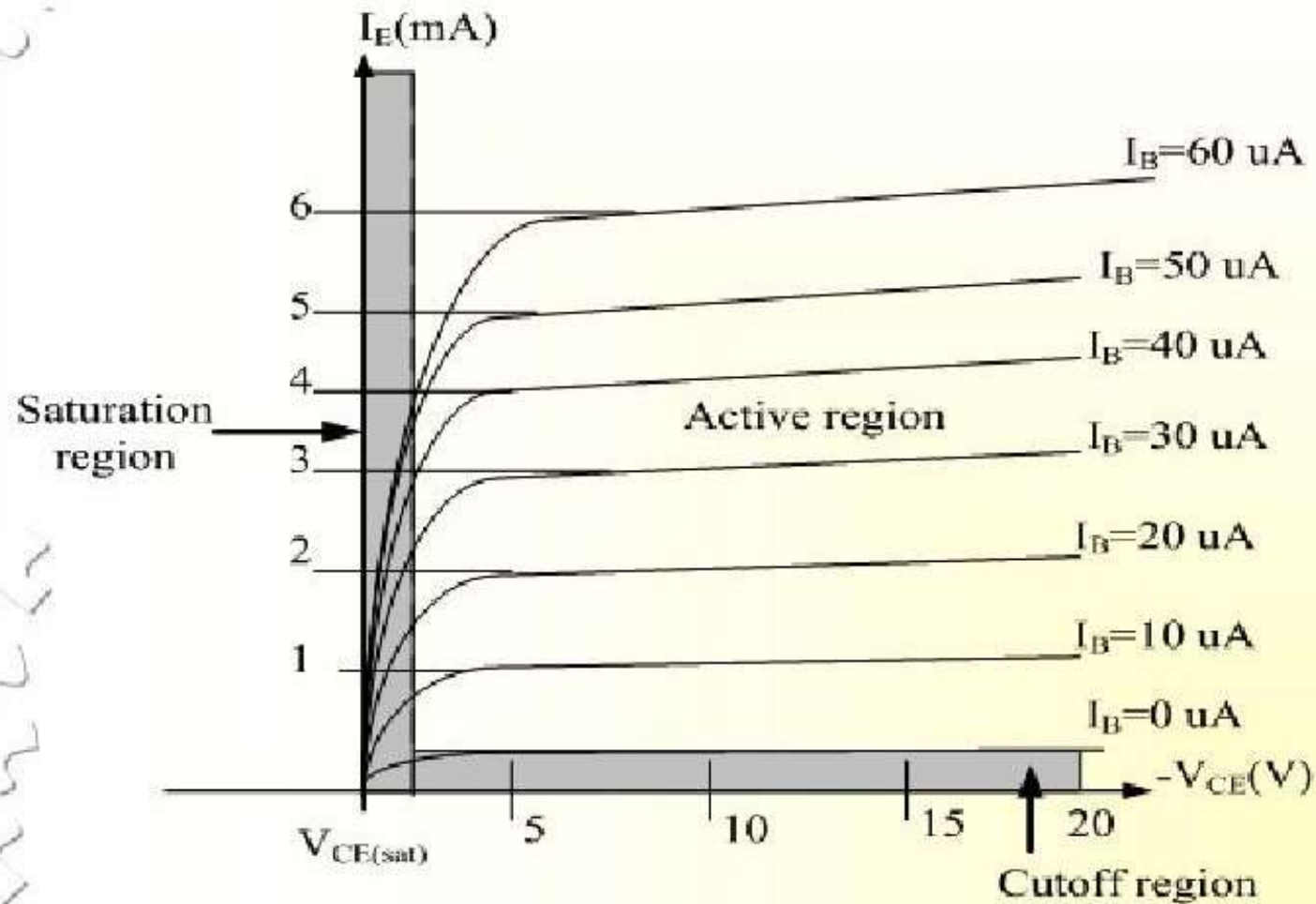
- Also called emitter-follower (EF).
- It is called common-emitter configuration since both the signal source and the load share the collector terminal as a common connection point.
- The output voltage is obtained at emitter terminal.
- The input characteristic of common-collector configuration is similar with common-emitter. configuration.
- Common-collector circuit configuration is provided with the load resistor connected from emitter to ground.
- It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.





Notation and symbols used with the common-collector configuration:  
 (a) pnp transistor ; (b) npn transistor.

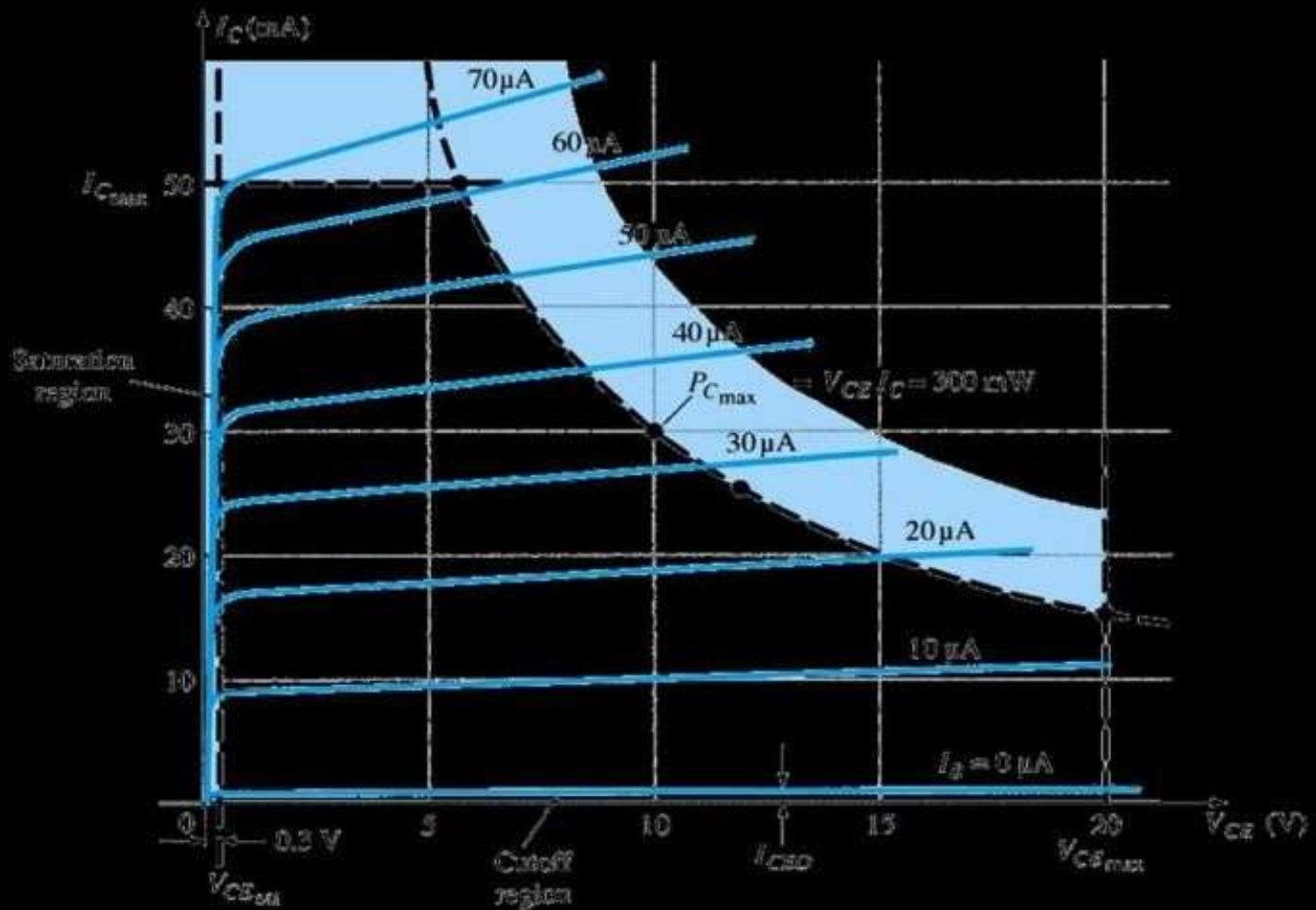
- For the common-collector configuration, the output characteristics are a plot of  $I_E$  vs  $V_{CE}$  for a range of values of  $I_B$ .



**Fig 4.9 : Output characteristic in CC configuration for npn transistor**

# Limits of Operation

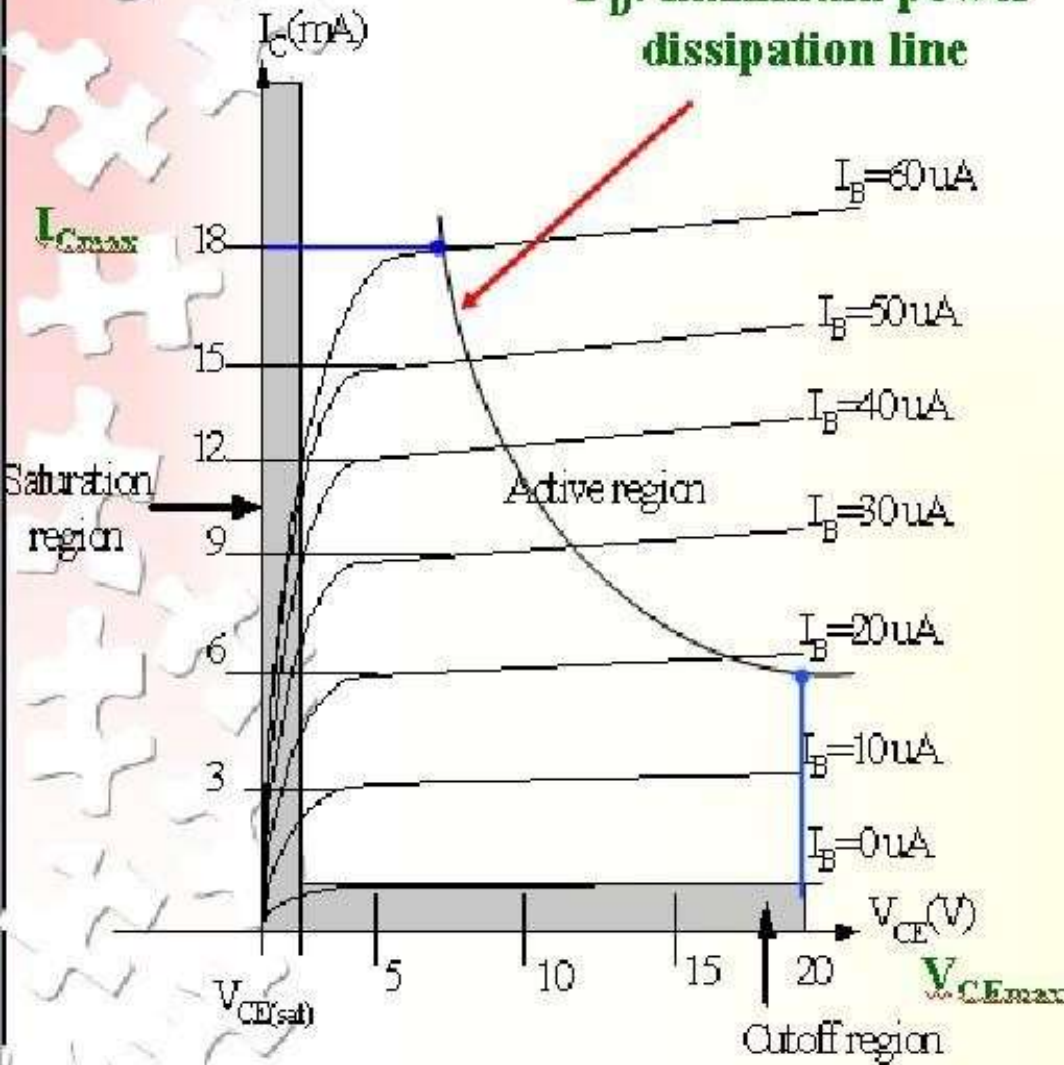
- Many BJT transistor used as an amplifier. Thus it is important to notice the limits of operations.
- At least 3 maximum values is mentioned in data sheet.
- There are:
  - a) Maximum power dissipation at collector:  $P_{Cmax}$  or  $P_D$
  - b) Maximum collector-emitter voltage:  $V_{CEmax}$  sometimes named as  $V_{BR(CEO)}$  or  $V_{CEO}$ .
  - c) Maximum collector current:  $I_{Cmax}$
- There are few rules that need to be followed for BJT transistor used as an amplifier. The rules are:
  - i) transistor need to be operate in active region!
  - ii)  $I_C < I_{Cmax}$
  - ii)  $P_C < P_{Cmax}$



Note:  $V_{CE}$  is at maximum and  $I_C$  is at minimum ( $I_{C_{max}} = I_{C_{EO}}$ ) in the cutoff region.  $I_C$  is at maximum and  $V_{CE}$  is at minimum ( $V_{CE_{max}} = V_{ce_{sat}} = V_{CEO}$ ) in the saturation region. The transistor operates in the active region between saturation and cutoff.

# Example 1:

$P_D$ : maximum power dissipation line



Refer to the fig.

Step 1:

The maximum collector power dissipation,

$$P_D = I_{Cmax} \times V_{CEmax} \quad (1)$$

$$= 18\text{m} \times 20 = 360 \text{ mW}$$

Step 2:

At any point on the characteristics the product of and must be equal to 360 mW.

Ex. 1. If choose  $I_{Cmax} = 5 \text{ mA}$ , substitute into the (1), we get

$$V_{CEmax} I_{Cmax} = 360 \text{ mW}$$

$$V_{CEmax}(5 \text{ m}) = 360/5 = \underline{7.2 \text{ V}}$$

Ex.2. If choose  $V_{CEmax} = 18 \text{ V}$ , substitute into (1), we get

$$V_{CEmax} I_{Cmax} = 360 \text{ mW}$$

$$(10) I_{Cmax} = 360\text{m}/18 = \underline{20 \text{ mA}}$$

# Derating $P_{Dmax}$

- $P_{Dmax}$  is usually specified at 25°C.
- The higher temperature goes, the less is  $P_{Dmax}$
- Example;
  - A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

# Transistor Biasing and Stabilization

# Transistor Biasing

The basic function of transistor is amplification. The process of raising the strength of weak signal without any change in its general shape is referred as faithful amplification. For faithful amplification it is essential that:-

1. Emitter-Base junction is forward biased
2. Collector- Base junction is reversed biased
3. Proper zero signal collector current

**The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is called transistor biasing.**



## **WHY BIASING?**

If the transistor is not biased properly, it would work inefficiently and produce distortion in output signal.

## **HOW A TRANSISTOR CAN BE BIASSED?**

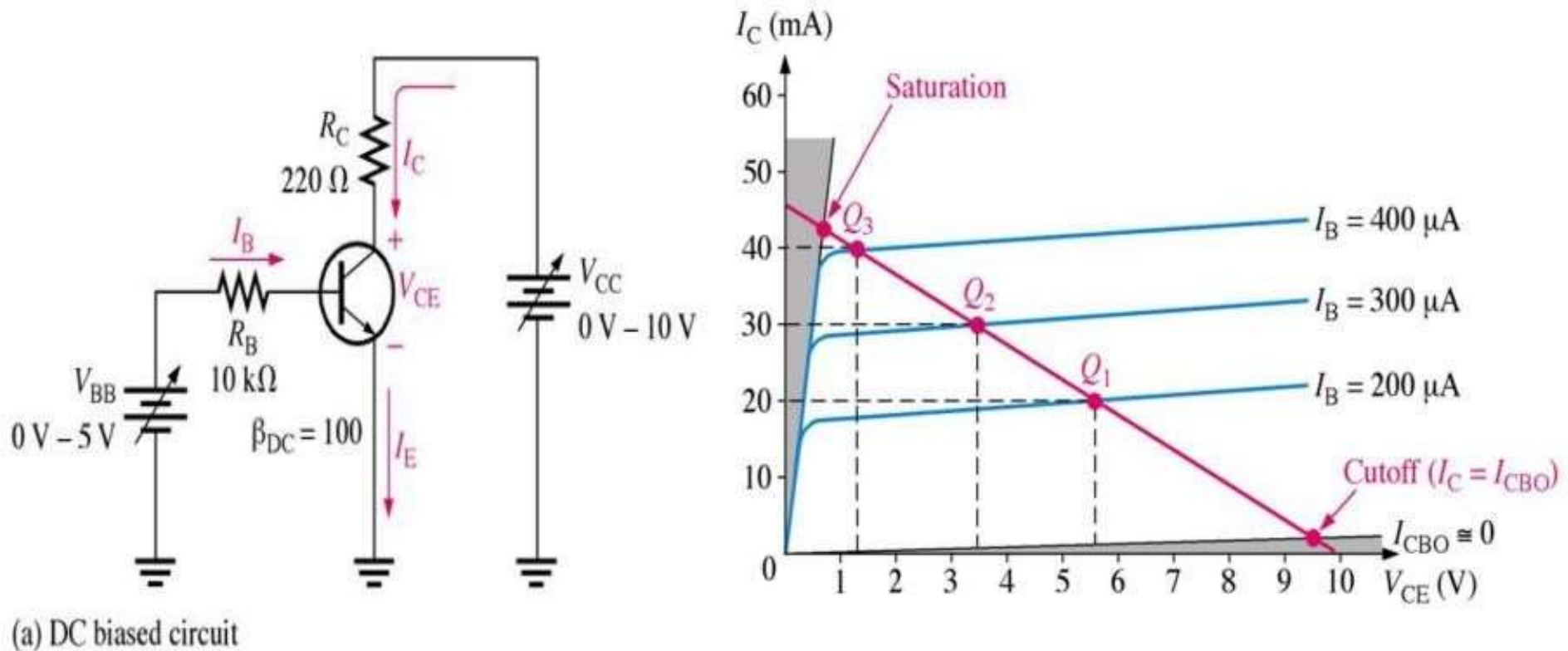
A transistor is biased either with the help of battery or associating a circuit with the transistor. The later method is more efficient and is frequently used. The circuit used for transistor biasing is called the biasing circuit.

# BIAS STABILITY

- Through proper biasing, a desired quiescent operating point of the transistor amplifier in the active region (linear region) of the characteristics is obtained. It is desired that once selected the operating point should remain stable. The maintenance of operating point stable is called Stabilisation.
- The selection of a proper quiescent point generally depends on the following factors:
  - (a) The amplitude of the signal to be handled by the amplifier and distortion level in signal
  - (b) The load to which the amplifier is to work for a corresponding supply voltage
- The operating point of a transistor amplifier shifts mainly with changes in temperature, since the transistor parameters—  $\beta$ ,  $I_{CO}$  and  $V_{BE}$  (*where the symbols carry their usual meaning*)—are functions of temperature.

# The DC Operating Point

For a transistor circuit to amplify it must be properly biased with dc voltages. The dc operating point between saturation and cutoff is called the **Q-point**. The goal is to set the Q-point such that it does not go into saturation or cutoff when an ac signal is applied.



# Requirements of biasing network

- Ensuring proper zero signal collector current.
- Ensuring  $V_{CE}$  not falling below 0.5V for Ge transistor and 1V for Silicon transistor at any instant.
- Ensuring Stabilization of operating point. (zero signal  $I_C$  and  $V_{CE}$ )

# The Thermal Stability of Operating Point ( $S_{I_{CO}}$ )

- **Stability Factor  $S$** :- The stability factor  $S$ , as the change of collector current with respect to the reverse saturation current, keeping  $\beta$  and  $V_{BE}$  constant. This can be written as:

The Thermal Stability Factor :  $S_{I_{CO}}$

$$S_{I_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$= \frac{\Delta I_C}{\Delta I_{CO}}$$

This equation signifies that  $I_C$  changes  $S_{I_{CO}}$  times as fast as  $I_{CO}$

Differentiating the equation of Collector Current  $I_C$  with respect to  $I_{CO}$  and rearranging the term we can write

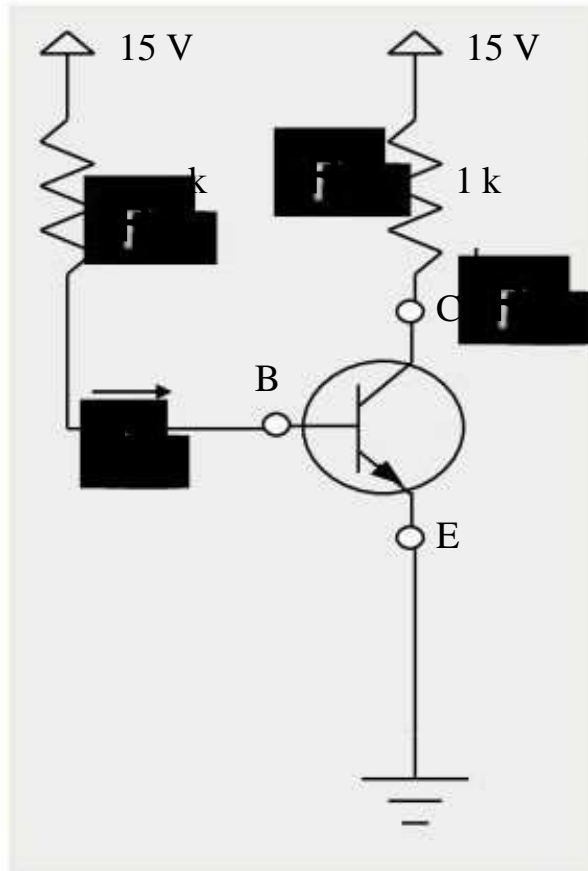
$$S_{I_{CO}} = 1 + \beta$$

It may be noted that Lower is the value of  $S_{I_{CO}}$  better is the stability

# Various Biasing Circuits

- **Fixed Bias Circuit**
- **Fixed Bias with Emitter Resistor**
- **Collector to Base Bias Circuit**
- **Potential Divider Bias Circuit**

# The Fixed Bias Circuit



The Thermal Stability Factor :  $S_T$

$$S_T = \frac{1}{1 - \beta \frac{R_E}{R_B + R_E}}$$

General Equation of  $S_T$  Comes out to be

$$S_T = 1 + \beta$$

Applying KVL through Base Circuit we can write,  $V_{CC} = I_B R_B + V_{BE}$

Diff w. r. t.  $V_{BE}$ , we get  $\frac{dI_B}{dV_{BE}} = -\frac{1}{R_B}$

$S_T = (1 + \beta)$  is very large

Indicating high  $V_{BE}$  stability

**Merits:**

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor ( $R_B$ ).
- A very small number of components are required.

**Demerits:**

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- When the transistor is replaced with another one, considerable change in the value of  $\beta$  can be expected. Due to this change the operating point will shift.
- For small-signal transistors (e.g., not power transistors) with relatively high values of  $\beta$  (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately  $\beta + 1$ . To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

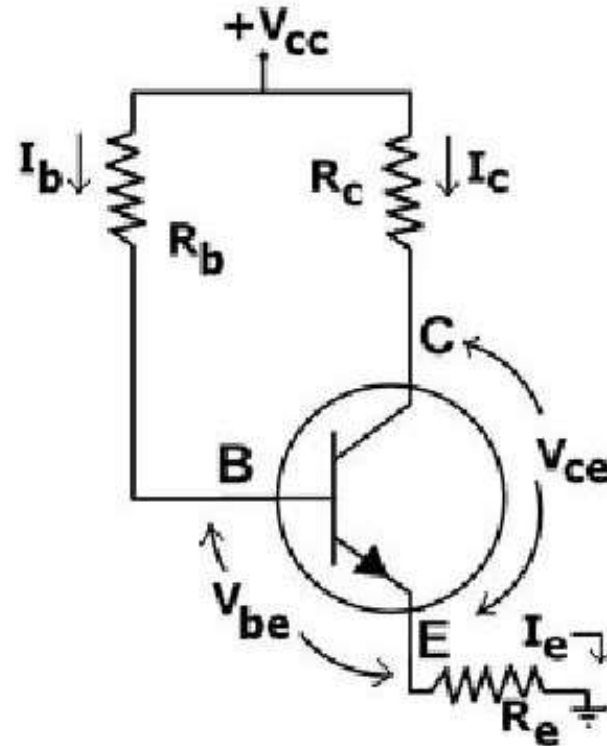


# Usage:

- Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where transistor is used as a switch. However, one application of fixed bias is to achieve crude automatic gain control in the transistor by feeding the base resistor from a DC signal derived from the AC output of a later stage.

# Fixed bias with emitter resistor

The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point.



**Merits:**

- The circuit has the tendency to stabilize operating point against changes in temperature and  $\beta$ -value.

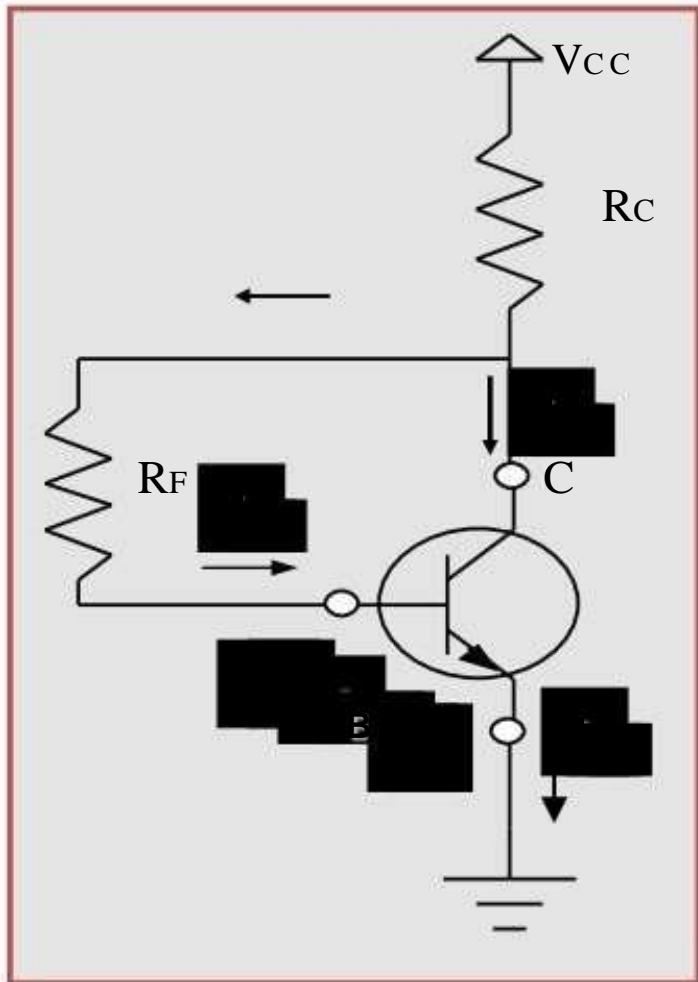
**Demerits:**

- As  $\beta$ -value is fixed for a given transistor, this relation can be satisfied either by keeping  $R_E$  very large, or making  $R_B$  very low.
  - If  $R_E$  is of large value, high  $V_{CC}$  is necessary. This increases cost as well as precautions necessary while handling.
  - If  $R_B$  is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.
- In addition to the above,  $R_E$  causes ac feedback which reduces the voltage gain of the amplifier.

**Usage:**

The feedback also increases the input impedance of the amplifier when seen from the base, which can be advantageous. Due to the above disadvantages, this type of biasing circuit is used only with careful consideration of the trade-offs involved.

# The Collector to Base Bias Circuit



This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor  $R_F$  is connected to the collector instead of connecting it to the DC source  $V_{CC}$ . So any thermal runaway will induce a voltage drop across the  $R_C$  resistor that will throttle the transistor's base current.

Applying KVL through base circuit

we can write  $(1 + \beta) I_B + I_E R_E + V_{BE} = V_{CC}$

Diff. w. r. t.  $I_B$  we get

$$1/\beta = -I_E R_E / (1 + \beta)$$

Therefore  $\xi_1 =$

$$1 - \beta R_E / (1 + \beta)$$

Which is less than  $(1 - \beta)$ , signifying better thermal stability

**Merits:**

- Circuit stabilizes the operating point against variations in temperature and  $\beta$  (i.e. replacement of transistor)

**Demerits:**

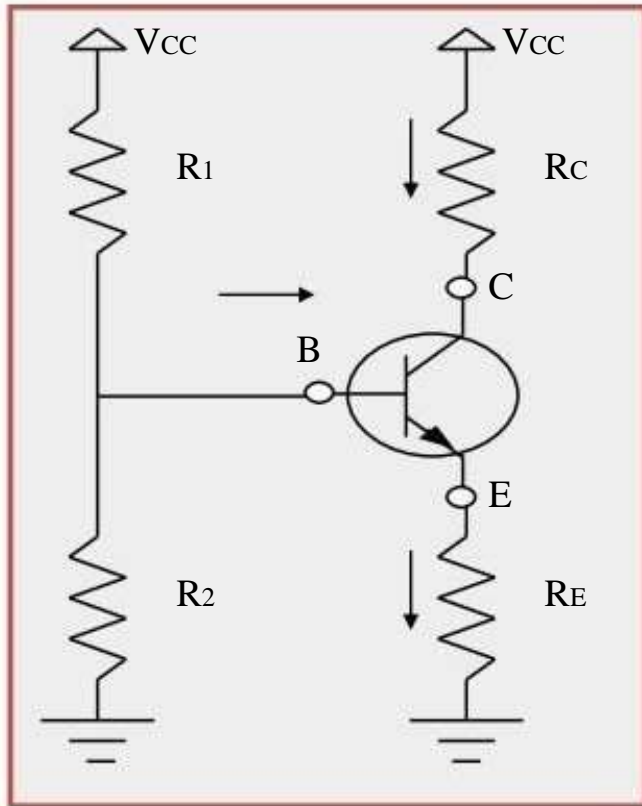
- As  $\beta$  -value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping  $R_c$  fairly large or making  $R_f$  very low.
  - If  $R_c$  is large, a high  $V_{cc}$  is necessary, which increases cost as well as precautions necessary while handling.
  - If  $R_f$  is low, the reverse bias of the collector-base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
  - The resistor  $R_f$  causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

**Usage:** The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

# The Potential Divider Bias Circuit

This is the most commonly used arrangement for biasing as it provides good bias stability. In this arrangement the emitter resistance  $R_E$  provides stabilization. The resistance  $R_E$  causes a voltage drop in a direction so as to reverse bias the emitter junction. Since the emitter-base junction is to be forward biased, the base voltage is obtained from  $R_1$ - $R_2$  network. The net forward bias across the emitter base junction is equal to  $V_B$  - dc voltage drop across  $R_E$ . The base voltage is set by  $V_{CC}$  and  $R_1$  and  $R_2$ . The dc bias circuit is independent of transistor current gain. In case of amplifier, to avoid the loss of ac signal, a capacitor of large capacitance is connected across  $R_E$ . The capacitor offers a very small reactance to ac signal and so it passes through the condenser.

# The Potential Divider Bias Circuit



To find the stability of this circuit, we have to  
convert the circuit into its Thevenin  
Equivalent circuit

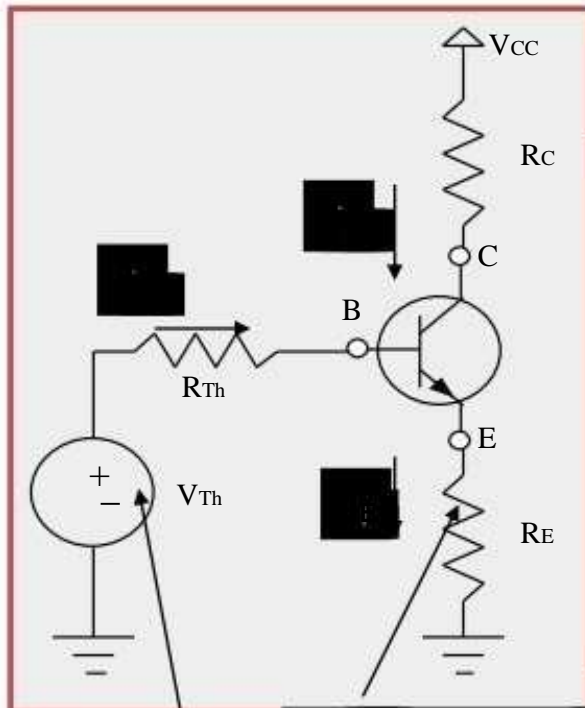
$$V_{th} = V_{CC} \frac{R_2}{R_1 + R_2}$$

$$R_{th} = R_1 \parallel R_2$$



# The Potential Divider Bias Circuit

Thévenin  
Equivalent Circuit



Self-bias Resistor

Thévenin  
Equivalent Voltage

Applying KVL through input base circuit

we can write  $V_{Th} - I_B R_{Th} - V_{BE} = 0$

Therefore,  $I_B = \frac{V_{Th} - V_{BE}}{R_{Th}}$

Diff. w. r. t.  $I_C$  & rearranging we get

$$\frac{dI_C}{dI_B} = \beta \left( \frac{V_{Th} - V_{BE}}{R_{Th}} \right)$$

Therefore

$$S_{I_{C0}} = \frac{1 + \beta}{1 + \beta \frac{R_E}{R_{Th} + R_E}}$$

This shows that  $S_{I_{C0}}$  is inversely proportional to  $R_E$  and it is less than  $(1 + \beta)$ , signifying better thermal stability.

## Merits:

- Operating point is almost independent of  $\beta$  variation.
- Operating point stabilized against shift in temperature.

## Demerits:

- As  $\beta$ -value is fixed for a given transistor, this relation can be satisfied either by keeping  $R_E$  fairly large, or making  $R_1 || R_2$  very low.
  - If  $R_E$  is of large value, high  $V_{CC}$  is necessary. This increases cost as well as precautions necessary while handling.
  - If  $R_1 || R_2$  is low, either  $R_1$  is low, or  $R_2$  is low, or both are low. A low  $R_1$  raises  $V_B$  closer to  $V_C$ , reducing the available swing in collector voltage, and limiting how large  $R_C$  can be made without driving the transistor out of active mode. A low  $R_2$  lowers  $V_{be}$ , reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
  - AC as well as DC feedback is caused by  $R_E$ , which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

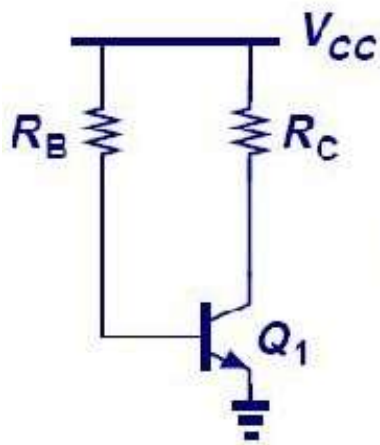
## Usage:

The circuit's stability and merits as above make it widely used for linear circuits.

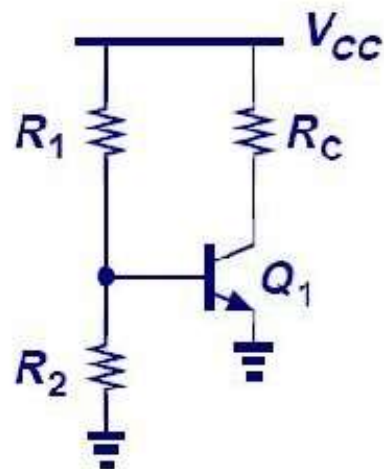
# Summary

- The Q-point is the best point for operation of a transistor for a given collector current.
- The purpose of biasing is to establish a stable operating point (Q-point).
- The linear region of a transistor is the region of operation within saturation and cutoff.
- Out of all the biasing circuits, potential divider bias circuit provides highest stability to operating point.

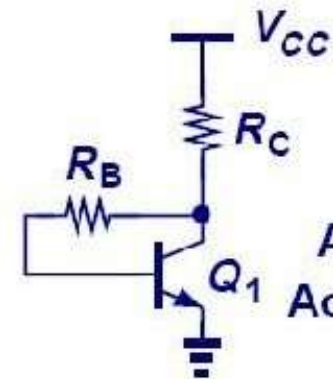
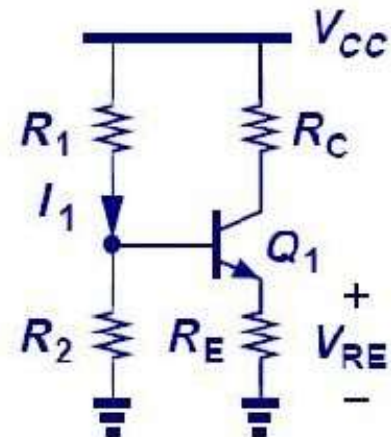
# Summary of Biasing Techniques



Sensitive  
to  $\beta$



Sensitive  
to Resistor Error



Always in  
Active Mode

# UNIT 3

## Amplifiers

# The Field Effect Transistor (FET)

- In 1945, Shockley had an idea for making a solid state device out of semiconductors.
- He reasoned that a strong electrical field could cause the flow of electricity within a nearby semiconductor.
- He tried to build one, but it didn't work.
- Three years later, Brattain & Bardeen built the first working transistor, the germanium point-contact transistor, which was designed as the junction (sandwich) transistor.
- In 1960 Bell scientist John Atalla developed a new design based on Shockley's original field-effect theories.
- By the late 1960s, manufacturers converted from junction type integrated circuits to field effect devices.

# The Field Effect Transistor

## (FET)

- Field effect devices are those in which current is controlled by the action of an electron field, rather than carrier injection.
- Field-effect transistors are so named because a weak electrical signal coming in through one electrode creates an electrical field through the rest of the transistor.
- The FET was known as a “unipolar” transistor.
- The term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

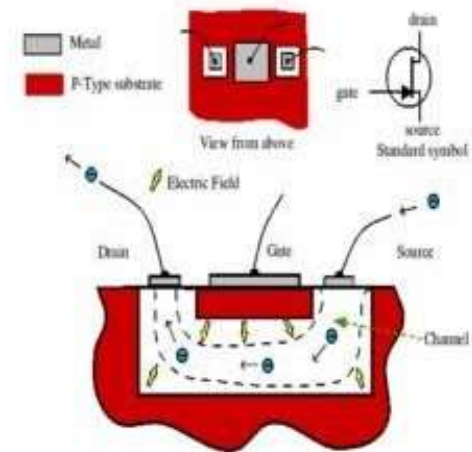
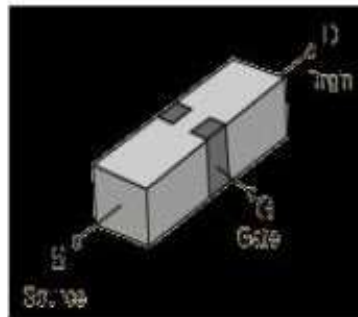
# The Field Effect Transistor (FET)

The family of FET devices may be divided into :

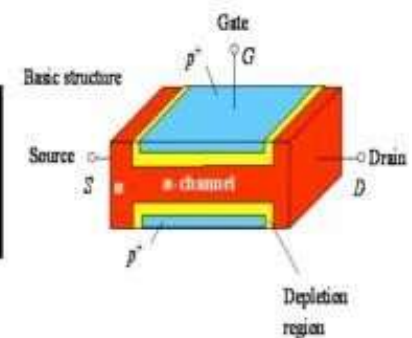
- Junction FET
- Depletion Mode MOSFET
- Enhancement Mode MOSFET



- 

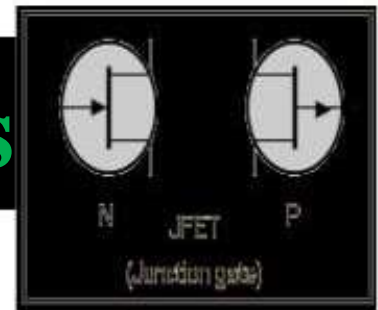


# Junction FETs

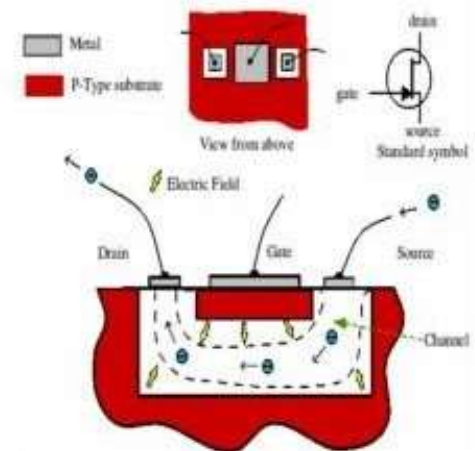
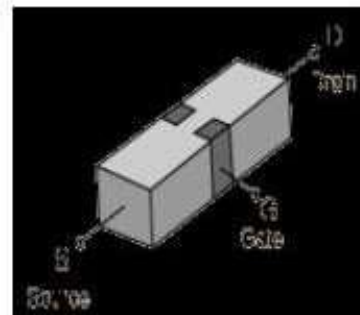
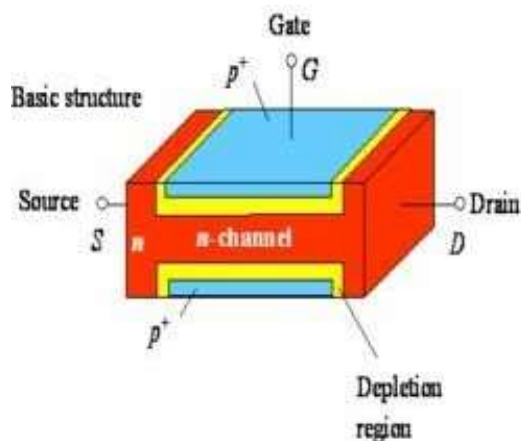


- JFET is a high-input resistance device, while the BJT is comparatively low.
- If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons.
- If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes.
- N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.

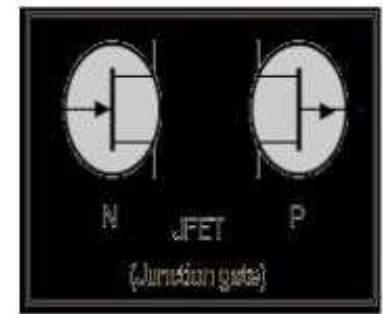
# Junction FETs (JFETs)



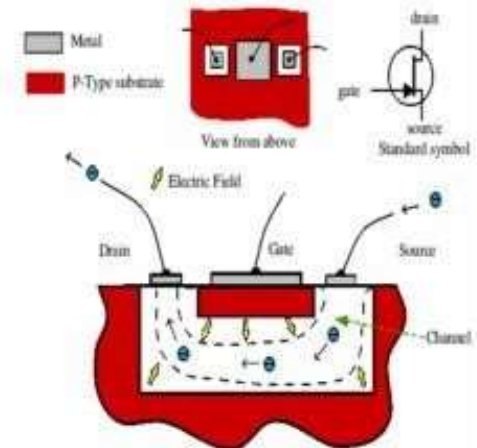
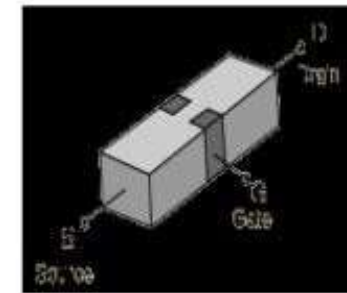
- The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased.
- The fundamental difference between JFET and BJT devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the BJT is always some value greater than zero.

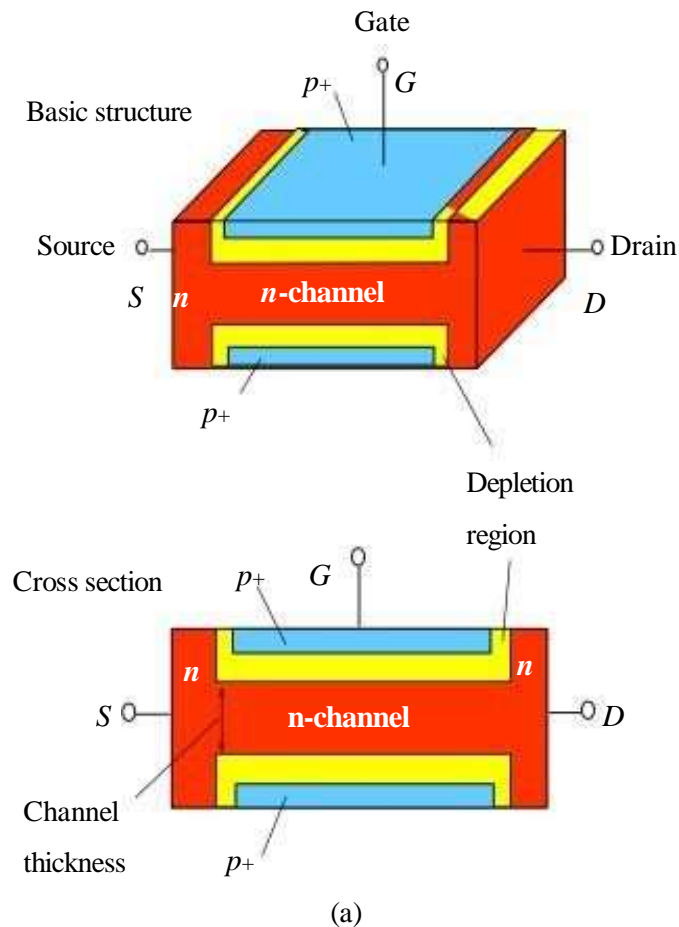


# Basic structure of JFE



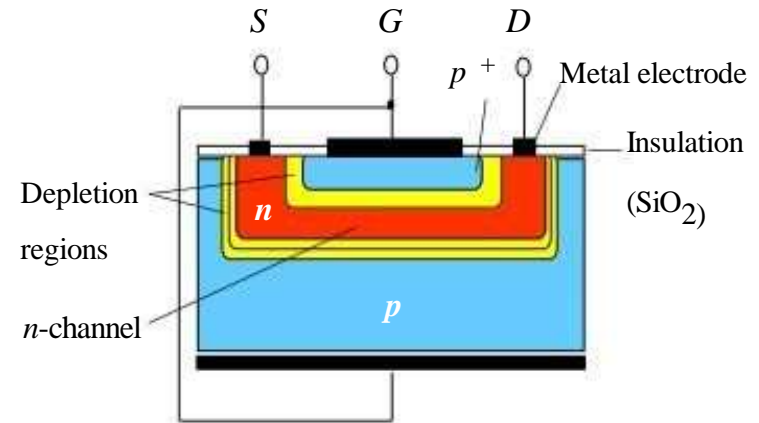
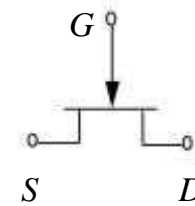
- In addition to the channel, a JFET contains two ohmic contacts: the source and the drain.
- The JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.





(a)

Circuit symbol  
for  $n$ -channel FET

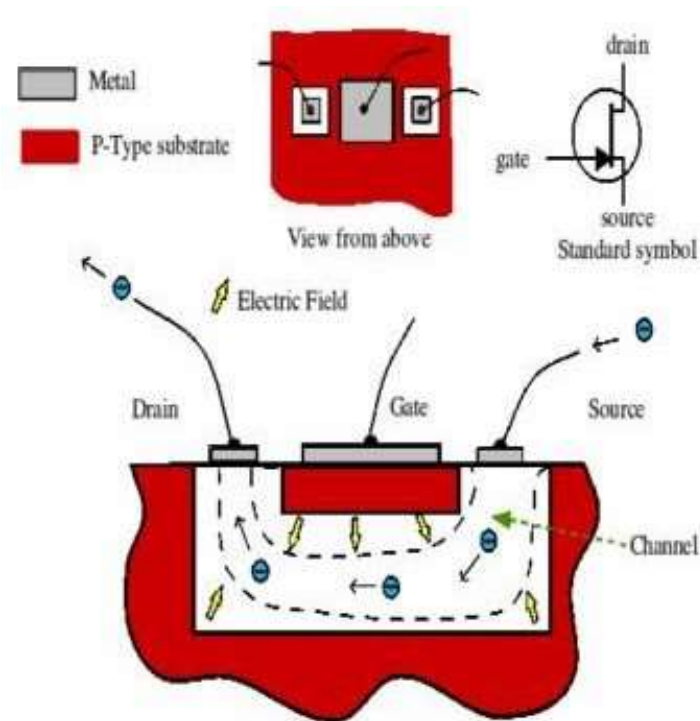


(b)

(a) The basic structure of the junction field effect transistor (JFET) with an  $n$ -channel. The two  $p^+$  regions are electrically connected and form the gate. (b) A simplified sketch of the cross section of a more practical  $n$ -channel JFET.

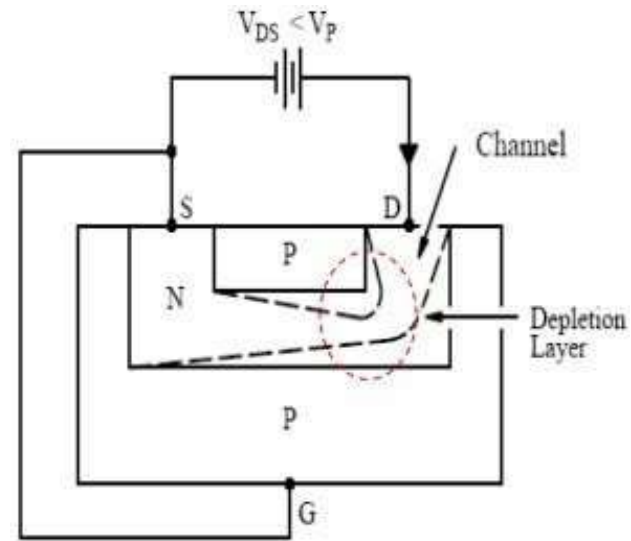
# N-channel JFET

- This transistor is made by forming a channel of N-type material in a *P-type substrate*.
- Three wires are then connected to the device.
- One at each end of the channel.
- One connected to the substrate.
- In a sense, the device is a bit like a PN-junction diode, except that there are two wires connected to the N-type side.



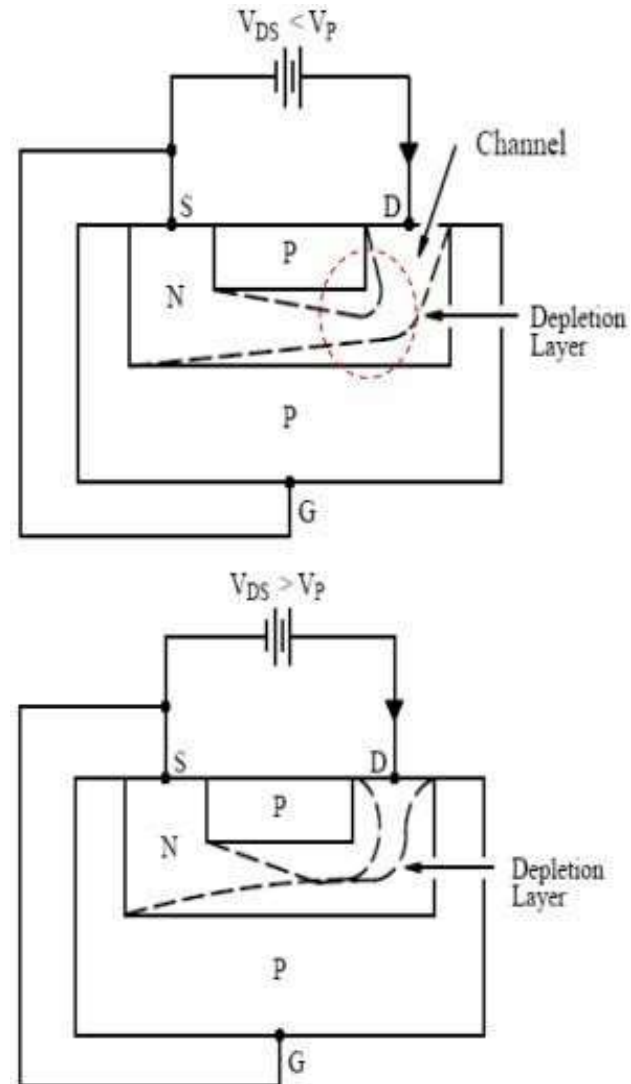
# How JFET Function

- The gate is connected to the source.
- Since the pn junction is reverse-biased, little current will flow in the gate connection.
- The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away.
- The most depleted portion is in the high field between the G and the D, and the least-depleted area is between the G and the S.

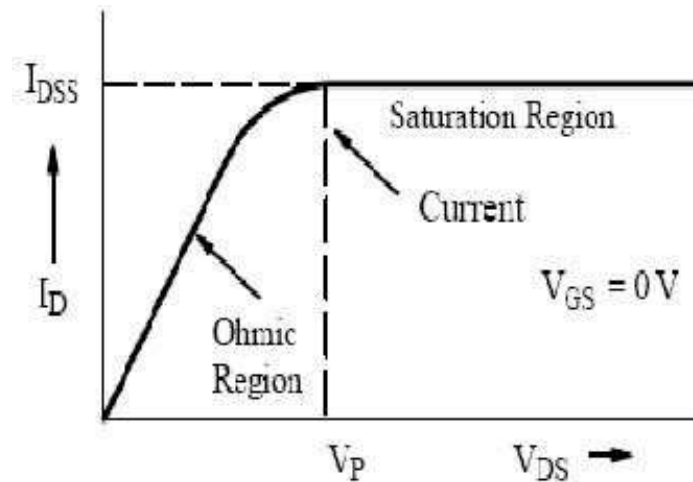


# How JFET Function

- Because the flow of current along the channel from the (+ve) drain to the (-ve) source is really a flow of free electrons from S to D in the n-type Si, the magnitude of this current will fall as more Si becomes depleted of free electrons.
- There is a limit to the drain current ( $I_D$ ) which increased  $V_{DS}$  can drive through the channel.
- This limiting current is known as  $I_{DSS}$  (*Drain-Source current with the gate shorted to the source*).

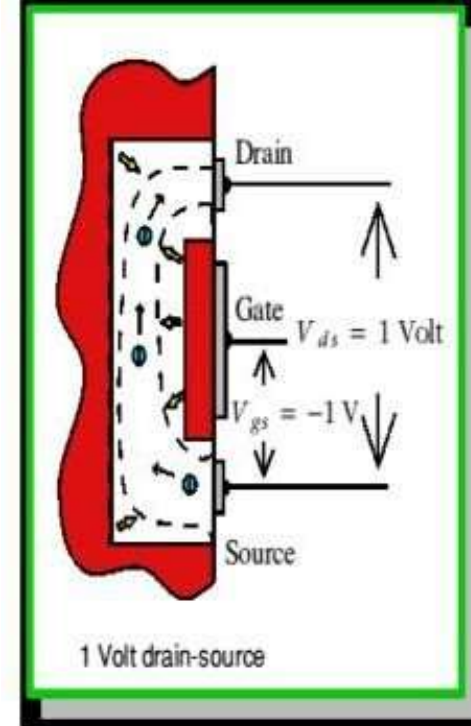




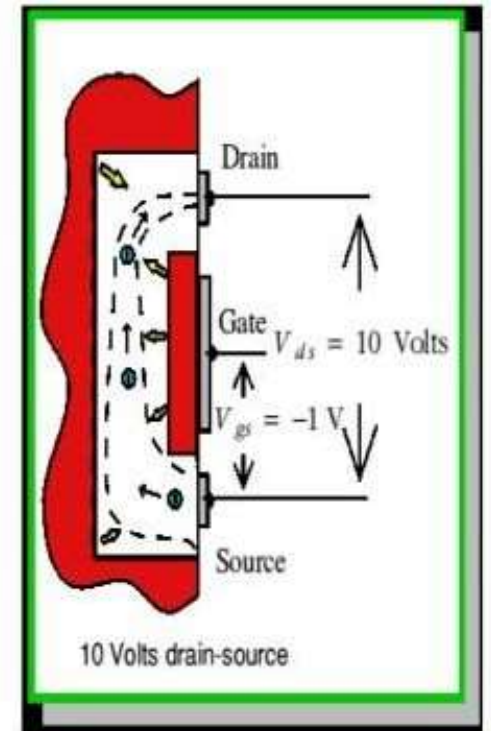


- The output characteristics of an n-channel JFET with the gate short-circuited to the source.
- The initial rise in  $I_D$  is related to the buildup of the depletion layer as  $V_{DS}$  increases.
- The curve approaches the level of the limiting current  $I_{DSS}$  when  $I_D$  begins to be pinched off.
- The physical meaning of this term leads to one definition of pinch-off voltage,  $V_P$ , which is the value of  $V_{DS}$  at which the maximum  $I_{DSS}$  flows.

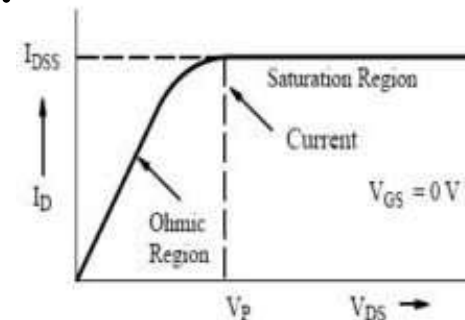
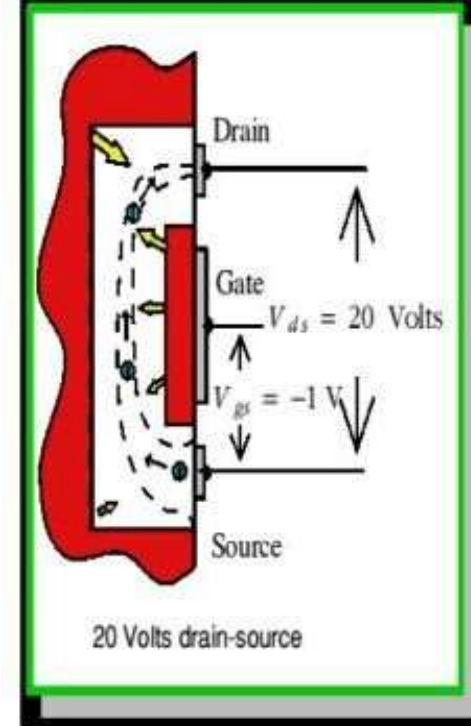
- With a steady gate-source voltage of 1 V there is always 1 V across the wall of the channel at the source end.
- A drain-source voltage of 1 V means that there will be 2 V across the wall at the drain end. (*The drain is 'up' 1V from the source potential and the gate is 1V 'down', hence the total difference is 2V.*)
- The higher voltage difference at the drain end means that the electron channel is squeezed down a bit more at this end.

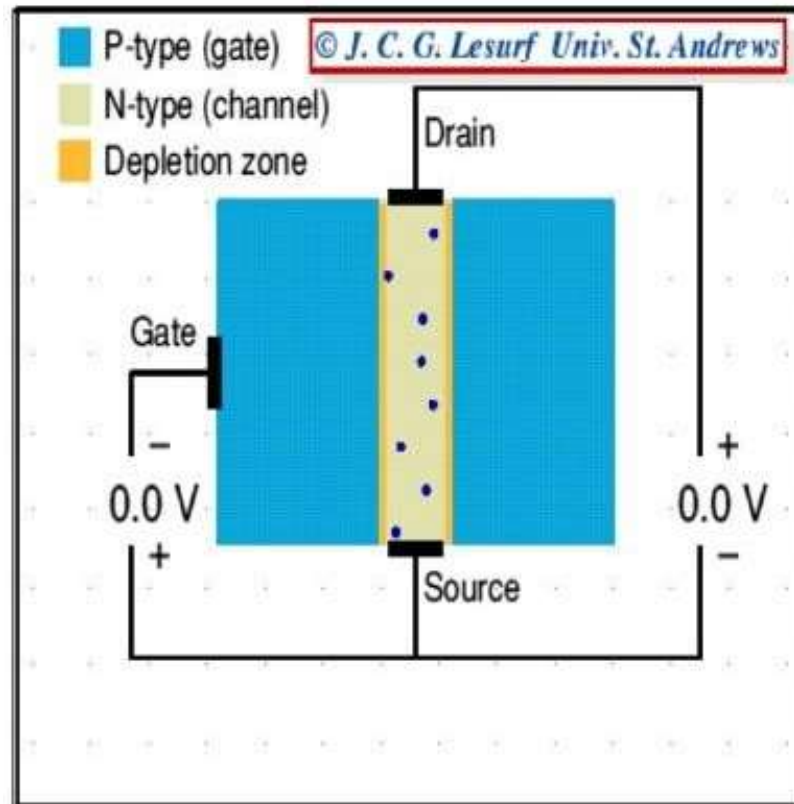


- When the drain-source voltage is increased to 10V the voltage across the channel walls at the drain end increases to 11V, but remains just 1V at the source end.
- The field across the walls near the drain end is now a lot larger than at the source end.
- As a result the channel near the drain is squeezed down quite a lot.

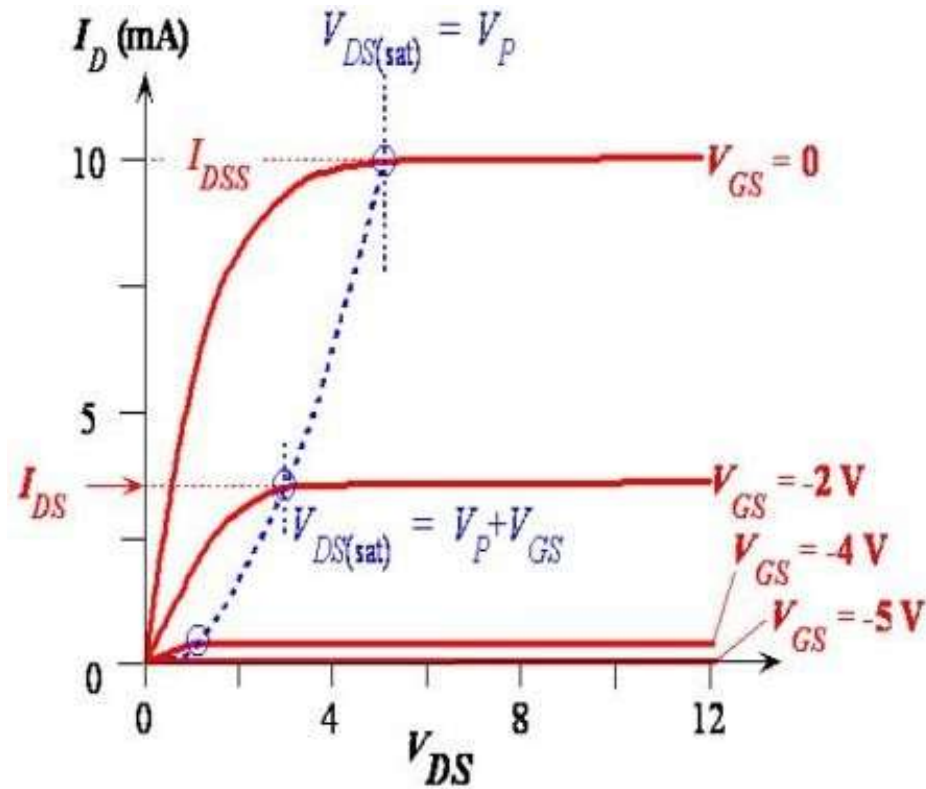


- Increasing the source-drain voltage to 20V squeezes down this end of the channel still more.
- As we increase this voltage we increase the electric field which drives electrons along the open part of the channel.
- However, also squeezes down the channel near the drain end.
- This reduction in the open channel width makes it harder for electrons to pass.
- As a result the drain-source current tends to remain constant when we increase the drain-source voltage.



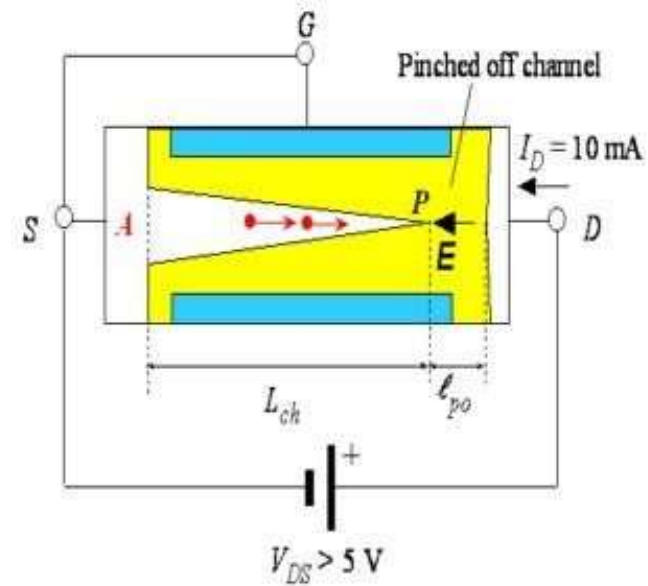


- Increasing  $V_{DS}$  increases the widths of depletion layers, which penetrate more into channel and hence result in more channel narrowing toward the drain.
- The resistance of the n-channel,  $R_{AB}$  therefore increases with  $V_{DS}$ .
- The drain current:  $I_{DS} = V_{DS}/R_{AB}$
- $I_D$  versus  $V_{DS}$  exhibits a sub linear behavior, see figure for  $V_{DS} < 5V$ .
- The pinch-off voltage,  $V_P$  is the magnitude of reverse bias needed across the p+n junction to make them just touch at the drain end.
- Since actual bias voltage across p+n junction at drain end is  $V_{GD}$ , the pinch-off occur whenever:  $V_{GD} = -V_P$ .



Typical  $I_D$  vs  $V_{DS}$  characteristics of a JFET for various fixed gate voltages  $V_{GS}$ .

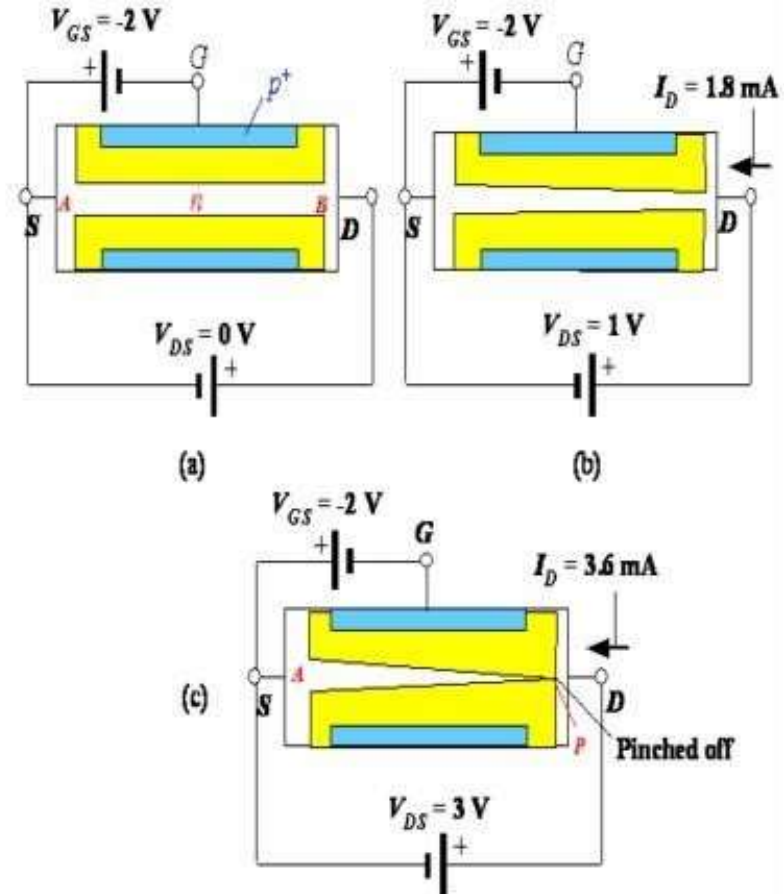
- Beyond  $V_{DS} = V_P$ , there is a short pinch-off channel of length,  $\ell_{po}$ .
- As  $V_{DS}$  increases, most of additional voltage simply drops across this region as this region is depleted of carriers and hence highly resistive.
- Voltage drop across channel length,  $L_{ch}$  remain as  $V_P$ .
- Beyond pinch-off then
 
$$I_D = V_P / R_{AP} \quad (V_{DS} > V_P).$$



The pinched-off channel and conduction for  $V_{DS} > V_P (=5 \text{ V})$ .



- What happens when negative voltage, say  $V_{GS} = -2\text{V}$ , is applied to gate with respect to source (with  $V_{DS}=0$ ).
- The p+n junctions are now reverse biased from the start, the channel is narrower, and channel resistance is now larger than in the  $V_{GS} = 0$  case.



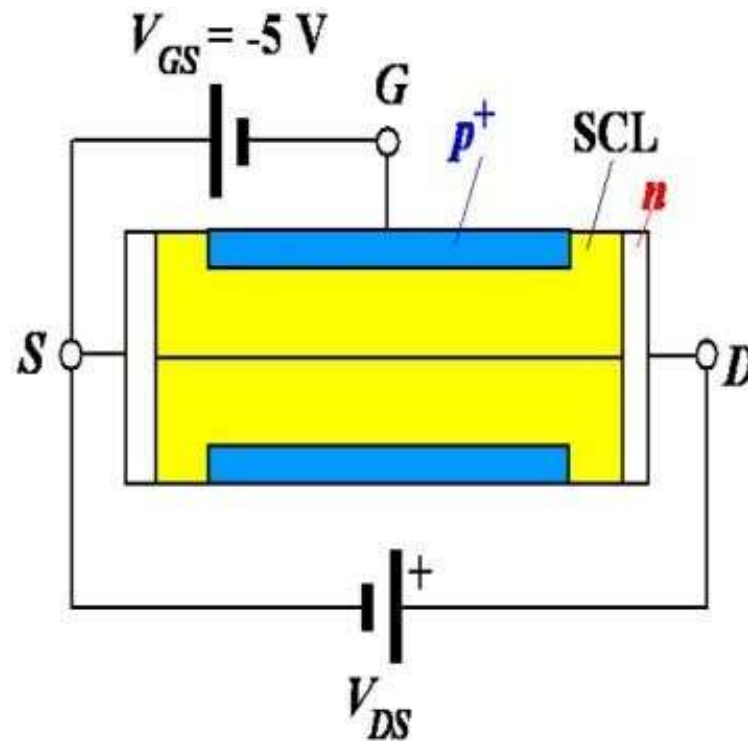
(a) The JFET with a negative  $V_{GS}$  voltage has a narrower n-channel at the start. (b) Compared to the  $V_{GS} = 0$  case, the same  $V_{DS}$  gives less  $I_D$  as the channel is narrower. (c) The channel is pinched off at  $V_{DS} = 3\text{ V}$  sooner than the  $V_{GS} = 0$  case where it was  $V_{DS} = 5\text{ V}$ .

- The drain current that flows when a small  $V_{DS}$  applied (Fig b) is now smaller than in  $V_{GS}=0$  case.
- Applied  $V_{DS}=3\text{ V}$  to pinch-off the channel (Fig c).
- When  $V_{DS}=3\text{V}$ ,  $V_{GD}$  across p+n junction at drain end is  $-5\text{V}$ , which is  $-V_P$ , so channel becomes pinch-off.
- Beyond pinch-off,  $I_D$  is nearly saturated just as in the  $V_{GS}=0$  case.
- Pinch-off occurs at  $V_{DS}=V_{DS(sat)}$ ,  $V_{DS(sat)}=V_P+V_{GS}$ , where  $V_{GS}$  is -ve voltage (reducing  $V_P$ ).
- For  $V_{DS}>V_{D(SAT)}$ ,  $I_D$  becomes nearly saturated at value as  $I_{DS}$ .

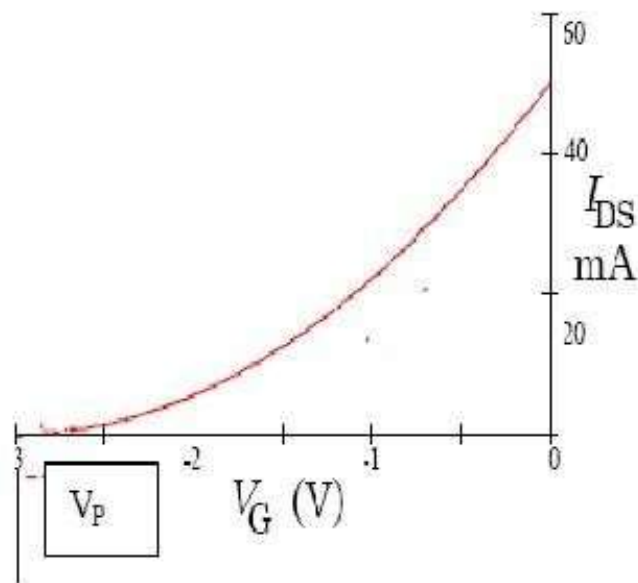
- Beyond pinch-off, with -ve  $V_{GS}$ ,  $I_{DS}$  is

$$I_D \approx I_{DS} \approx \frac{V_{DS(sat)}}{R_{AP}(V_{GS})} = \frac{V_P + V_{GS}}{R_{AP}(V_{GS})}, \quad V_{DS} > V_{DS(sat)}$$

- Where  $R_{AP}(V_{GS})$  is the effective resistance of the conducting n-channel from A to P, which depends on channel thickness and hence  $V_{GS}$ .
- When  $V_{GS} = -V_P = -5V$  with  $V_{DS} = 0$ , the two depletion layers touch over the entire channel length and the whole channel is closed.
- The channel said to be off.



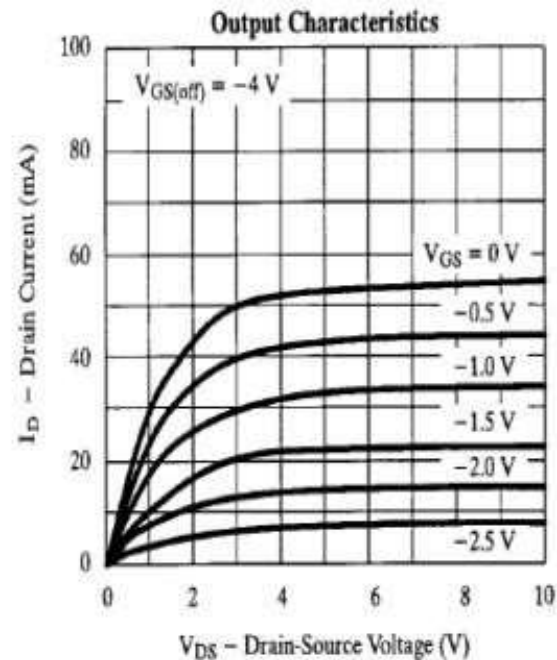
When  $V_{GS} = -5\text{ V}$  the depletion layers close the whole channel from the start, at  $V_{DS} = 0$ . As  $V_{DS}$  is increased there is a very small drain current which is the small reverse leakage current due to thermal generation of carriers in the depletion layers.



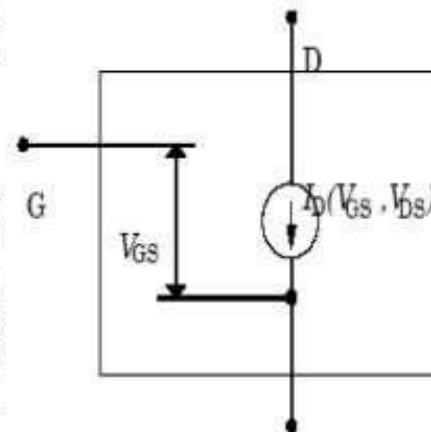
**Figure 1: JFET Transfer Characteristic**

A more useful JFET model replaces the variable resistor with a variable current source whose current depends on the gate voltage  $V_{GS}$  and the drain-source voltage,  $V_{DS}$ .

The drain-source current is largest when the gate-source voltage  $V_{GS}$  is zero, typically about 50mA. As  $V_{GS}$  is made negative, the current decreases. When the gate-source voltage  $V_{GS}$  reaches a critical value called the gate-source pinch off voltage  $V_S$ , the drain current  $I_D$  is cutoff entirely; no current flows. The value of  $V_S$  depends on the particular type of JFET (and even varies substantially between JFETs of the same type), but is typically around -4V. As  $V_{GS}$  is raised towards 0V, current  $I_D$  starts to flow. A typical plot of the current vs. gate voltage is shown in Fig. 1 below. Simple models of JFET performance predict that the curve will be parabolic, but actual devices may differ substantially from this prediction.



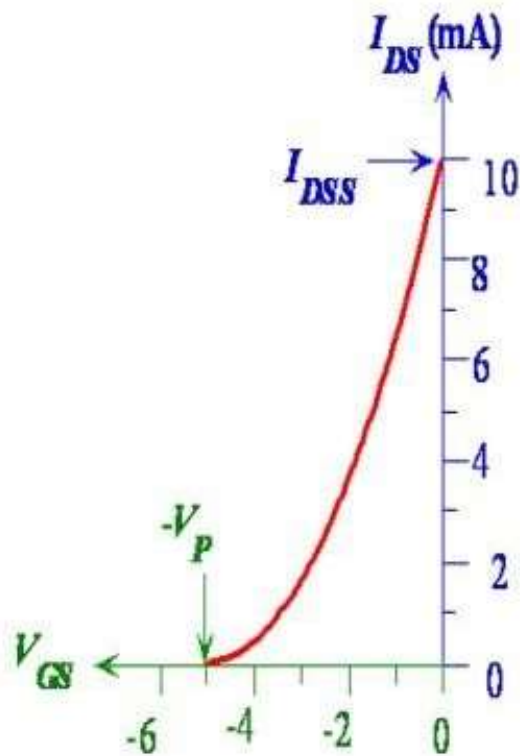
The source current also depends on the drain source voltage.



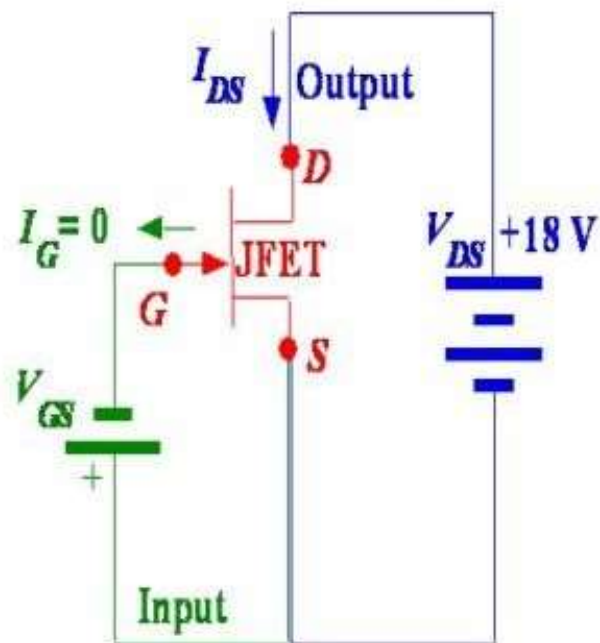
- There is a convenient relationship between  $I_{DS}$  and  $V_{GS}$ .
- Beyond pinch-off

$$I_{DS} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{SG(off)}} \right)^2$$

- Where  $I_{DSS}$  is drain current when  $V_{GS} = 0$  and  $V_{GS(off)}$  is defined as  $-V_P$ , that is gate-source voltage that just pinches off the channel.
- The pinch off voltage  $V_P$  here is a +ve quantity because it was introduced through  $V_{DS(sat)}$ .
- $V_{GS(off)}$  however is negative,  $-V_P$ .



(a)

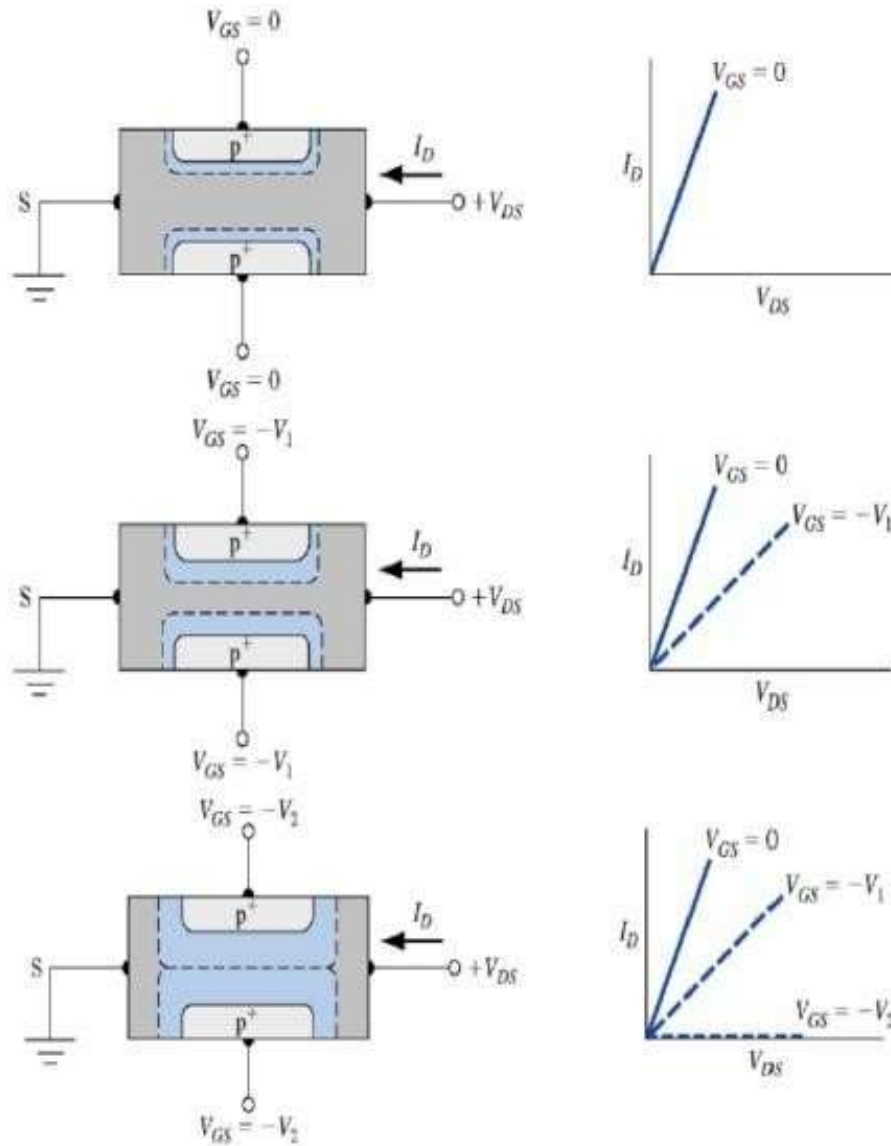


(b)

(a) Typical  $I_{DS}$  vs  $V_{GS}$  characteristics of a JFET (b).

The DC circuit in which  $V_{GS}$  in the gate-source circuit (input) controls the drain current  $I_{DS}$  in the drain-source (output) circuit in which  $V_{DS}$  is kept constant and large ( $V_{DS} > V_P$ ).

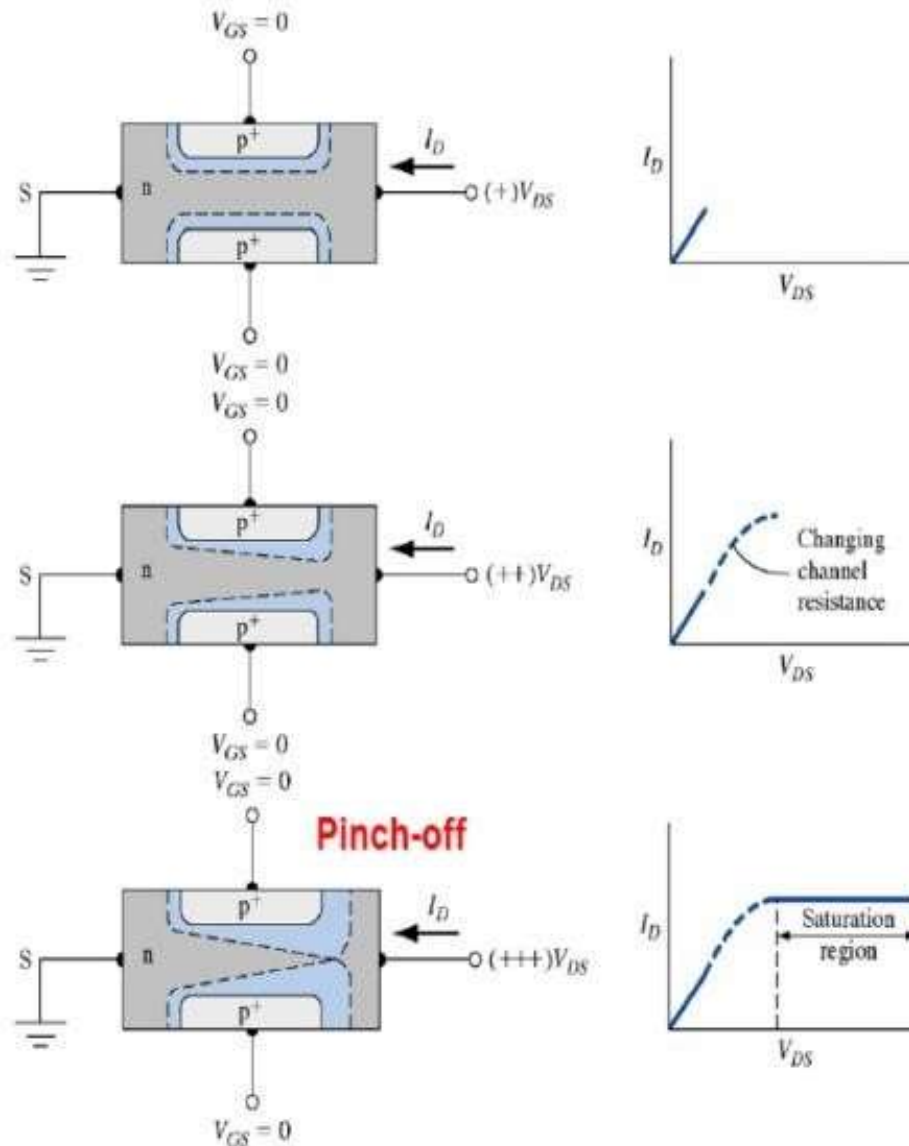
# I-V characteristics



**$V_G$  controls the channel width  $\rightarrow V_G$  control  $I_d$**

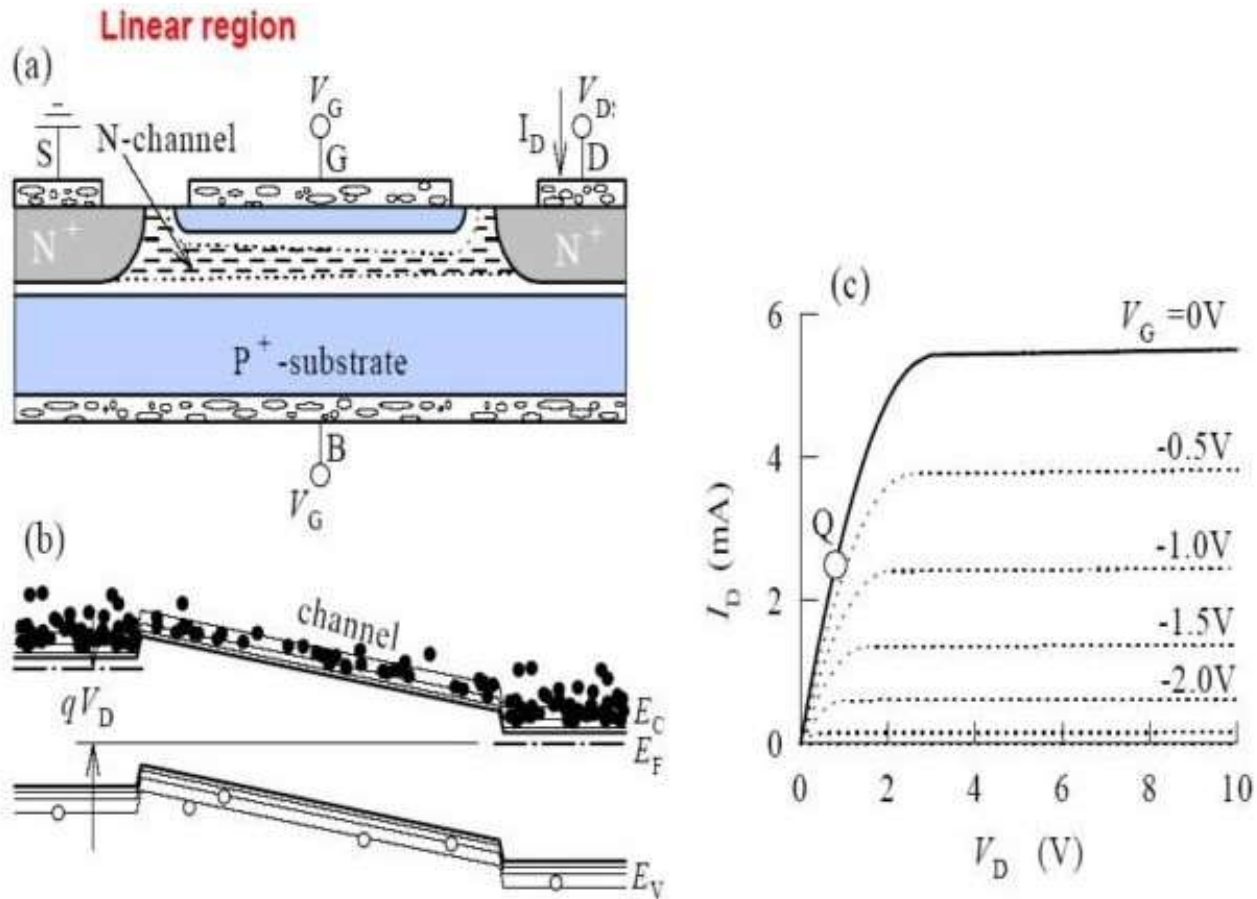


# I-V characteristics



After pinch-off:  $I_D \neq f(V_D)$ ;  $I_D = f(V_G)$  - current source

# JFET: I-V characteristics



# The transconductance curve

- The process for plotting transconductance curve for a given JFET:
- Plot a point that corresponds to value of  $V_{GS(off)}$ .
- Plot that corresponds to value of  $I_{DSS}$ .
- Select 3 or more values of  $V_{GS}$  between 0 V and  $V_{GS(off)}$ . For value of  $V_{GS}$ , determine the corresponding value of  $I_D$  from

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

- Plot the point from (3) and connect all the plotted point with a smooth curve.

Example: Plot the transconductance curve for a JFET with  $V_{GS(off)} = -6$  V and  $I_{DSS} = 3$  mA.

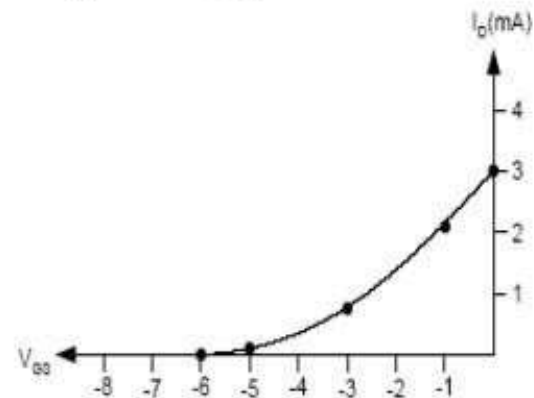
At  $V_{GS(off)} = -6$  V,  $I_D = 0$ .

At  $I_{DSS} = 3$  mA,  $V_{GS} = 0$ .

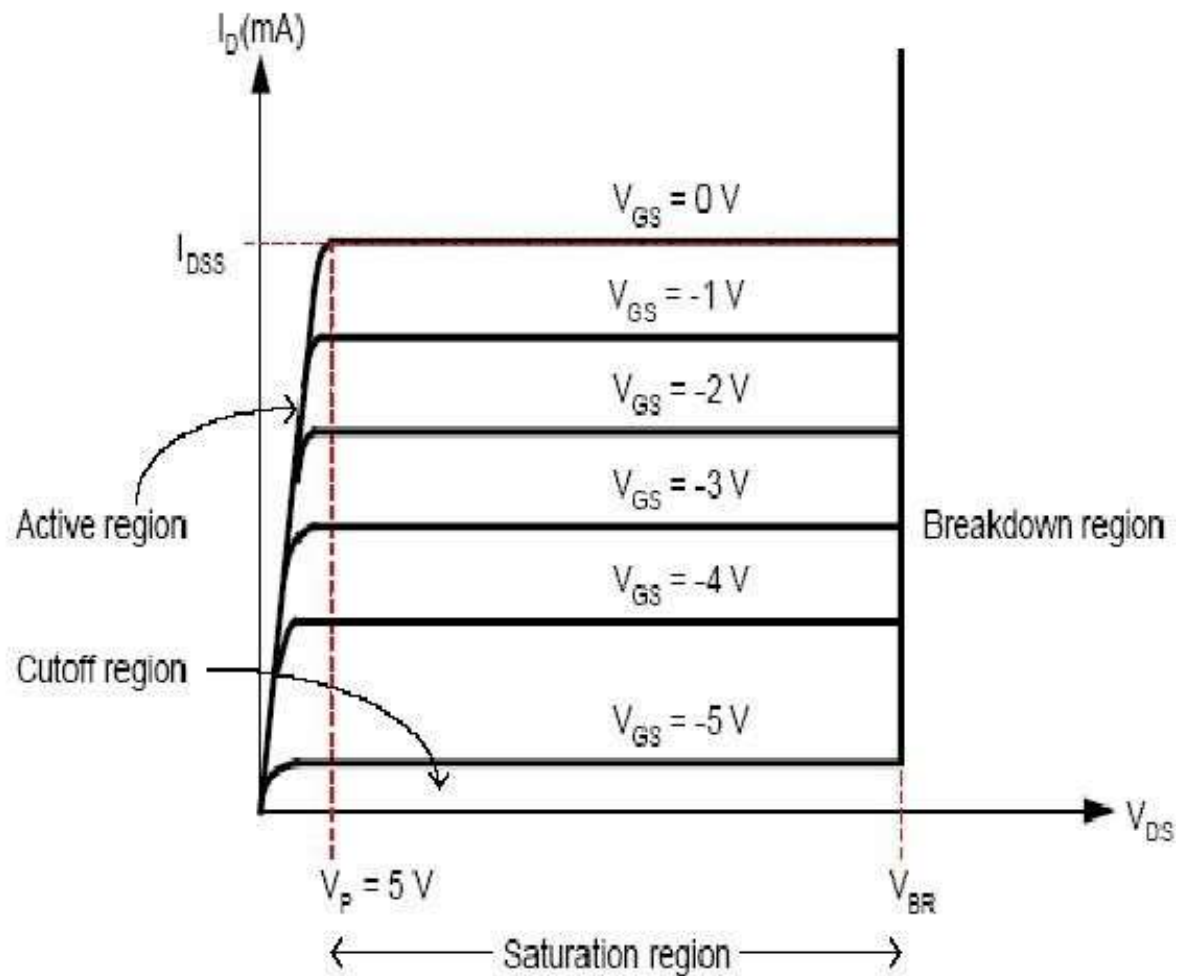
At  $V_{GS} = -1$  V,  $I_D = 2.08$  mA.

At  $V_{GS} = -3$  V,  $I_D = 0.75$  mA.

At  $V_{GS} = -5$  V,  $I_D = 0.083$  mA.



- The relationship between  $V_{GS}$ ,  $V_{DS}$  and  $I_{DSS}$  is as shown below.

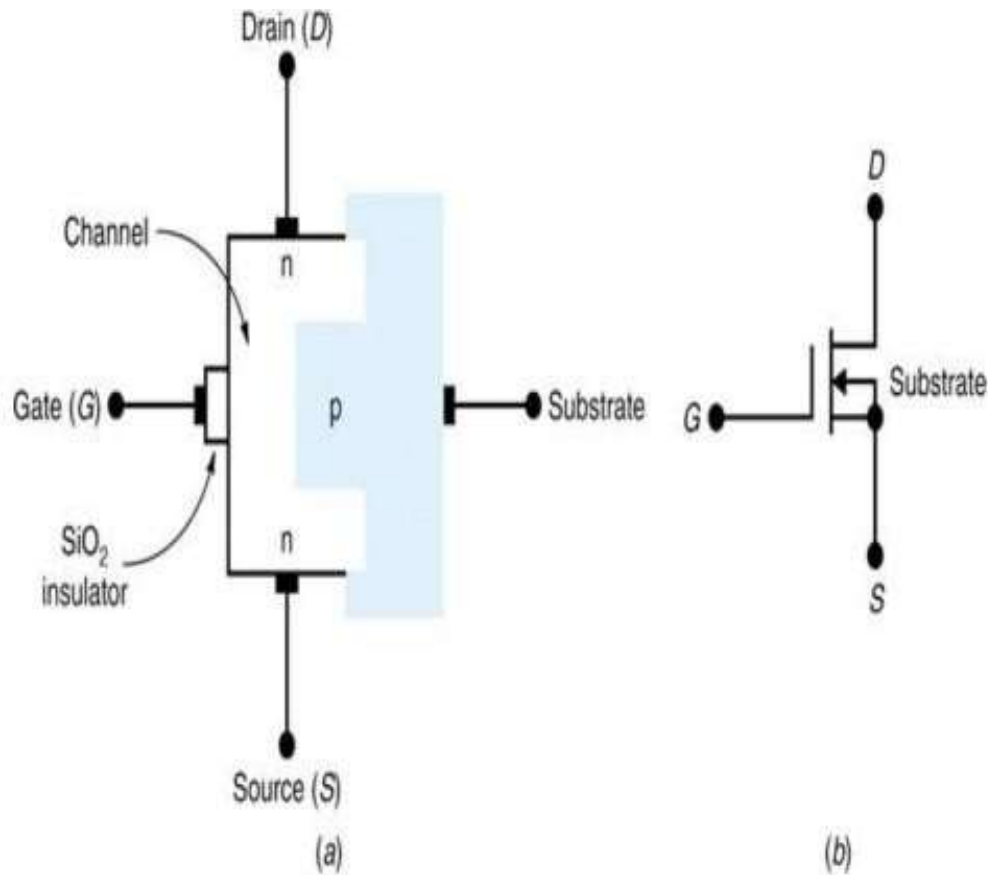


**JFET drain curves**

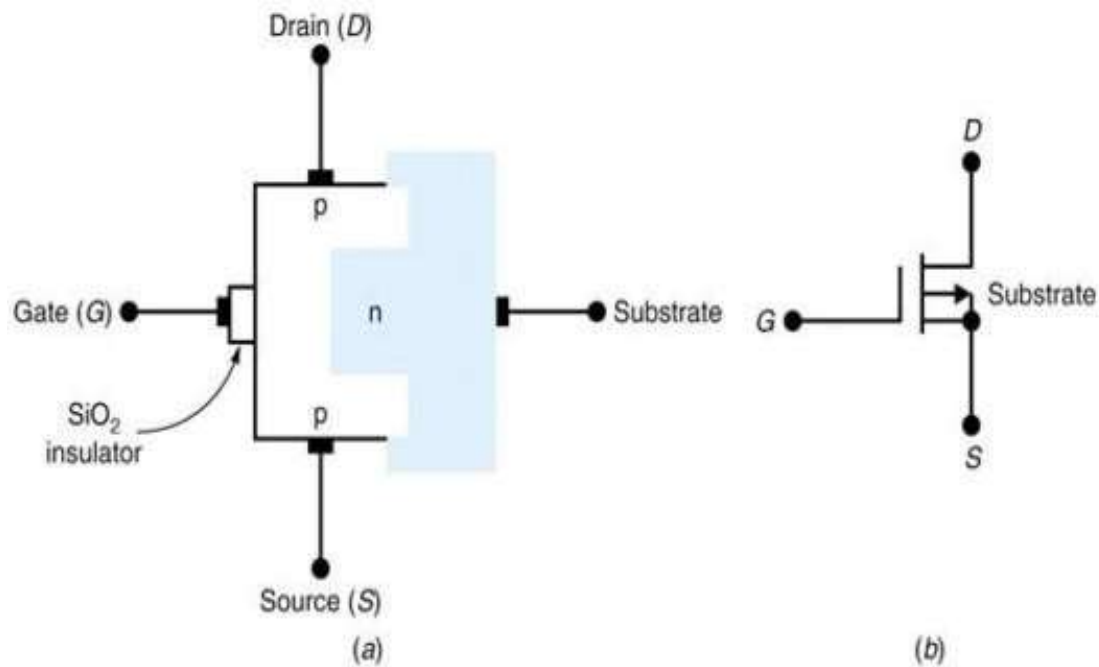
# MOSFETs and Their Characteristics

- The **metal-oxide semiconductor** field effect transistor has a gate, source, and drain just like the JFET.
- The drain current in a MOSFET is controlled by the gate-source voltage  $V_{GS}$ .
- There are two basic types of MOSFETs: the enhancement-type and the depletion-type.
- The enhancement-type MOSFET is usually referred to as an E-MOSFET, and the depletion-type, a D-MOSFET.
- The MOSFET is also referred to as an IGFET because the gate is insulated from the channel.

# MOSFETs and Their Characteristics

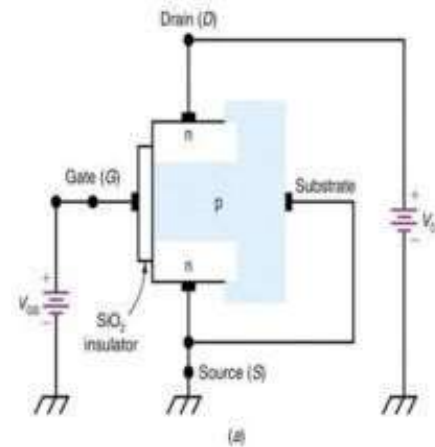


# MOSFETs and Their Characteristics



# MOSFETs and Their Characteristics

Fig. 30-20 (a) shows the construction of an n-channel, enhancement-type MOSFET. The p-type substrate makes contact with the  $\text{SiO}_2$  insulator. Because of this, there is no channel for conduction between the drain and source terminals.

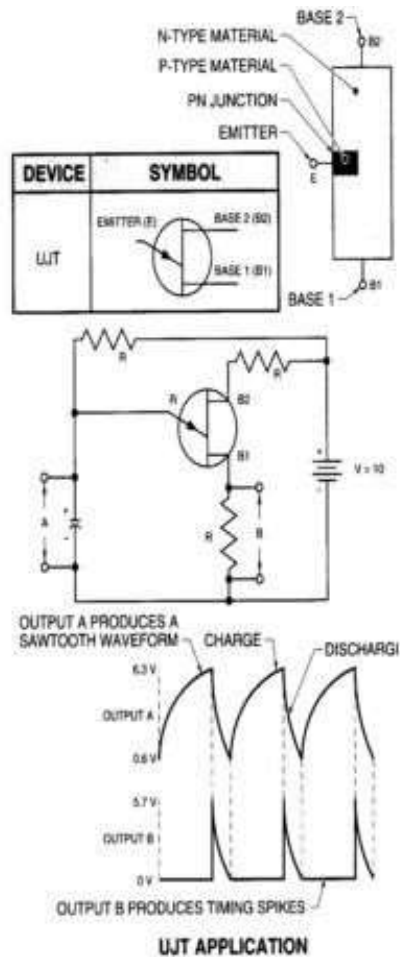




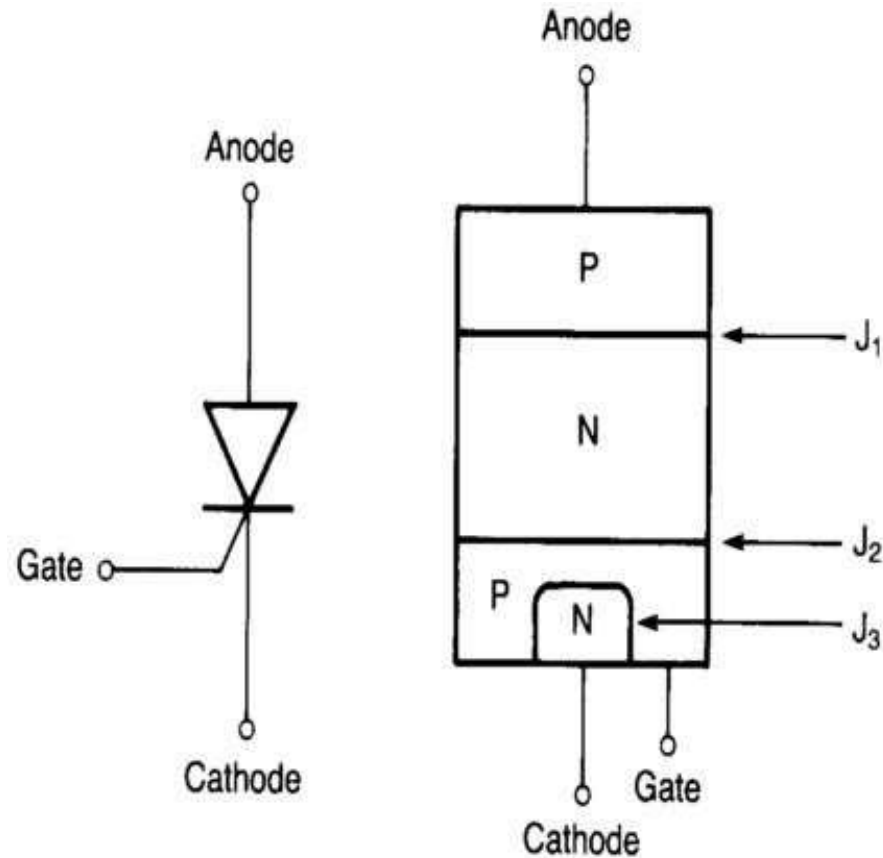
# Unijunction Transistor (UJT)

- Simple two layer transistor
- Operates using the principle of avalanche breakdown producing a saw tooth output
- Used to trigger an SCR or TRIAC
- Also used within pulse circuitry
- Output from photocells, thermistors, and other transducers can be used to trigger

# Unijunction Transistor (UJT)



# Silicon Controlled Rectifier (SCR)



# SCR - Continued

## **Three terminals**

**anode - P-layer**

**cathode - N-layer (opposite end)**

**gate - P-layer near the cathode**

## **Three junctions - four layers**

**Connect power such that the anode is positive with respect to the cathode - no current will flow**

**NOTE: Blocked by the reverse bias of junction 2**

# SCR - Continued

- Positive potential applied to the gate
  - Current will flow - TURNED-ON
  - Once turned on, gate potential can be removed and the SCR still conducts

CALLED LATCHING

- Holding current maintains latch

# Silicon Controlled Rectifier

