MOHAMED SATHAK A.J. COLLEGE OF ENGINEERING

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CS3351-DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

EPC-II YEAR CSE, IT/III RD SEMESTER

UNIT-I COMBINATIONAL LOGIC

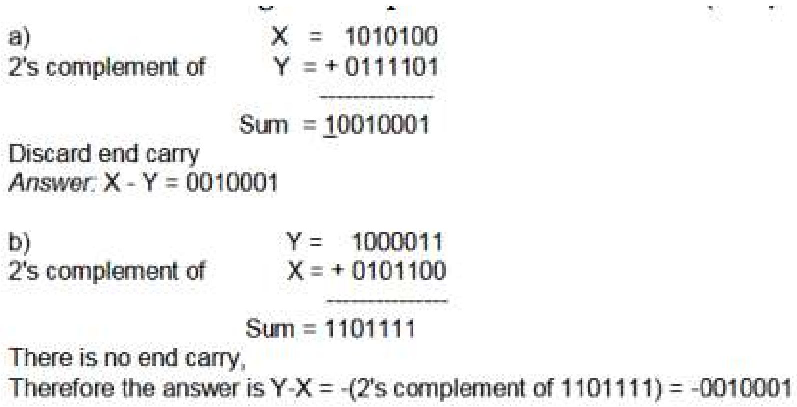
PART-A

1. **How many bits are required to represent the decimal numbers in the range 0 to 999 using straight binary code? Using BCD codes?**

(999) 10 = (1111100111) 2 → 10 bits are required using straight binary code

(999) 10 = (1001 1001 1001) BCD → 12 bits are required using BCD code

2. **Given 2 binary numbers. X = 1010100 and Y = 1000011. Find X –Y and Y – X using 2's compliments.**



a) X = 1010100

2's complement of Y = + 0111101

Sum = 10010001

Discard end carry

Answer: X - Y = 0010001

b) Y = 1000011

2's complement of X = + 0101100

Sum = 1101111

There is no end carry,

Therefore the answer is Y-X = -(2's complement of 1101111) = -0010001

3. **A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch.**

Which logic gate does the logic of switching of the bulb resembles?

XOR gate

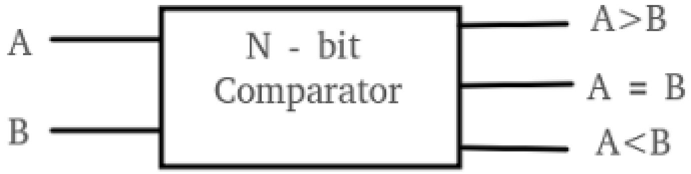
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

4. **Design the combinational circuit with 3 inputs and 1 output. The output is 1 when the binary value of the input is less than 3.**

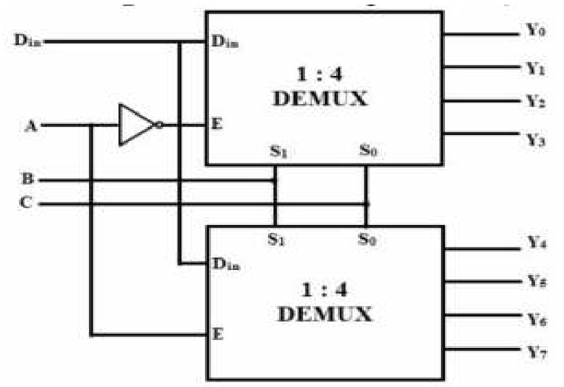
The output is 0 otherwise.

5. **What is magnitude comparator?**

A magnitude digital Comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition.



6. **Draw 1:8 Demultiplexer using two 1:4 Demultiplexer.**



7. **What is a priority encoder?**

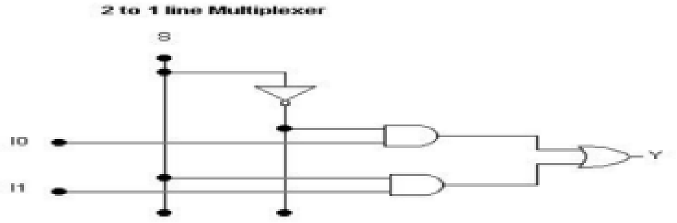
A priority encoder is an encoder circuit that includes the priority function. The operation of the priority encoder is such that if two or more inputs are activated at the same time, the output binary code will be generated to the highest-numbered input.

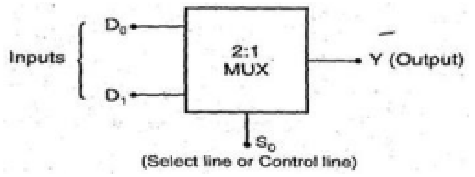
8. **Define Combinational circuit**.

A combinational circuit consists of logical gates whose outputs at any time are determined from the present combination of inputs.

A combinational circuit performs an operation that can be specified logically by a set of Boolean functions. It consists of input variables, gates and output variables.

9. **Draw the circuit for 2 to 1 multiplexer circuit. and Give functional block diagram of 2 * 1 MUX.**





10**. Define Karnaugh map.**

Karnaugh map is a map method that provides a simple, straightforward procedure for minimizing Boolean functions in canonical form.

This method may be regarded as a pictorial form of a truth table. A K-map is a diagram made up of squares, with each square representing one minterm of the function that is to be minimized.

11. **What are the limitations of k-map?**

i. Generally, it is limited to six variable map (i.e.) more than six variable involving expressions are not reduced.

ii. The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard form.

The minimum expression obtained might not be unique.

12. **List the advantages and disadvantages of BCD code**

The advantages of BCD code are

(i)Any large decimal number can be easily converted into corresponding binary number
(ii)A person needs to remember only the binary equivalents of decimal number from 0 to 9.
(iii)Conversion from BCD into decimal is also very easy.

The disadvantages of BCD code are

(i.) The code is least efficient. It requires several symbols to represent even small numbers.
(ii) Binary addition and subtraction can lead to wrong answer.
(iii) Special codes are required for arithmetic operations.
(iv) This is not a self-complementing code.
(v) Conversion into other coding schemes requires special methods

PART-B

1. i.Design a 4 bit adder / subtractor circuit and explain.

ii.What is BCD adder? Design an adder to perform arithmetic addition of two decimal digits in BCD.

2. Explain in detail about Encoders and Decoders.

3. (i) Implement the following Boolean functions with a multiplexer:

$F(w,x,y,z) = \sum (2,3,5,6,11,14,15)$

(ii).Implement the Boolean function $F(x,y,z) = \sum (1,2,6,7)$ using multiplexer

4. Design an one-bit and 2-bit magnitude comparator.

5. Simplify the following Boolean into (i) SOP form and (ii) POS form and implement the simplified functions using AND, OR gates.

$F(A,B,C,D) = \sum(0,1,2,5,8,9,10)$

6. Design a combinational circuit with 4 inputs, w, x, y and z and 3 outputs, a, b and c. When the binary input is 0, 1, 2, 3, 4, 5, 6, 7 the any of the 2 output is one. When the binary input is 8 to 14, the any of the one output is one and if all inputs is 1, all outputs are 1.

UNIT-II SYNCHRONOUS SEQUENTIAL LOGIC

PART-A

1.What is meant by triggering of Flip flop?

The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop

2.Define race around condition.

A race occurs with more than one bit change in state transitions because two bits are "racing" to be the other. for example 00 -> 11. it can be 01 first, or 10 first, and this may cause problems. When this leads to problems, it's called a critical race. but if this race condition eventually leads to the final or intended state anyway, it's ok. for example, with an input of 1, 00->11 is expected. but with an input of 1, the state 10 leads to next state 11, and the same is with 01 leading to next state 11. so you have no problem.

3.Mention the different types of shift registers.

There are 4 types of shift registers: serial in-serial out (SISO) shift registers, serial in-parallel out (SIPO) shift registers, parallel in-serial out (PISO) shift registers and parallel in-parallel out (PIPO) shift registers

4.What are the significances of state assignment?

In order to design a sequential circuit with physical components, it is necessary to assign unique coded binary values to the states. In synchronous circuits-state assignments are made with the objective of circuit reduction. Asynchronous circuits-its objective is to avoid critical races

5.What is edge triggered flip flop?

An edge-triggered flip-flop changes states either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input. The three basic types are introduced here: S-R, J-K and D.

6.What are Mealy and Moore machines?

A Mealy Machine changes its output on the basis of its present state and current input. Mealy machines react faster to inputs. They generally react in the same clock cycle.

A Moore Machine’s output depends only on the current state. It does not depend on the current input. In Moore machines, more logic is required to decode the outputs resulting in more circuit delays. They generally react one clock cycle later.

7.What are synchronous Counters?

The clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called Synchronous counter**.** Synchronous Counter examples are: Ring counter, Johnson counter etc…

8. Define state table.

The state table representation of a sequential circuit consists of three sections labeled present state, next state and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.

9. What is a state diagram?

(i) State diagram is the graphical representation of state table of sequential logic circuits.

(ii)In the state diagram, a state is represented by a circle and the transition between states is indicated by directed lines connecting the circles.

(iii)The directed lines are labeled with two binary numbers separated by a slash. The input value during the present state is labeled first and the number after the slash gives the output during the present state.

10. What do you meant by the term state reduction problem?

The reduction of the number of flip-flops in a sequential circuit is referred to as the state – reduction problem. State – reduction algorithms are concerned with procedures for reducing the number of states in a state table while keeping the external input – output requirements unchanged.

11. What is flip-flop?

Flip-flop is a sequential circuit which is used to store single bit of information at a time i.e. either 1 or 0 at a time. It has two stable output states. It can stay in one of the two stable states unless state is changed by applying external inputs. Thus, it as a basic memory element for storage of data in binary form. There are various types of flip-flops. 1.S-R flip flop 2.J-K flip-flop 3.D-flip flop 4.T-flip-flop.

12. How race around condition can be eliminated?

Race around condition can be eliminated in JK latch by two ways 1. Using the edge triggered J-K flip-flop. 2. Using the master slave J-K flip-flop.

13. What is the minimum number of flip-flops needed to build a counter of modulus 60?

Modulus N <2^6 = 64, k = 6 .The minimum number of flip-flops needed to build a counter of modulus 60 is 6.

14. If a serial-in-serial-out shift register has N stages and if the clock frequency is f, what will be the time delay between input and output?

Time delay between input and output = N / f

15. When is a counter said to suffer from lockout?

In a counter if the next state of some unused state is again an unused state and if by chance the counter happens to find itself in the unused states and never arrived at a used state then the counter is said to be in the lockout conditions.

PART-B

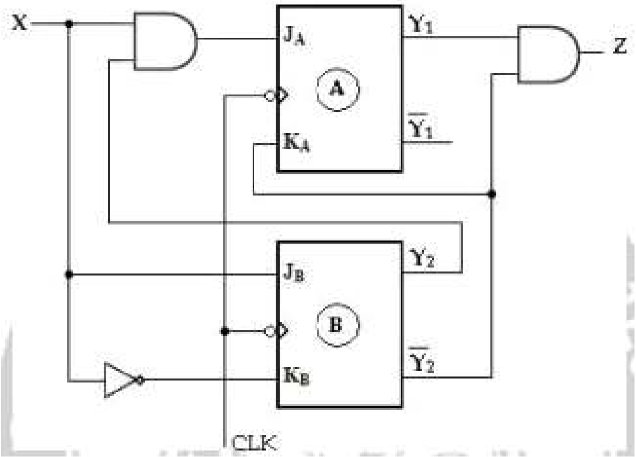
1.Explain the operation of JK FF, SR FF, T-FF and D-FF with a neat diagram. Also discuss their characteristic equation and excitation table.

2.What are registers ? Construct a 4 bit register using D flip flops and explain the operations on types of register.

3. Design a logic circuit diagram for 3-bit synchronous up-down counter.

4.Design a MOD-10 Synchronous counter using JK flip-flops. Write execution table and state table.

5.Analyze the synchronous Moore circuit and obtain its state diagram.



6.A sequential circuit with two ‘D’ Flip-Flops A and B, one input (x) and one output (y). The Flip-Flop input functions are: DA= Ax+ Bx DB= A’x and the circuit output function is, Y= (A+ B) x’.

(i) Draw the logic diagram of the circuit,
(ii) Tabulate the state table
(iii) Draw the state diagram.

UNIT-III COMPUTER FUNDAMENTALS

PART-A

1. **Define Moore’s Law.**
   Moore's law is the observation that, over the history of computing hardware, the number of transistors on integrated circuits doubles approximately every 18 to 24 months.

   The law is named after Intel co-founder Gordon E. Moore, who described the trend in his 1965 paper.
2. **Define the terms response time and throughput.**
   The response time is the time between the start and completion of a task also referred to as execution time.

   The throughput or bandwidth-.the total amount of work done in a given unit of time

3. **What are the operations of computer hardware?**

An operation, in computing, is an action that is carried out to accomplish a given task. There are five basic types of computer operations: inputting, processing, outputting, storing and controlling.
Computer operations are executed by the five primary functional units that make up a computer system. The units correspond directly to the five types of operations. They include the input unit, storage unit, output unit and two of the main components in the central processing unit (CPU) -- the arithmetic logic unit (ALU) and the control unit (CU).

4. ***What is meant by* Operands?**

Operands are definite elements of computer instruction that show what information is to be operated on. The most important general categories of data are

1. Addresses
2. Numbers
3. Characters
4. Logical data

5. **Define Instruction set completeness.**

A set of instructions is said to be complete if the computer includes a sufficient number of instructions in each of the following categories:

- Arithmetic, logical and shift instructions
- A set of instructions for moving information to and from memory and processor registers.
- Instructions which controls the program together with instructions that check status conditions.
- Input and Output instructions

6. **What is meant by instruction sequencing?**

The order in which the instructions in a program are carried out. Normally the sequence proceeds in a linear fashion through the program,
and the address of the instructions is obtained from the program counter in the control unit.

Instruction Execution Sequence

1. Read instruction from memory (*fetch*)
2. Read machine state (*read*)
3. Perform operation (*execute*)
4. Update machine state (*update*)

7. **Difference between memory location and memory address.**
   Memory addresses are fixed-length sequences of digits conventionally displayed and manipulated as unsigned integers.
   Memory location in a stored-program computer holds a binary number or decimal number of some sort.
8. **Define Addresing modes and their types.**
   The term addressing modes refers to the way in which the operand of an instruction is specified. The addressing mode specifies a rule for interpreting or modifying the address field of the instruction before the operand is actually executed.

Types of Addressing Modes

- Immediate Addressing
- Register Addressing.
- Indirect Addressing.
- Indexed Addressing.
- Based Addressing.

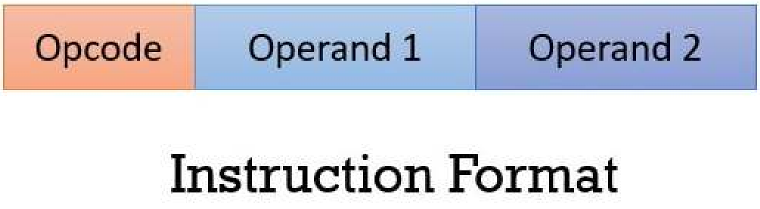
9. **Define ISA and their types.**

The *Instruction Set Architecture* (ISA) is the part of the processor that is visible to the programmer or compiler writer. The ISA serves as the boundary between software and hardware.

The 3 most common types of ISAs are:

Stack - The operands are implicitly on top of the stack.
Accumulator - One operand is implicitly the accumulator.
General Purpose Register (GPR) - All operands are explicitely mentioned, they are either registers or memory locations.

10. What is meant by instruction format and types?



The **Opcode** shown above determines the nature of the **operation** to be performed. The **operands**, Operand 1 and operand 2 identify the data on which operation has to be performed. The operand can be a **memory location, a processor register, immediate value** or **logical data.**

11. Mention instruction format types.

1. Instructions that **transfers** the data between the memory of the computer and processor register.
2. Instructions that can perform **arithmetic and logical operations** on the data.
3. Instructions controlling the **sequencing** of execution of instructions, like branch instruction.
4. Instructions performing the **I/O transfer** i.e. transferring the data from internal storage to the external storage or device.

12. What do you meant by Assembly Language Notation?

Assembly Language notations are used to represent the **machine instructions**. An assembly language instruction specifies the **operation**, that has to be performed and the **operands** that will be involved in the operation.

Assembly language instruction use **mnemonics** to denote the operations. These mnemonics are nothing but the abbreviation of the word that describes the nature of operation. Like, for addition it has Add, for Multiplication it has Mul, for division Div.

PART-B

1. With neat diagram, describe about Von Neumann Architecture.

2. Discuss about Instructions and Instruction sequencing.

3. What are addressing modes? Explain the various addressing modes with examples.

4. Describe about an encoding of machine instructions with an example.

5.Write any program and show the interaction between assembly and high level language.

6. Write a note on i.ISA ii.Address and Machine instruction

UNIT-IV PROCESSOR

1, **Define data hazard.**

A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline. A data hazard is a situation in which the pipeline is stalled because the data to be operated on are delayed for some reason.

2. **List the two steps involved in executing an instruction.**

- Fetch the Instruction
- Fetch the operands

3. **Define data path element.**

A unit used to operate on or hold data within a processor. In the MIPS Implementation, the data path elements include the instruction and data memories, the register file, the ALU, and adders.

4. List the five stages of instruction execution.

1. IF: Instruction fetch
2. ID: Instruction decode and register file read
3. EX: Execution or address calculation
4. MEM: Data memory access
5. WB: Write back

5. How data hazard can be prevented in pipelining?

Data hazards in the instruction pipelining can prevented by the following techniques.

a) Operand Forwarding b) Software Approach

6**. Define Pipelining.**

In order to reduce the overall processing time several instructions are being executed simultaneously. This process is termed as pipelining.

7. **Define instruction hazard or control hazard.**

A pipeline may also be stalled because of the delayed in the availability of an instruction. This may be a result of a miss in the catch, requiring the instruction to be fetched from the main memory. Such hazard are often called control hazard..

8. **Give the major limitation of pipelining technique.**

If an instruction is stalled in the pipeline, no later instructions can proceed. Thus, if there is a dependency between two closely spaced instructions in the pipeline, it will stall.

9. **How addressing modes affect the instruction pipelining?**

Degradation of performance is an instruction pipeline may be due to address dependency where operand address cannot be calculated without available information needed by addressing mode for e.g. An instructions with register indirect mode cannot proceed to fetch the operand if the previous instructions is loading the address into the register. Hence operand access is delayed degrading the performance of pipeline.

10. **List out the methods used to improve system performance.**

The methods used to improve system performance are

1. Processor clock
2. Basic Performance Equation
3. Pipelining
4. Clock rate
5. Instruction set
6. Compiler

11. What is the difference between uniprocessor and multiprocessor?

Uniprocessor: - A type of architecture that is based on a single computing unit. All operations (additions, multiplications, etc) are done sequentially on the unit.

Multiprocessor: - A type of architecture that is based on multiple computing units. Some of the operations (not all, mind you) are done in parallel and the results are joined afterwards.

12. Define MIPS.

MIPS is an instruction execution rate, MIPS specifies performance inversely to execution time; faster computers have a higher MIPS rating.

13. Define the Term WORD.

The natural unit of access in a computer, usually a group of 32 bits; corresponds to the size of a register in the MIPS architecture.

14. What are called data transfer instructions?

MIPS must include instructions that transfer data between memory and registers. Such instructions are called data transfer instructions. To access a word in memory, the instruction must supply the memory address. Memory is just a large, single-dimensional array, with the address acting as the index to that array, starting at 0.

PART-B

1. Describe the data path and control considerations for pipelining.
2. Describe in detail about micro programmed control.
3. Describe about pipelining?
4. Explain in detail about how a control unit is designed in a processor.
5. Write a short note on Data hazard and Control hazards
6. With neat example explain about an instruction execution.

UNIT –V MEMORY AND I/O

PART-A

1. Define is memory access time.

The time that elapses between the initiation of an operation and the completion of that operation is called memory access time. e.g.: time between the read and the MFC signal.

2. Define memory cycle time.

Memory cycle time is the minimum time delay required between the initiation of two successive memory operations.eg: time between two successive read operations.

3. What is cache memory?

Cache memory is a small, fast memory that is inserted between the larger, slower main memory and the processor.
It holds the currently active segments of a program and their data.

4. What are the uses of memory management unit?

The virtual address space is mapped onto the physical memory where data are actually stored.

A special memory control circuit, often called the memory management unit, implements the mapping function.

5. Define memory latency and bandwidth.

The term memory latency is used to refer to the amount of time it takes to transfer a word of data to or from the memory. If the performance measure is defined in terms of the number of bits or bytes that can be transferred in one second, then the measure is called memory bandwidth.

6. Define seek time, rotational time and access time?

-Seek time is the time required to move the read/write head to the proper track.

-Rotational or latency time is the amount of time that elapses after the head is positioned over the correct track until the starting position of the address sector passes under the read/write head. The sum of these above two delays is called the disk access time.

7. An address space is specified by 24 bits and the corresponding memory space by 16 bits: How many words are in the (a) virtual memory (b) main memory.

We consider a unit of memory called page. A page is typically rather large, for example 4 KB (4096 bytes). A page is the unit of memory that is transferred between disk and main memory. A virtual page is either in memory or on disk. Example: 32-bit virtual address space Pages that are 4 KB large (4 KB = 212 bytes) 16 MB main memory (16 MB = 224 bytes)

8. Define − Rotational Latency

Rotational latency, also called rotational delay, is the time required for the desired sector of a disk to rotate under the read/write head, usually assumed to be half the rotation time.

9. What is direct-mapped cache?

Direct-mapped cache is a cache structure in which each memory location is mapped to exactly one location in the cache. For example, almost all directmapped caches use this mapping to find a block, (Block address) modulo (Number of blocks in the cache).

10. What are the writing strategies in cache memory?

Write-through is a scheme in which writes always update both the cache and the next lower level of the memory hierarchy, ensuring that data is always consistent between the two. Write-back is a scheme that handles writes by updating values only to the block in the cache, then writing the modified block to the lower level of the hierarchy when the block is replaced.

11. What are the various block placement schemes in cache memory?

Direct-mapped cache is a cache structure in which each memory location is mapped to exactly one location in the cache. Fully associative cache is a cache structure in which a block can be placed in any location in the cache. Set-associative cache is a cache that has a fixed number of locations (at least two) where each block can be placed.

12. What is meant by USB?

A USB-A port refers to a port in a host device that allows it to connect with a receptor device, either through a USB cable or by plugging in the receptor device directly (as with a USB flash drive). USB drives are commonly used for **storage, data backup and transferring files between devices**. USB drives come in multiple storage capacities and different ports, each having a unique shape.

13. Define SATA.

SATA, in full **serial advanced technology attachment**, also called **serial ATA**, an interface for transferring data between a computer's central circuit board and storage devices. SATA replaced the long-standing PATA (parallel ATA) interface.

Serial communication transfers data one bit at a time, rather than in several parallel streams.

14. What is the need for Hierarchy of Memories?

Programmers want memory to be fast, large, and cheap. The hierarchical arrangement of storage in current computer architectures is called the memory hierarchy.

It is designed to take advantage of memory locality in computer programs. Each level of the hierarchy is of higher speed and lower latency, and is of smaller size, than lower levels.

PART-B

1. Explain DMA Controller with the block diagram?
2. Explain the various mapping techniques associated with cache memories.
3. i. Explain the Address Translation in Virtual Memory.

   ii. Write a short note on interrupt I/O.
4. Discuss about Parallel and serial interface.
5. Describe in detail about memory management.
6. i.Analyze the memory hierarchy in terms of speed, size and Cost

   ii. Write about an interconnection standards.